1-A, Positive Fixed Voltage, Low-Dropout Regulator

FEATURES

- **1.5% Typical Accuracy**
- **Low I_Q: 100 µA (max)**
  - **500 times lower than standard 1117 devices**
- **V_{IN}: 2.0 V to 5.5 V**
  - **Absolute maximum V_{IN} = 6.0 V**
- **Stable with 0-mA Output Current**
- **Low Dropout: 455 mV at 1 A for V_{OUT} = 3.3 V**
- **High PSRR: 65 dB at 1 kHz**
- **Minimum Ensured Current Limit: 1.1 A**
- **Stable with Cost-Effective Ceramic Capacitors:**
  - **With 0-Ω ESR**
- **Temperature Range: –40°C to +125°C**
- **Thermal Shutdown and Ovecurrent Protection**
- **Available in SOT223 Package**
  - **See *Package Option Addendum* at end of this document for complete list of available voltage options**

APPLICATIONS

- **Set Top Boxes**
- **TVs and Monitors**
- **PC Peripherals, Notebooks, Motherboards**
- **Modems and Other Communication Products**
- **Switching Power Supply Post-Regulation**

DESCRIPTION

The TLV1117LV series of low-dropout (LDO) linear regulators is a low input voltage version of the popular 1117 voltage regulator.

The TLV1117LV is an extremely low-power device that consumes 500 times lower quiescent current than traditional 1117 voltage regulators, making it suitable for applications that mandate very low standby current. The TLV1117LV family of LDOs is also stable with 0 mA of load current; there is no minimum load requirement, making it an ideal choice for applications where the regulator is required to power very small loads during standby in addition to large currents on the order of 1 A during normal operation. The TLV1117LV offers excellent line and load transient performance, resulting in very small magnitude undershoots and overshoots of output voltage when the load current requirement changes from less than 1 mA to more than 500 mA.

A precision bandgap and error amplifier provides 1.5% accuracy. A very high power-supply rejection ratio enables usage of the device for post-regulation after a switching regulator. Other valuable features include low output noise and low-dropout voltage.

The device is internally compensated to be stable with 0-Ω equivalent series resistance (ESR) capacitors. These key advantages enable the use of cost-effective, small-size ceramic capacitors. Cost-effective capacitors that have higher bias voltages and temperature derating can also be used if desired.

The TLV1117LV series is available in a SOT223 package.

TLV1117LVxxDCY

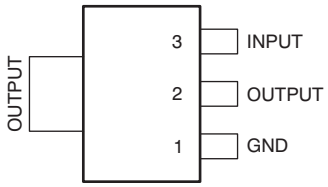

Figure 1.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TLV1117LV**vv***(A)***yyyz**	**VV** is the nominal output voltage (for example, 33 = 3.3 V). ***YYY*** is the package designator. **Z** is the package quantity. Use *R* for reel (2500 pieces), and *T* for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = +25°C (unless otherwise noted). All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	Input voltage range, V_{IN}	–0.3	+6.0	V
	Output voltage range, V_{OUT}	–0.3	+6.0	V
Current	Maximum output current, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Dissipation Ratings* Table		
Temperature	Operating junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Ratings	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV1117LV DCY 3 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	62.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	47.2	
θ_{JB}	Junction-to-board thermal resistance	12.0	
ψ_{JT}	Junction-to-top characterization parameter	6.1	
ψ_{JB}	Junction-to-board characterization parameter	11.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	T_A < +25°C
High-K(1)	DCY	47.2	62.9	1.59 W

(1) The JEDEC high K (2s2p) board used to derive these data was a 3-inch x 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

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ELECTRICAL CHARACTERISTICS

At $V_{IN} = V_{OUT(TYP)} + 1.5$ V; I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			TLV1117LV Series MIN	TLV1117LV Series TYP	TLV1117LV Series MAX	UNIT
V_{IN}	Input voltage range				2.0		5.5	V
V_{OUT}	DC output accuracy	V_{OUT} > 2 V			–1.5		+1.5	%
		1.5 V ≤ V_{OUT} < 2 V			–2		+2	%
		1.2 V ≤ V_{OUT} < 1.5 V			–40		+40	mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA				1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 1 A				1	35	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 x $V_{OUT(NOM)}$	V_{OUT} < 3.3 V	I_{OUT} = 200 mA		115		mV
				I_{OUT} = 500 mA		285		mV
				I_{OUT} = 800 mA		455		mV
				I_{OUT} = 1 A		570	800	mV
			V_{OUT} ≥ 3.3 V	I_{OUT} = 200 mA		90		mV
				I_{OUT} = 500 mA		230		mV
				I_{OUT} = 800 mA		365		mV
				I_{OUT} = 1 A		455	700	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$			1.1			A
I_Q	Quiescent current	I_{OUT} = 0 mA				50	100	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA, f = 100 Hz				65		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 2.8 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA				60		μV_{RMS}
t_{STR}	Startup time(2)	C_{OUT} = 1.0 µF, I_{OUT} = 1 A				100		µs
UVLO	Undervoltage lockout	V_{IN} rising				1.95		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing				+165		°C
		Reset, temperature decreasing				+145		°C
T_J	Operating junction temperature				–40		+125	°C

(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ = 2.5 V so that V_{IN} = 2.45 V.
(2) Startup time = time from when V_{IN} asserts to when output is sustained at a value greater than or equal to 0.98 × $V_{OUT(NOM)}$.

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FUNCTIONAL BLOCK DIAGRAM

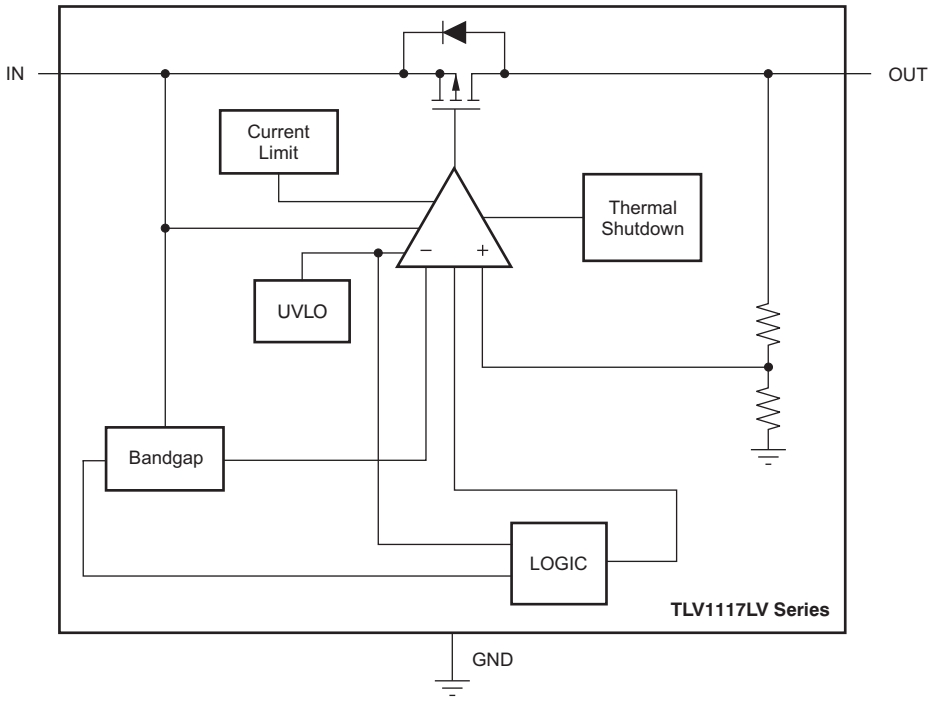
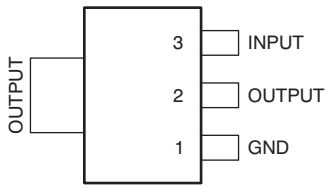


Figure 2. TLV1117LV Block Diagram

PIN CONFIGURATIONS

DCY PACKAGE
SOT223
(TOP VIEW)



PIN DESCRIPTIONS

TLV1117LV(1)		DESCRIPTION
NAME	TLV1117LVDCY	
IN	3	Input pin. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
OUT	2, Tab	Regulated output voltage pin. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	1	Ground pin

(1) Shaded cells indicate preview device.

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TYPICAL CHARACTERISTICS

At $V_{IN} = V_{OUT(TYP)} + 1.5$ V; $I_{OUT} = 10$ mA, $C_{OUT} = 1.0$ µF, and $T_A = +25°C$, unless otherwise noted.

LINE REGULATION

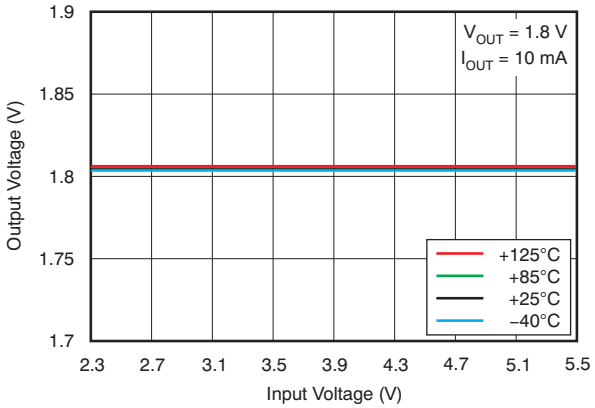

Figure 3.

LINE REGULATION

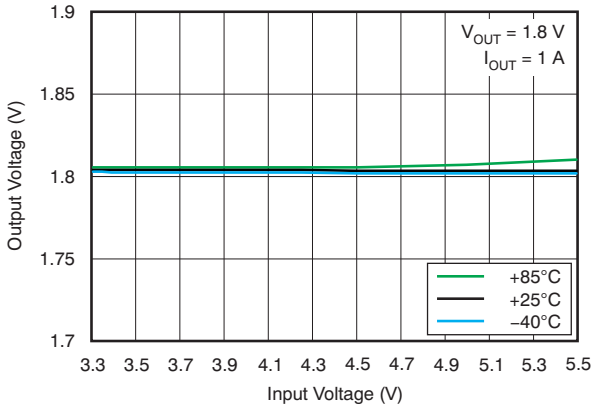

Figure 4.

LOAD REGULATION

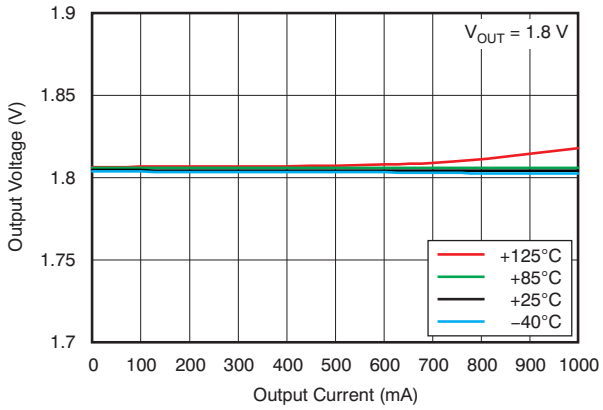

Figure 5.

DROPOUT VOLTAGE vs INPUT

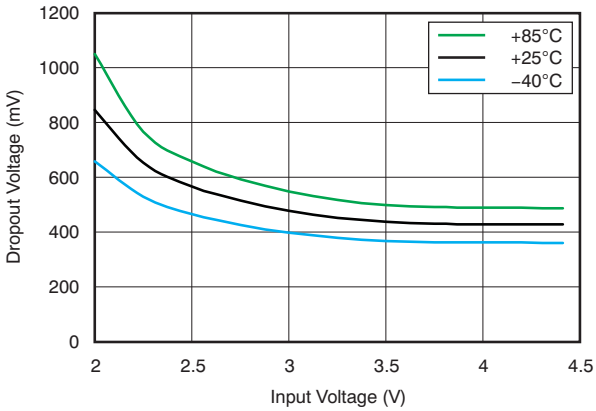

Figure 6.

DROPOUT VOLTAGE vs OUTPUT

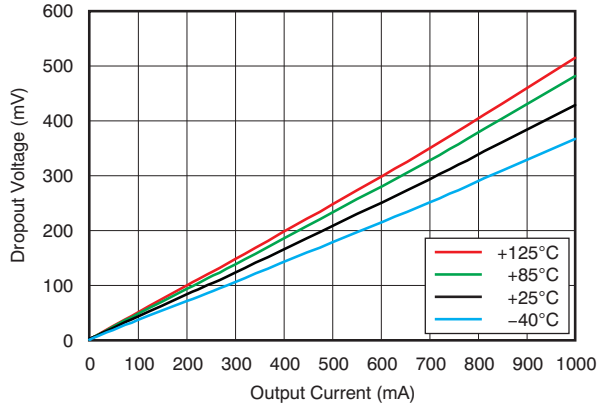

Figure 7.

OUTPUT VOLTAGE vs TEMPERATURE

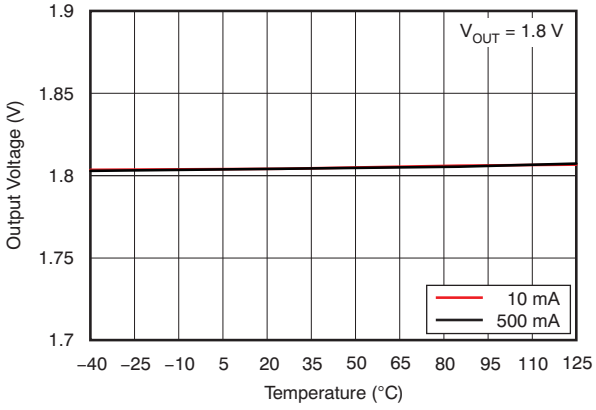

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

At $V_{IN} = V_{OUT(TYP)} + 1.5$ V; $I_{OUT} = 10$ mA, $C_{OUT} = 1.0$ µF, and $T_A = +25°C$, unless otherwise noted.

QUIESCENT CURRENT vs LOAD

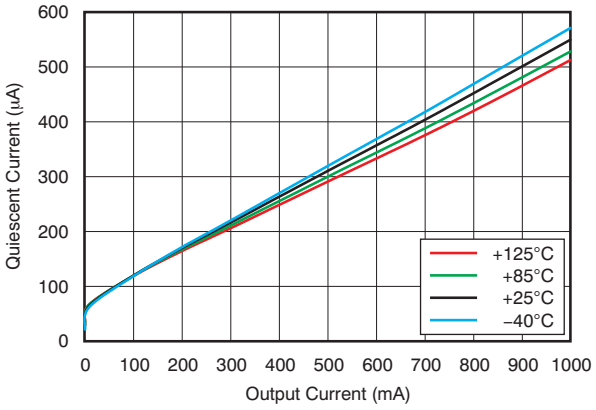

Figure 9.

CURRENT LIMIT vs INPUT VOLTAGE

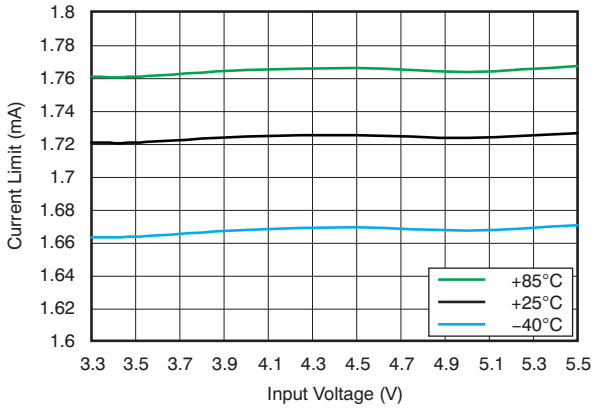

Figure 10.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

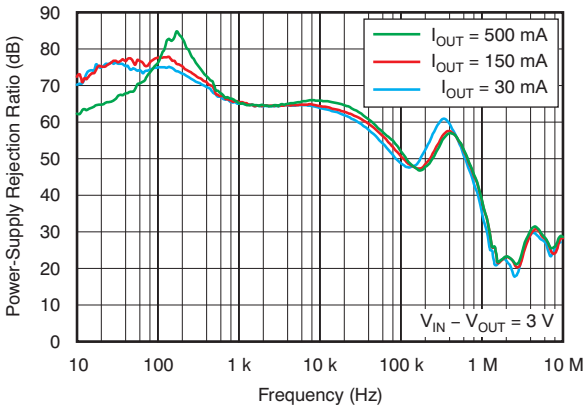

Figure 11.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

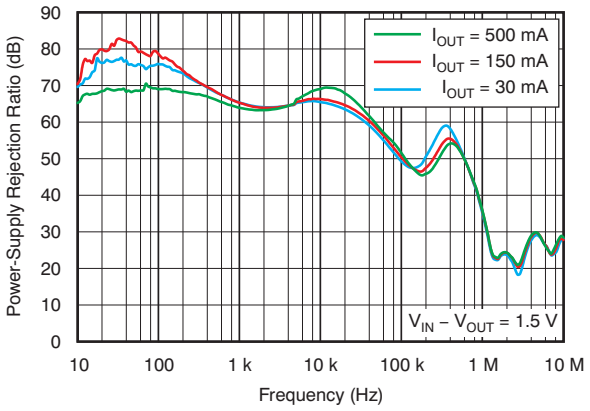

Figure 12.

POWER-SUPPLY REJECTION RATIO vs OUTPUT CURRENT

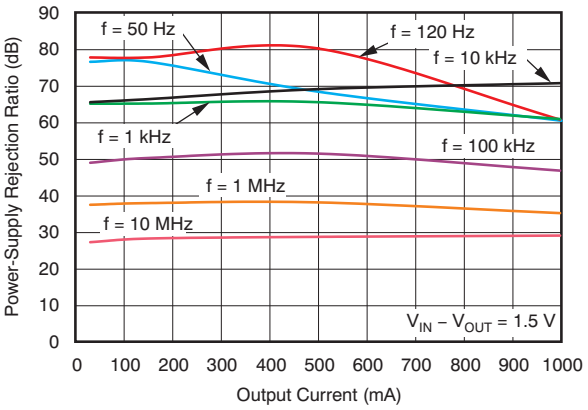

Figure 13.

SPECTRAL NOISE DENSITY vs FREQUENCY

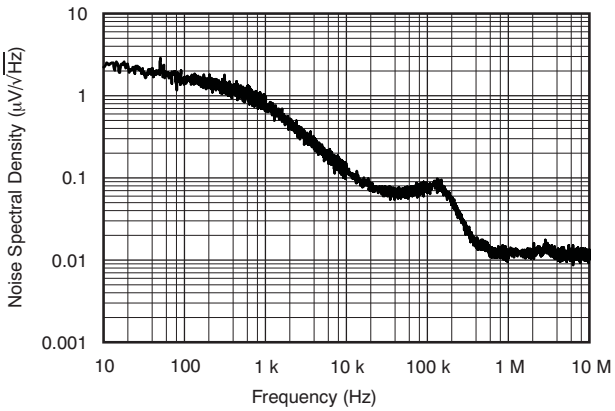

Figure 14.

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TYPICAL CHARACTERISTICS (continued)

At $V_{IN} = V_{OUT(TYP)} + 1.5$ V; $I_{OUT} = 10$ mA, $C_{OUT} = 1.0$ µF, and $T_A = +25°C$, unless otherwise noted.

LOAD TRANSIENT RESPONSE
200 mA to 500 mA, C_{OUT} = 1 µF

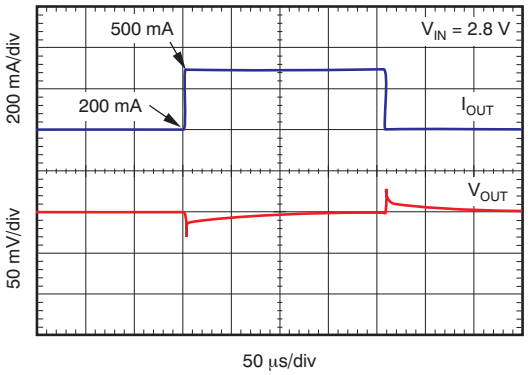

Figure 15.

LOAD TRANSIENT RESPONSE
200 mA to 500 mA, C_{OUT} = 10 µF

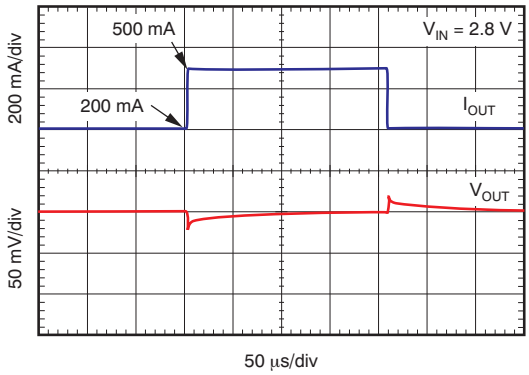

Figure 16.

LOAD TRANSIENT RESPONSE
1 mA to 500 mA, C_{OUT} = 1 µF

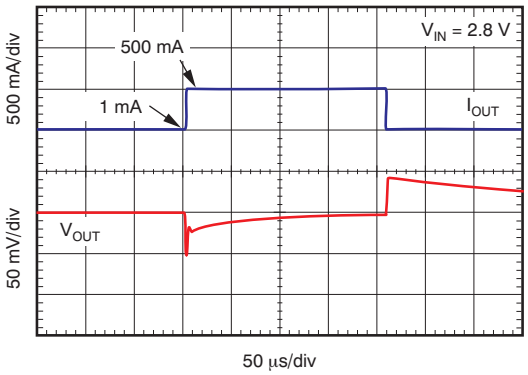

Figure 17.

LOAD TRANSIENT RESPONSE
1 mA to 500 mA, C_{OUT} = 10 µF

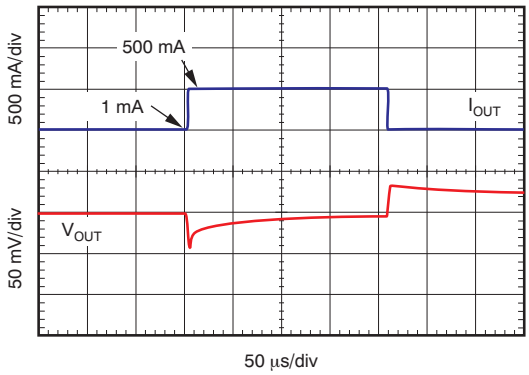

Figure 18.

LOAD TRANSIENT RESPONSE
200 mA to 1 A, C_{OUT} = 1 µF

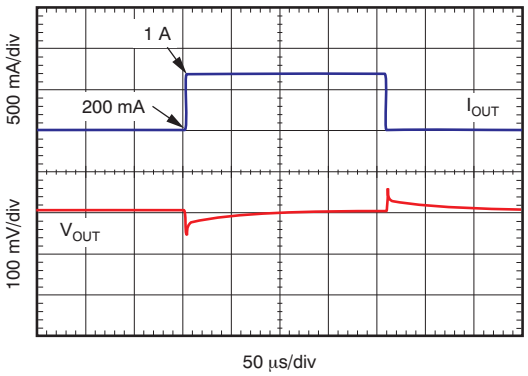

Figure 19.

LOAD TRANSIENT RESPONSE
200 mA to 1 A, C_{OUT} = 10 µF

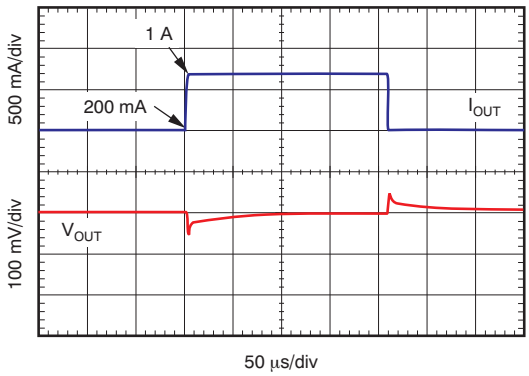

Figure 20.

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TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 1.5 V; I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = +25°C, unless otherwise noted.

LOAD TRANSIENT RESPONSE
1 mA to 1 A, C_{OUT} = 1 µF

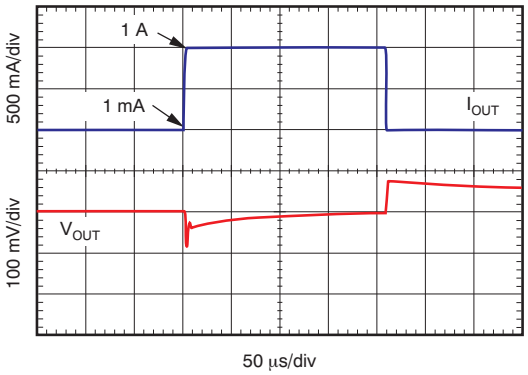

Figure 21.

LOAD TRANSIENT RESPONSE
1 mA to 1 A, C_{OUT} = 10 µF

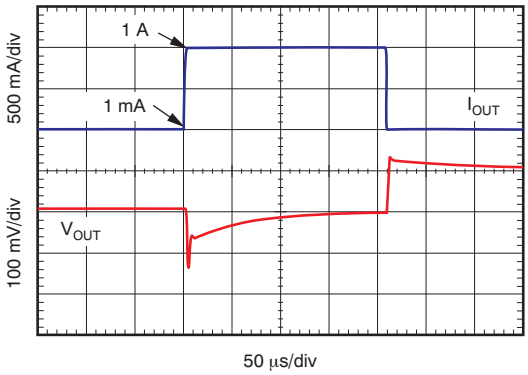

Figure 22.

LINE TRANSIENT RESPONSE
V_{OUT} = 1.8 V, I_{OUT} = 10 mA

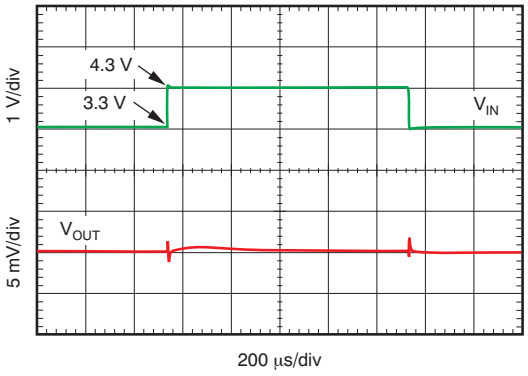

Figure 23.

LINE TRANSIENT RESPONSE
V_{OUT} = 1.8 V, I_{OUT} = 500 mA

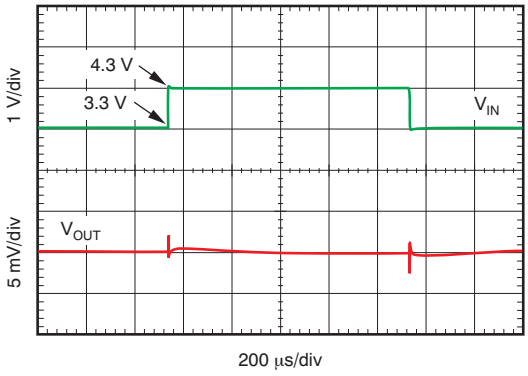

Figure 24.

LINE TRANSIENT RESPONSE
V_{OUT} = 1.8 V, I_{OUT} = 1 A

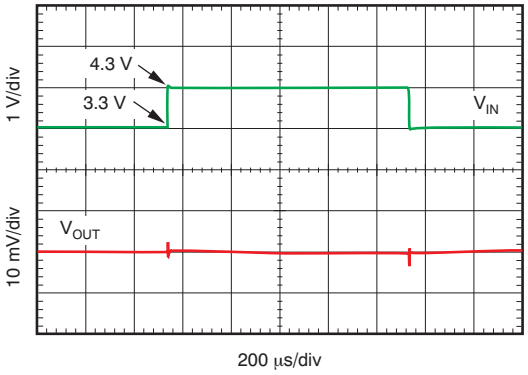

Figure 25.

LINE TRANSIENT RESPONSE
V_{OUT} = 1.8 V, I_{OUT} = 10 mA

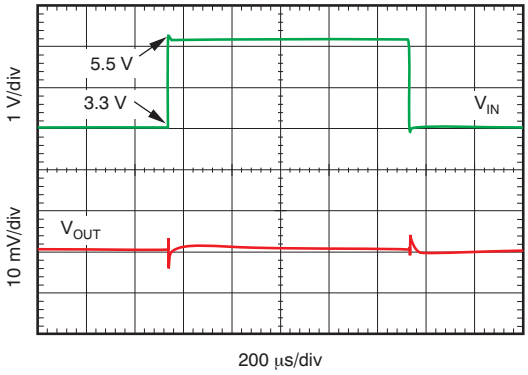

Figure 26.

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TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 1.5 V; I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = +25°C, unless otherwise noted.

LINE TRANSIENT RESPONSE
V_{OUT} = 1.8 V, I_{OUT} = 500 mA

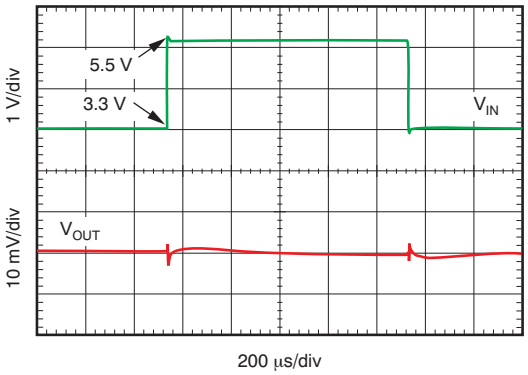

Figure 27.

LINE TRANSIENT RESPONSE
V_{OUT} = 1.8 V, I_{OUT} = 1 A

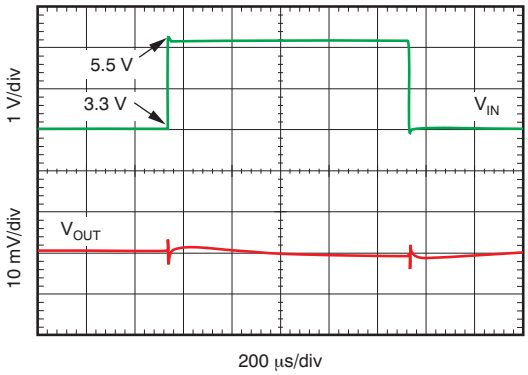

Figure 28.

APPLICATION INFORMATION

The TLV1117LV is a low quiescent current linear regulator designed for high current applications. Unlike typical high current linear regulators, the TLV1117LV series consume significantly less quiescent current. These devices deliver excellent line and load transient performance. The device is low noise, and exhibits a very good power-supply rejection ratio (PSRR). As a result, it is ideal for high current applications that require very sensitive power-supply rails.

This family of regulators offers both current limit and thermal protection. The operating junction temperature range of the device is –40°C to +125°C.

Input and Output Capacitor Requirements

For stability, 1.0-µF ceramic capacitors are required at the output. Higher-valued capacitors improve transient performance. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. Unlike traditional linear regulators that need a minimum ESR for stability, the TLV1117LV series are ensured to be stable with no ESR. Therefore, cost-effective ceramic capacitors can be used with these devices. Effective output capacitance that takes bias, temperature, and aging effects into consideration must be greater than 0.5 µF to ensure stability of the device.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF, low-ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located physically close to the power source. If source impedance is greater than 2 Ω, a 0.1-µF input capacitor may also be necessary to ensure stability.

Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors should be placed as close to the device pins as possible. To improve characteristic ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. Higher value ESR capacitors may degrade PSRR performance.

Internal Current Limit

The TLV1117LV internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and can be calculated by the formula: $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details

The PMOS pass element in the TLV1117LV device has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Dropout Voltage

The TLV1117LV uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} – V_{OUT})$ approaches dropout

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude.

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Undervoltage Lockout (UVLO)

The TLV1117LV uses an undervoltage lockout circuit keep the output shut off until internal circuitry operating properly.

Thermal Information

Thermal protection disables the output when the junction temperature rises to approximately +165°C,allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV1117LV has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV1117LV into thermal shutdown degrades device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1:

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} \quad (1)$$

Package Mounting

Current solder pad footprint recommendations for the TLV1117LV are available from the Texas Instruments web site at www.ti.com. The mechanical drawing for the DCY (SOT223) package and the recommended land pattern for the DCY (SOT223) package are both appended to this data sheet.

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REVISION HISTORY

NOTE: Page numbers from previous revisions may differ from page numbers in the current version.

Changes from Original (May, 2011) to Revision A	Page
• Updated front-page figure	1
• Corrected errors in pin numbers listed in Pin Descriptions table and shown in device pinout	4
• Deleted example mechanical drawing and land pattern figures (Figure 29 and Figure 30, respectively)	11

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLV1117LV12DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV12DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV15DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV15DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV18DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV18DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV25DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV25DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV28DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV28DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV30DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV30DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV33DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TLV1117LV33DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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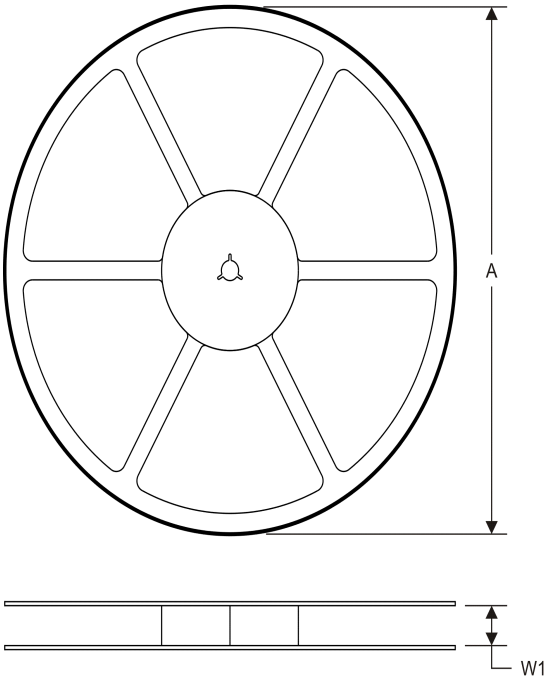
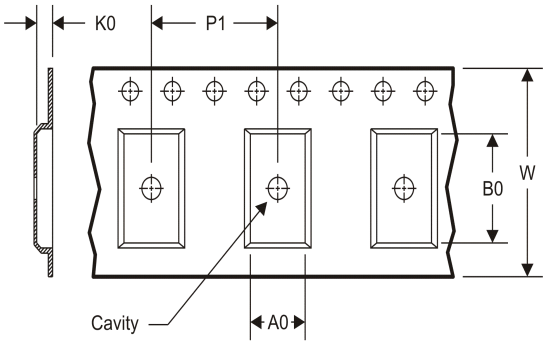
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



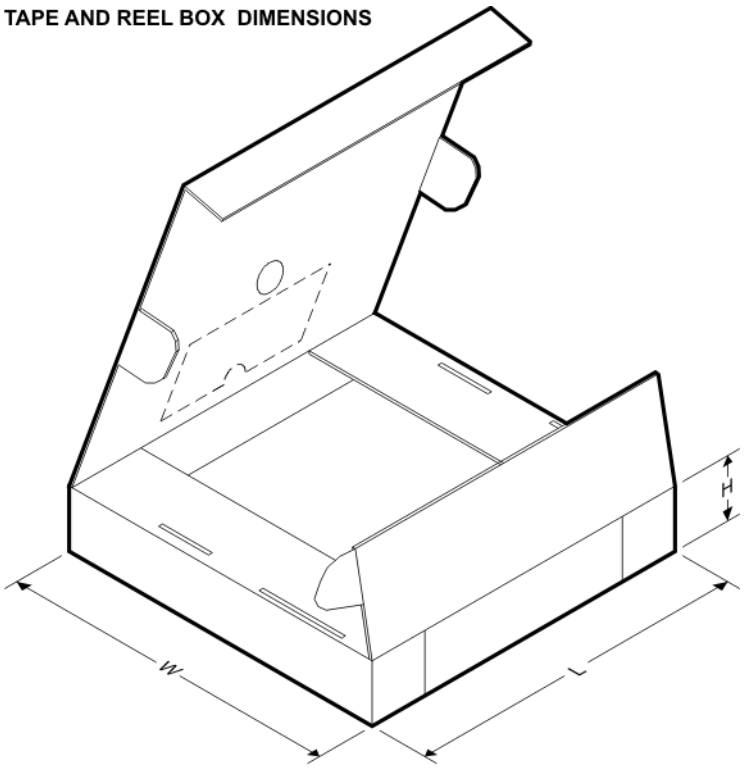
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117LV12DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TLV1117LV12DCYT	SOT-223	DCY	4	250	177.8	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TLV1117LV18DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TLV1117LV18DCYT	SOT-223	DCY	4	250	177.8	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TLV1117LV25DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV25DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV33DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TLV1117LV33DCYT	SOT-223	DCY	4	250	177.8	12.4	7.05	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

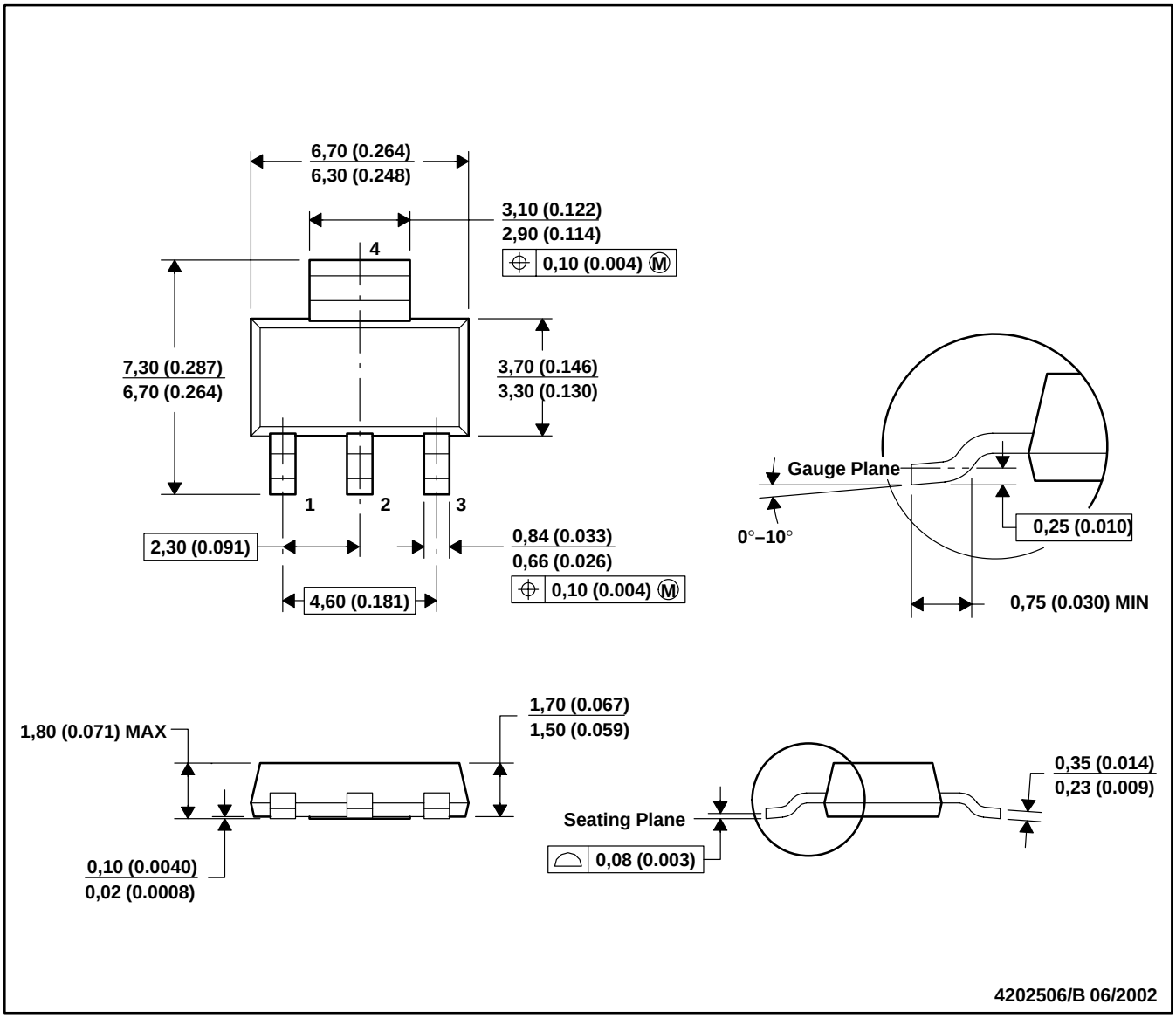


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117LV12DCYR	SOT-223	DCY	4	2500	358.0	335.0	35.0
TLV1117LV12DCYT	SOT-223	DCY	4	250	358.0	335.0	35.0
TLV1117LV18DCYR	SOT-223	DCY	4	2500	358.0	335.0	35.0
TLV1117LV18DCYT	SOT-223	DCY	4	250	358.0	335.0	35.0
TLV1117LV25DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV25DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV33DCYR	SOT-223	DCY	4	2500	358.0	335.0	35.0
TLV1117LV33DCYT	SOT-223	DCY	4	250	358.0	335.0	35.0

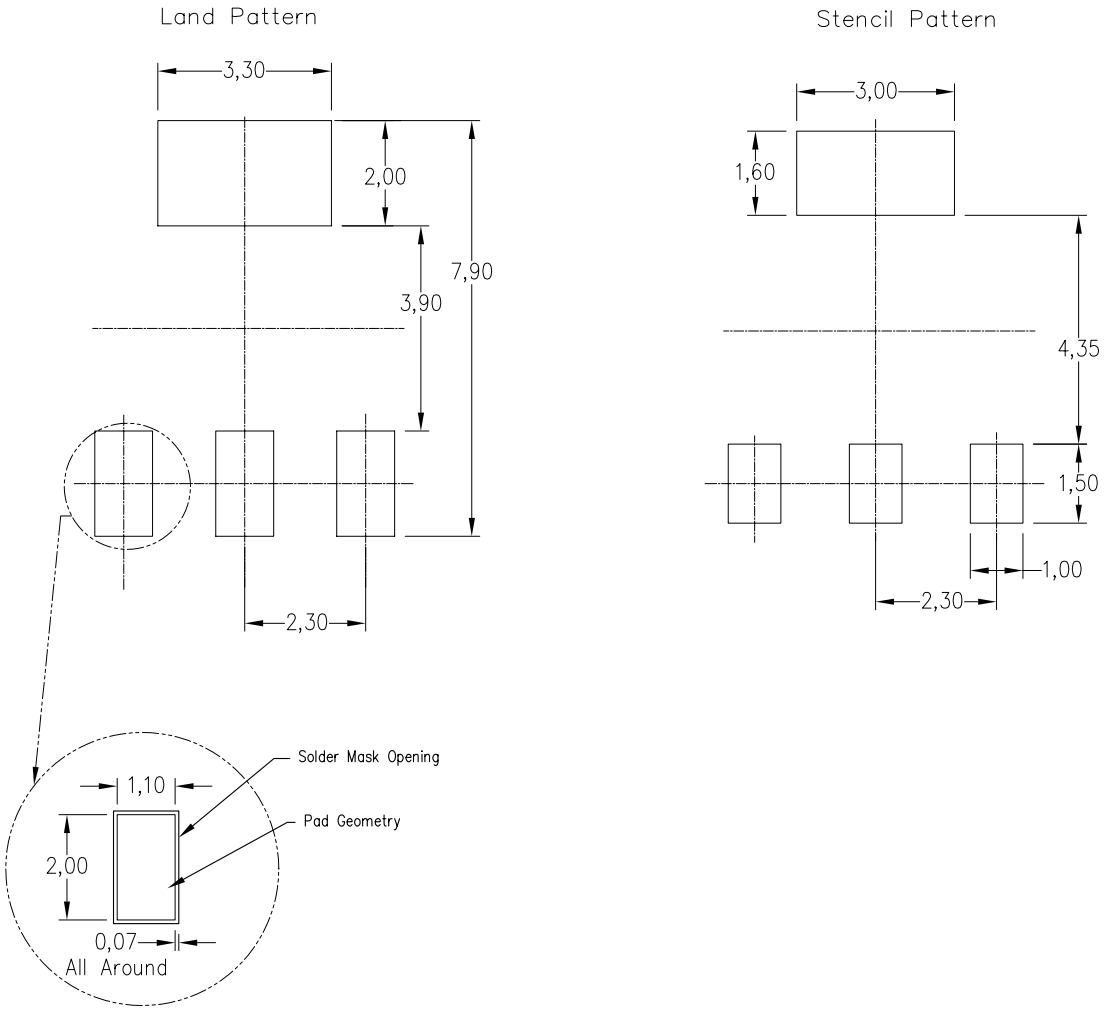
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



4210278/B 11/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.

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