TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS054C – Revised September 2003

CD4069UB Types

CMOS Hex Inverter

High-Voltage Types (20-Volt Rating)

■ CD4069UB types consist of six CMOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter/Buffers are not required.

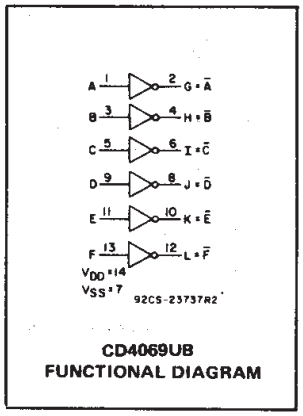
The CD4069UB-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation—t_{PHL},t_{PLH}=30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative **Standard No. 13B,** "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Logic inversion
- Pulse shaping
- Oscillators
- High-input-impedance amplifiers



CD4069UB
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

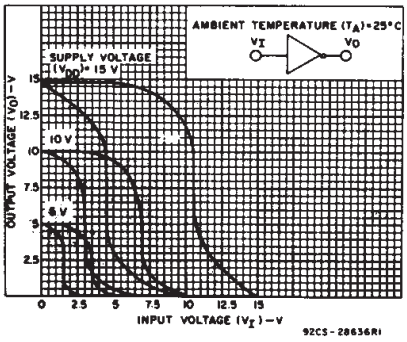


Fig. 1 – Minimum and maximum voltage transfer characteristics.

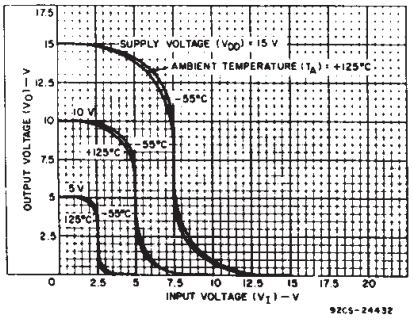


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time;	t_{PLH}, t_{PHL}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance;	C_{IN}	Any Input	10	15	pF

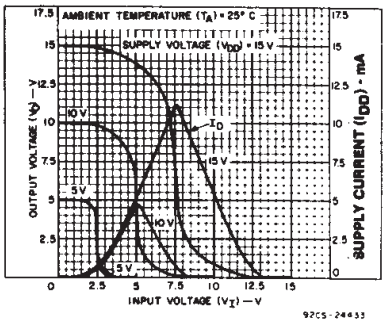


Fig. 3 – Typical current and voltage transfer characteristics.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	5	5	0.05				–	0	0.05	V
	–	10	10	0.05				–	0	0.05	
	–	15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0	5	4.95				4.95	5	–	
	–	0	10	9.95				9.95	10	–	
	–	0	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2				—	—	2	
	13.5	–	15	2.5				–	—	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	—	—	
	1	–	10	8				8	—	—	
	1.5	–	15	12.5				12.5	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

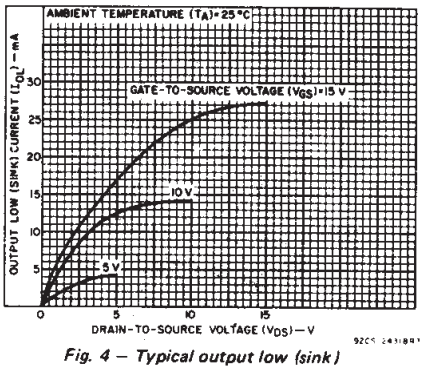


Fig. 4 – Typical output low (sink) current characteristics.

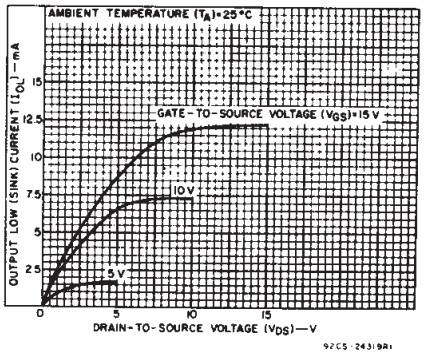


Fig. 5 – Minimum output low (sink) current characteristics.

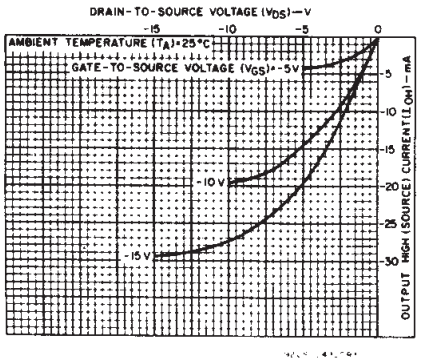


Fig. 8 – Typical output high (source) current characteristics.

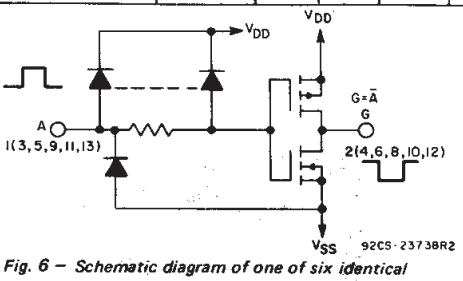


Fig. 6 – Schematic diagram of one of six identical inverters.

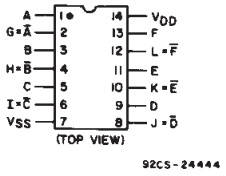


Fig. 7 – CD4069UB terminal assignment.

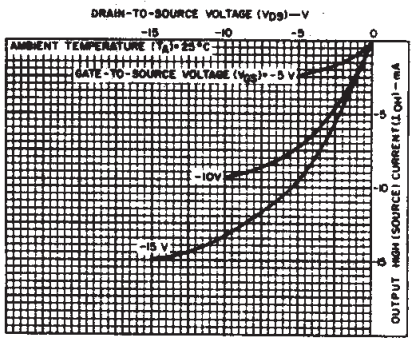


Fig. 9 – Minimum output high (source) current characteristics.

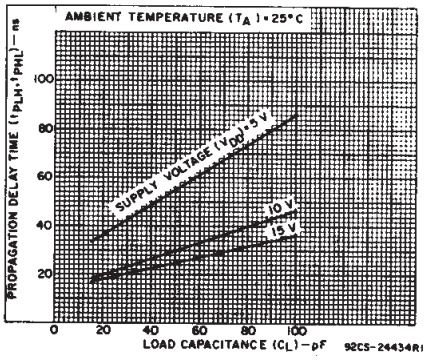


Fig. 10 – Typical propagation delay time vs. load capacitance.

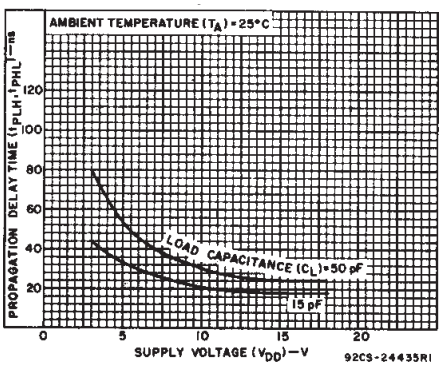


Fig. 11 – Typical propagation delay time vs. supply voltage.

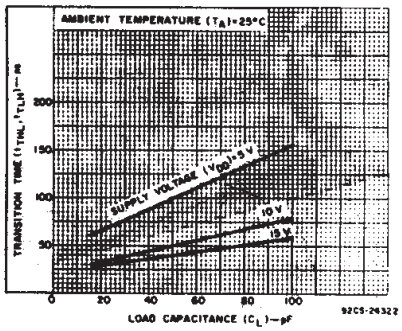


Fig. 12 – Typical transition time vs. load capacitance.

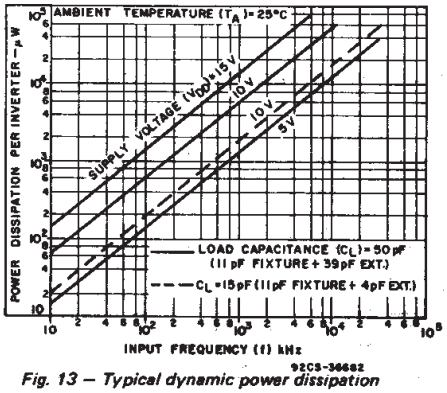


Fig. 13 – Typical dynamic power dissipation vs. frequency.

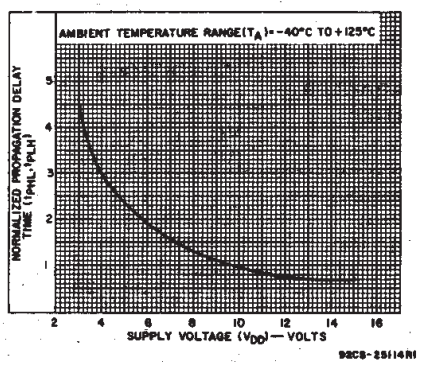


Fig. 14 – Variation of normalized propagation delay time (t_{PHL} and t_{PLH}) with supply voltage.

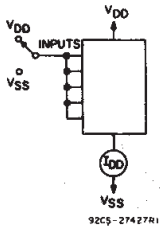


Fig. 15 – Quiescent device current test circuit.

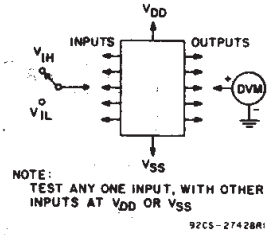


Fig. 16 – Noise immunity test circuit.

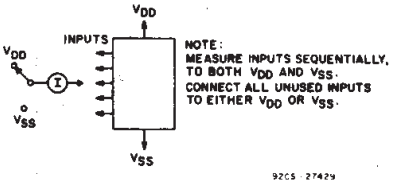
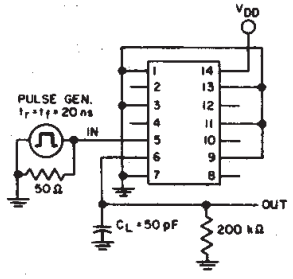


Fig. 17 – Input leakage current test circuit.



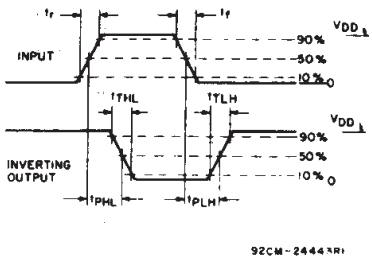


Fig. 18 – Dynamic electrical characteristics test circuit and waveforms.

APPLICATIONS

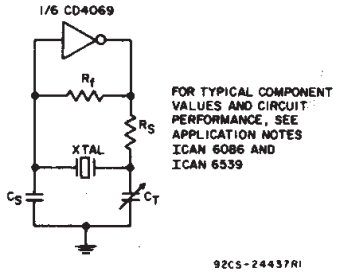


Fig. 19 – Typical crystal oscillator circuit.

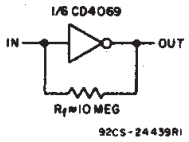


Fig. 20 – High-input impedance amplifier.

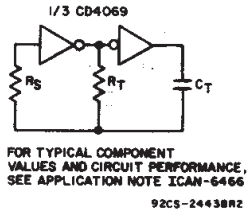
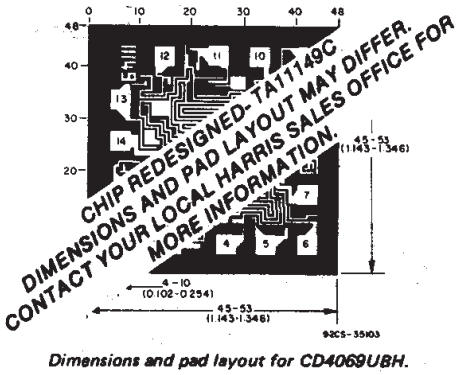


Fig. 21 – Typical RC oscillator circuit.



Dimensions and pad layout for CD4069UBH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

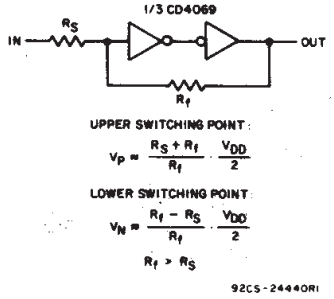


Fig. 22 – Input pulse shaping circuit (Schmitt trigger).

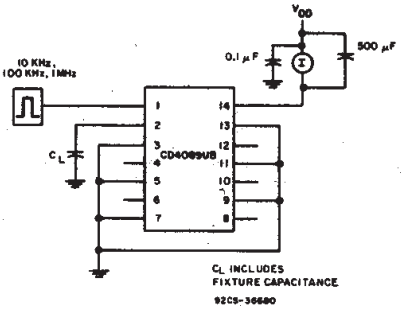


Fig. 23 – Dynamic power dissipation test circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4069UBE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4069UBE	Samples
CD4069UBEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4069UBE	Samples
CD4069UBF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4069UBF	Samples
CD4069UBF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4069UBF3A	Samples
CD4069UBM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM	Samples
CD4069UBM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	CD4069UBM	Samples
CD4069UBM96E4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		Samples
CD4069UBM96G4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	CD4069UBM	
CD4069UBME4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	CD4069UBM	Samples
CD4069UBMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM	Samples
CD4069UBMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM	Samples
CD4069UBMTE4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	CD4069UBM	Samples
CD4069UBMTG4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	CD4069UBM	Samples
CD4069UBNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UB	Samples
CD4069UBNSRE4	ACTIVE	SO	NS	14		TBD	Call TI	Call TI	-55 to 125	CD4069UB	Samples
CD4069UBNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UB	Samples
CD4069UBPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
CD4069UBPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4069UBPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
CD4069UBPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
CD4069UBPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
CD4069UBPWRG4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-55 to 125	CM069UB	Samples
JM38510/17401BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 17401BCA	Samples
M38510/17401BCA	ACTIVE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125	JM38510/ 17401BCA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4069UB, CD4069UB-MIL :

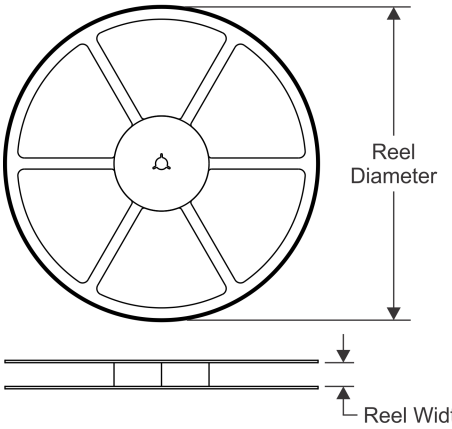
- Catalog: CD4069UB
- Military: CD4069UB-MIL

NOTE: Qualified Version Definitions:

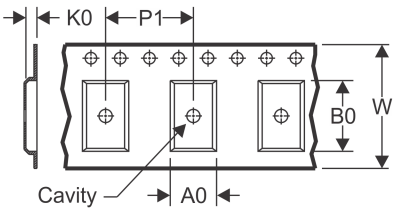
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

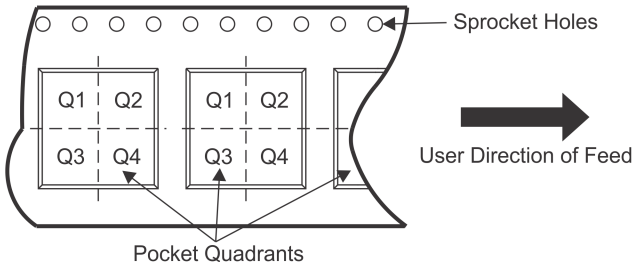


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

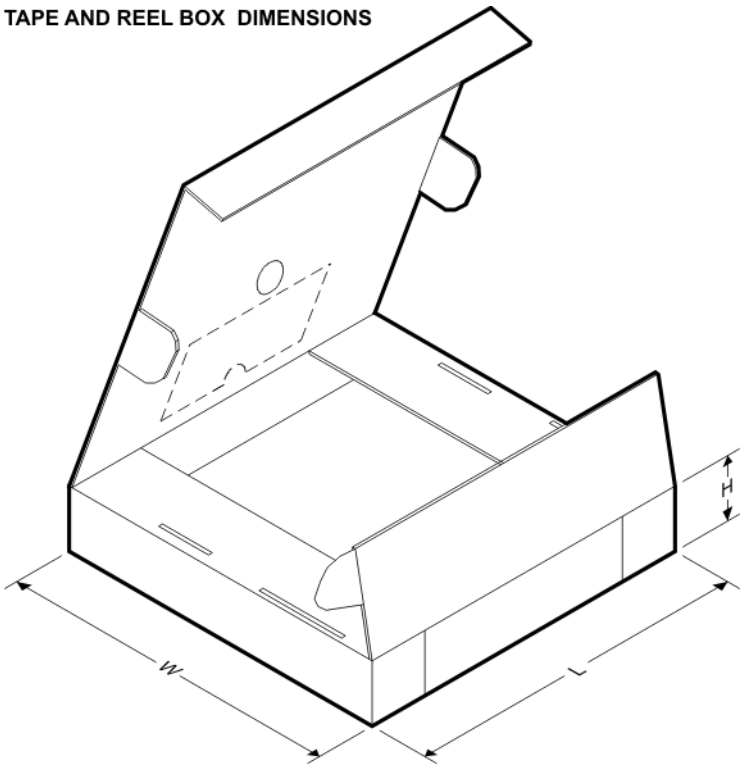
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4069UBM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4069UBM96	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
CD4069UBMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4069UBNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4069UBPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



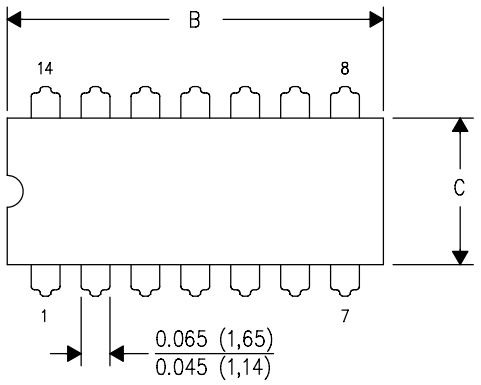
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4069UBM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4069UBM96	SOIC	D	14	2500	364.0	364.0	27.0
CD4069UBMT	SOIC	D	14	250	367.0	367.0	38.0
CD4069UBNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4069UBPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

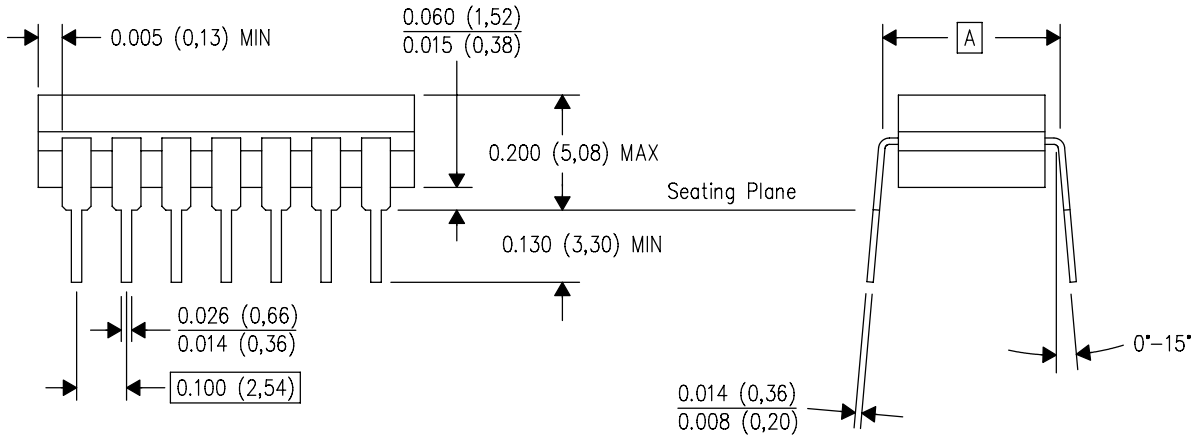
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



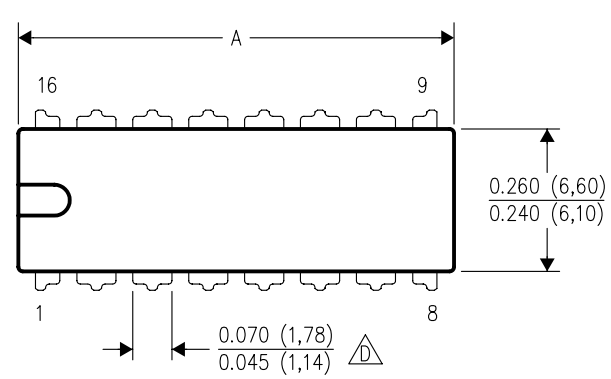
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

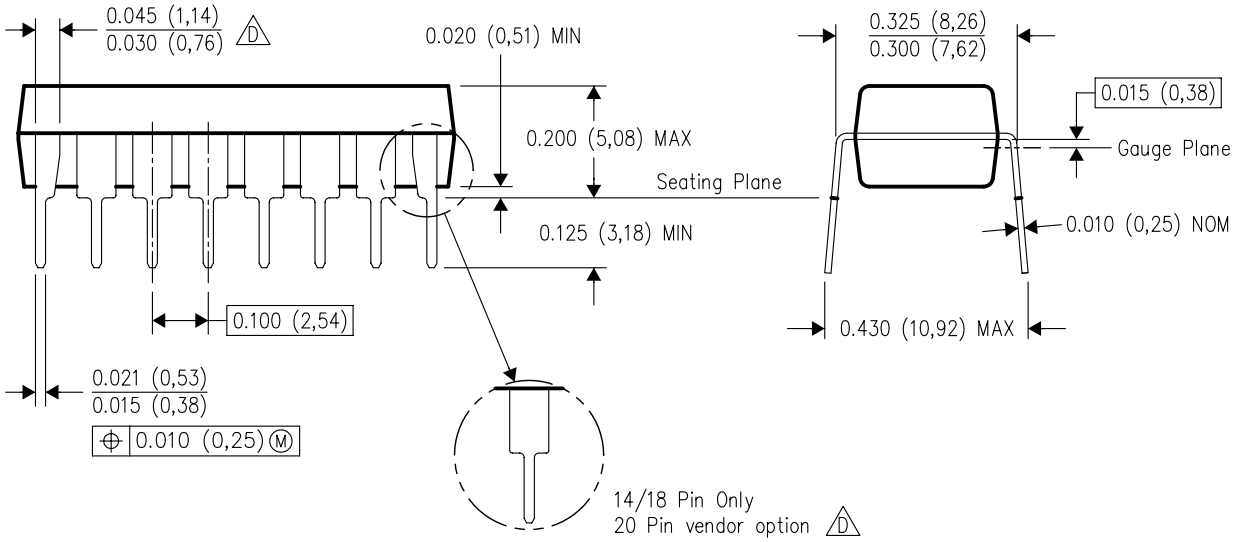
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



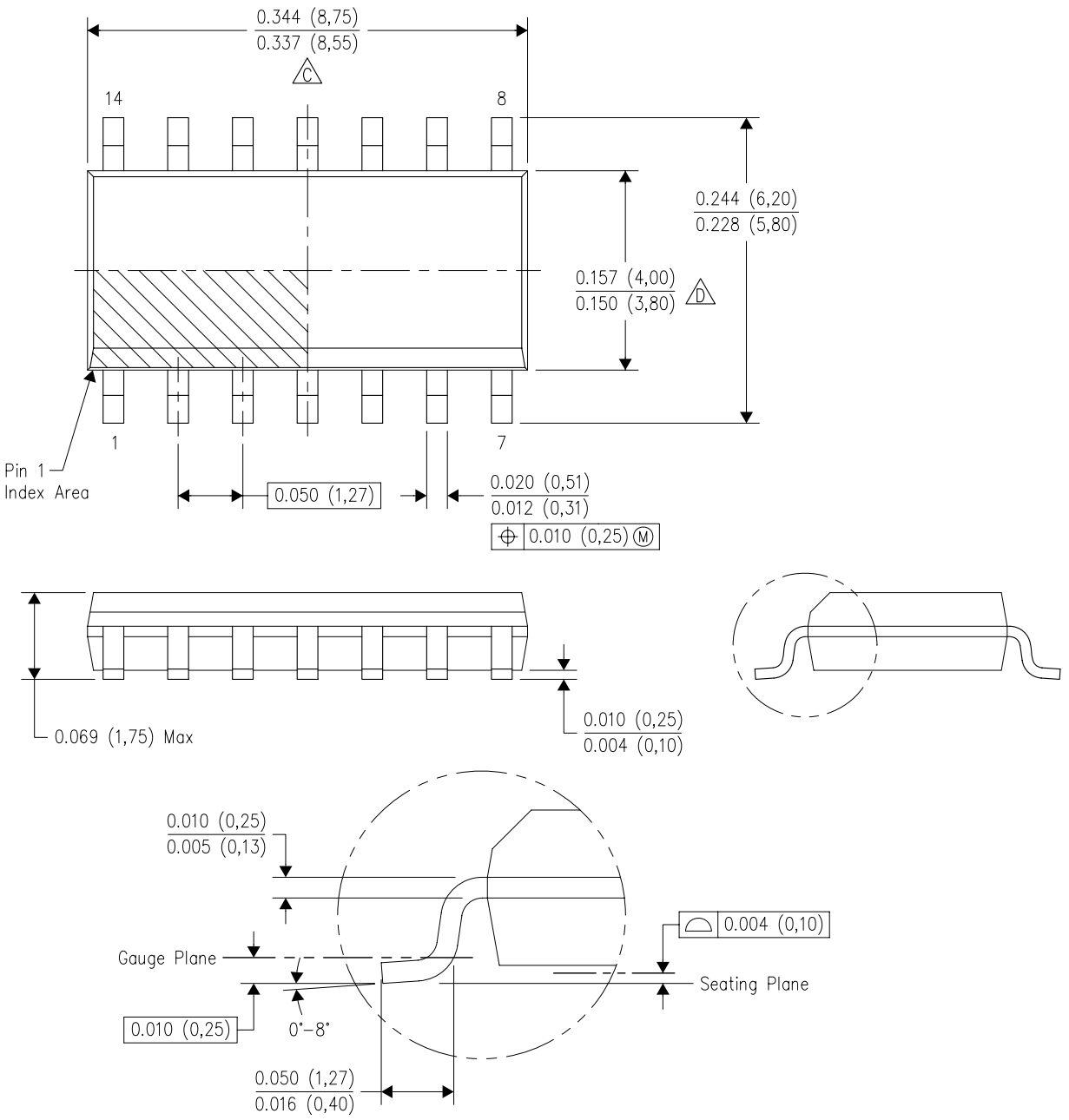
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

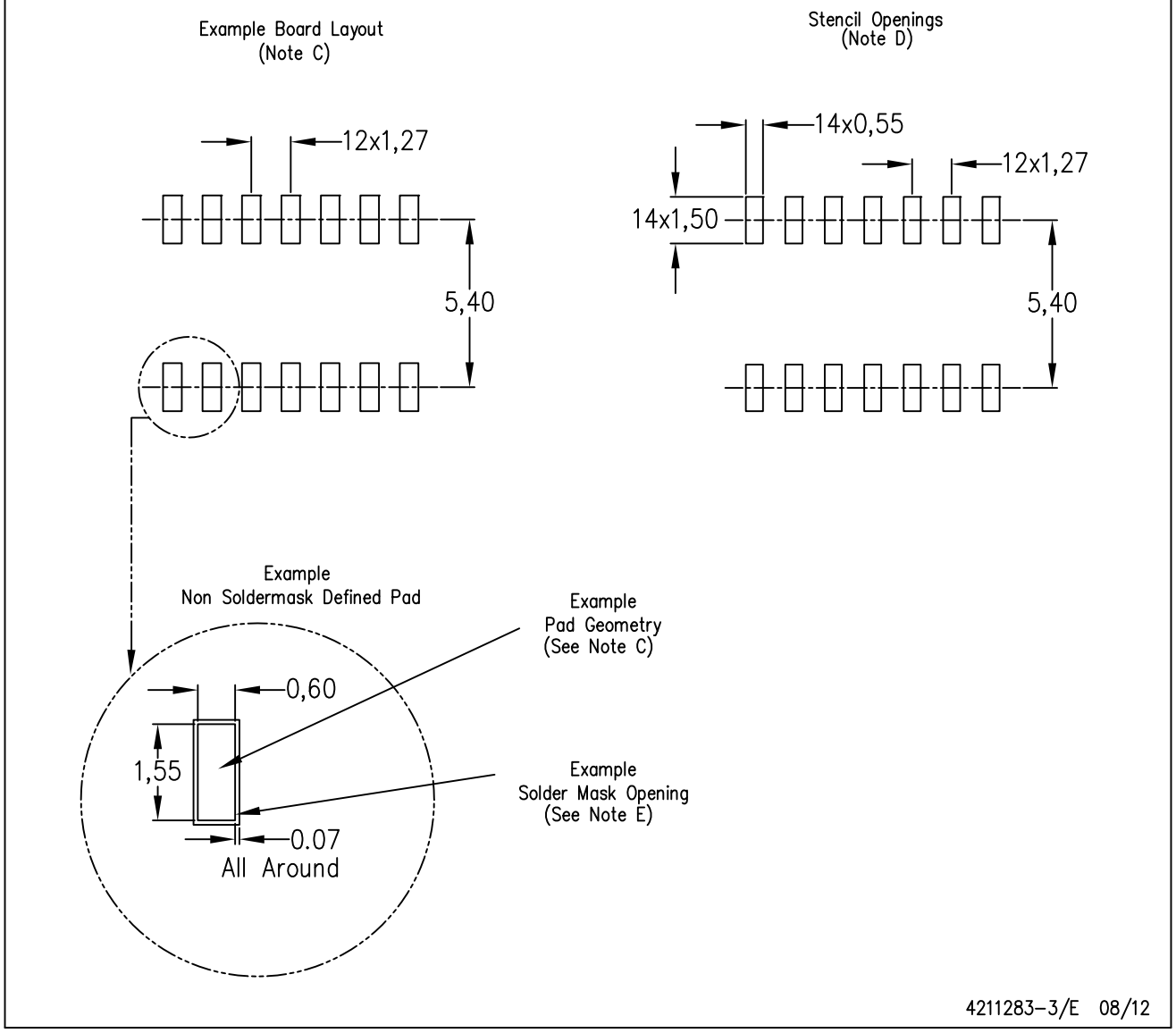
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



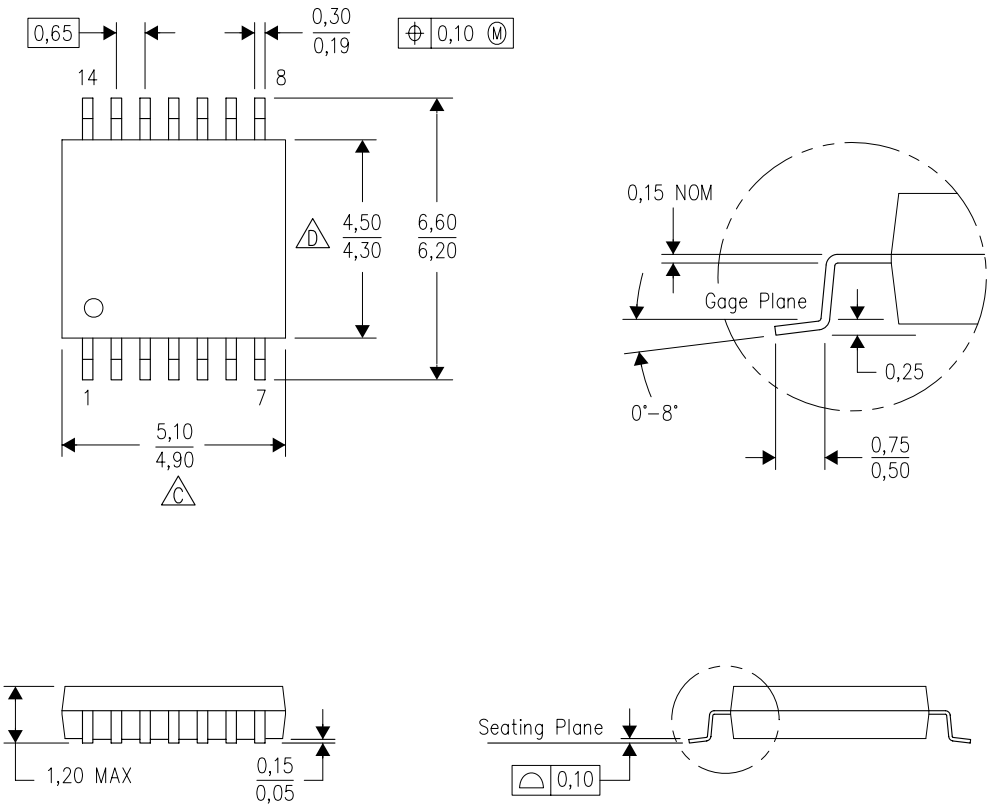
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

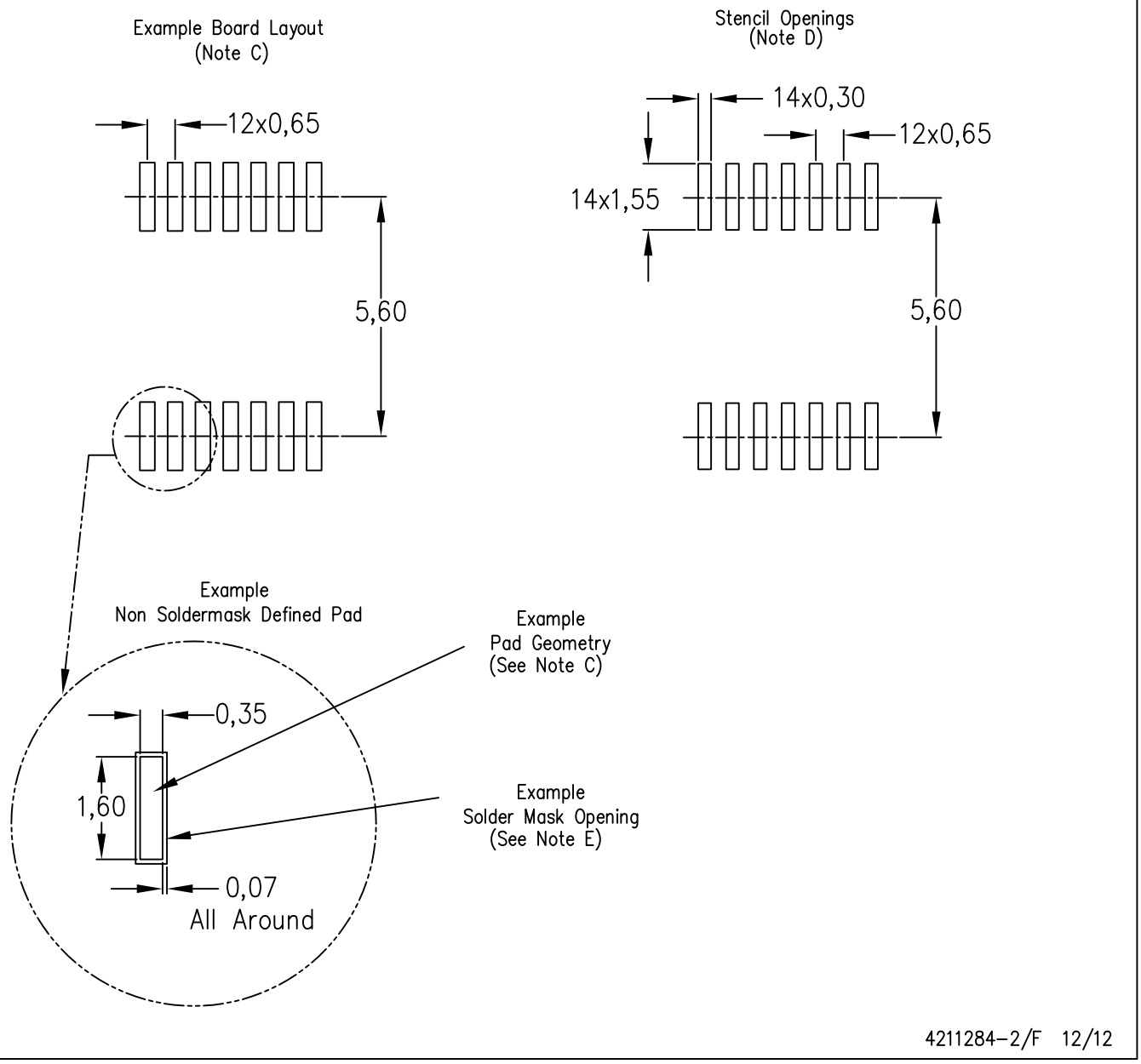
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

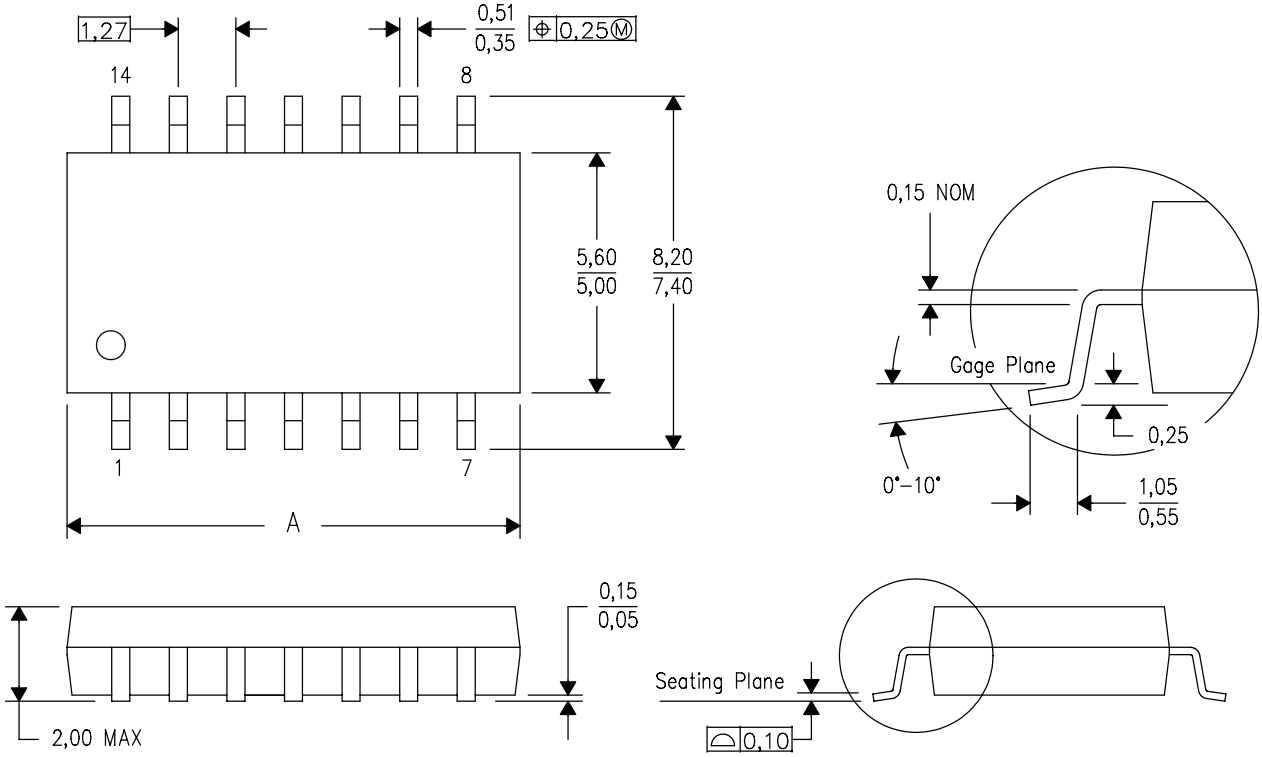


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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