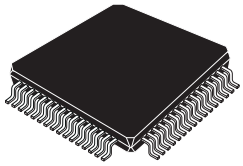
TDA7421N

AM/FM TUNER FOR CAR RADIO AND HI-FI APPLICATIONS

PRELIMINARY DATA

- HIGH PERFORMANCE FRONT-END IC FOR AM/FM RECEIVERS
- FULLY INTEGRATED HIGH-SPEED PLL FOR OPTIMIZED RDS APPLICATIONS
- FM MPX/AM AUDIO OUTPUT, 450kHz AM IF OUTPUT FOR STEREO AM APPLICATIONS
- AM DOUBLE CONVERSION ARCHITECTURE
- AM/FM STATION DETECTOR AND DIGITAL IF-COUNTER
- SINGLE FREQUENCY REFERENCE FOR BOTH AM AND FM
- FULL ELECTRICAL ADJUSTMENT
- I^2C-BUS PROGRAMMABLE



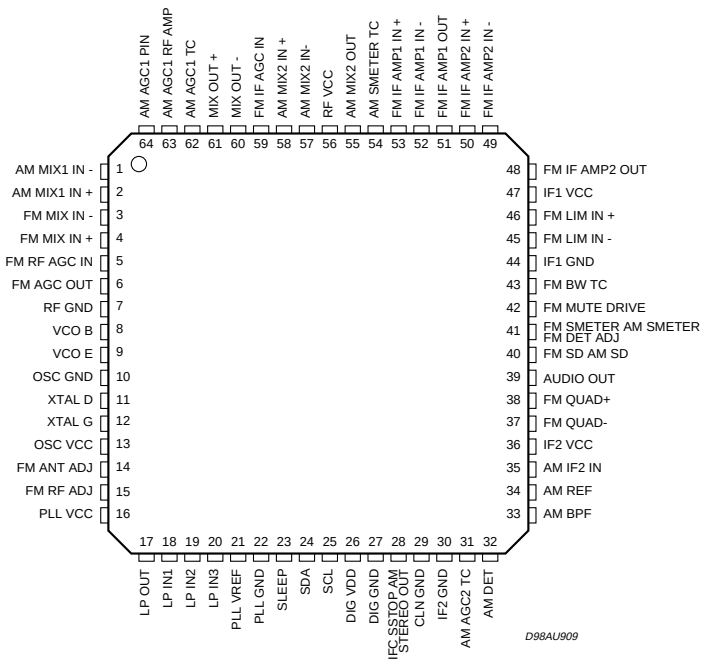
TQFP64

ORDERING NUMBER: TDA7421N

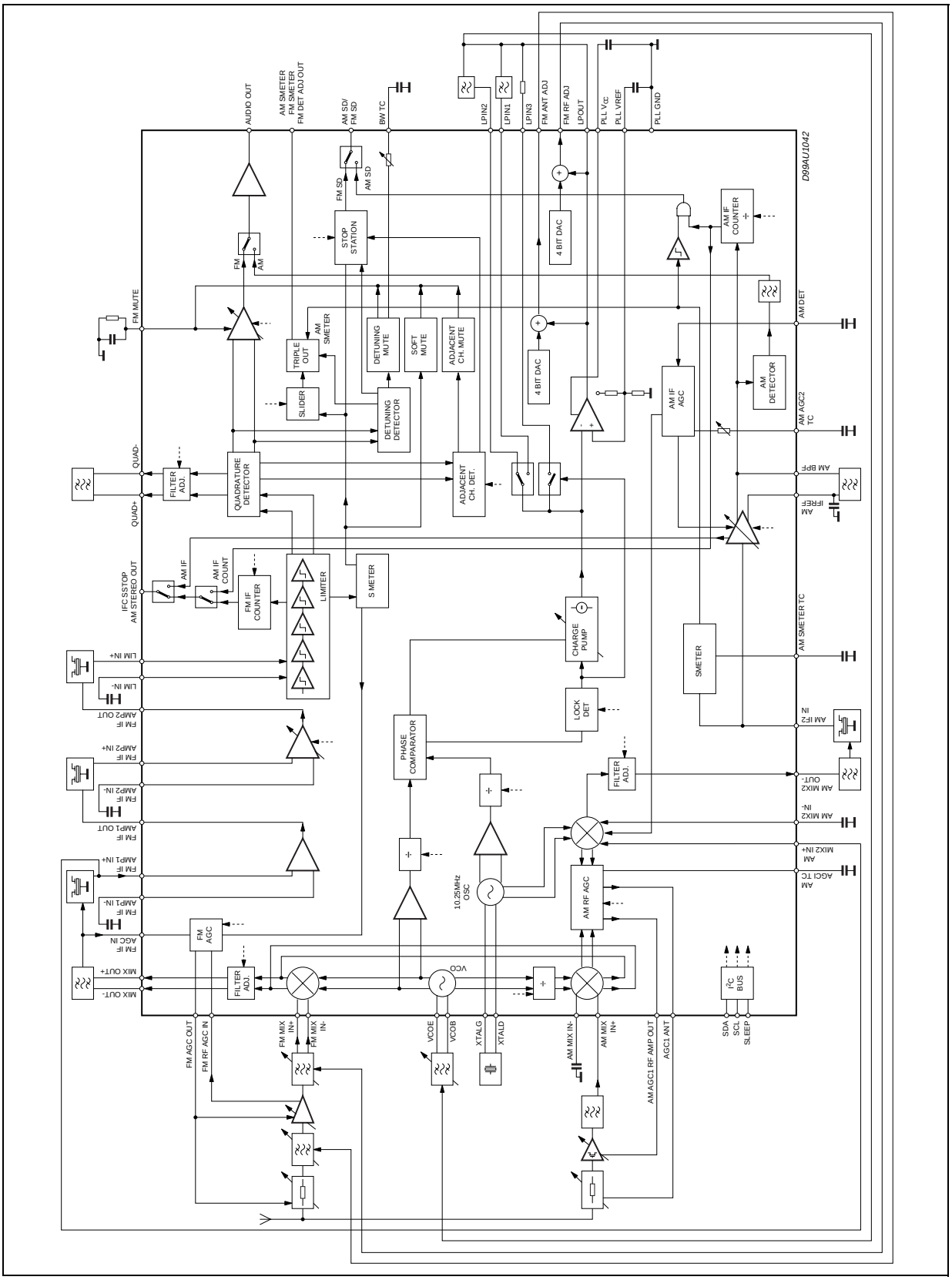
DESCRIPTION

The TDA7421N is a high-performance tuner circuit which integrates AM and FM sections, PLL frequency sinthesizer and IF counter on a single chip.
Use of BICMOS technology allows the implementation of tuning functions with a minimum of external components.Value spread of external components can be fully compensated by means of on-chip electrical adjustment controlled by external µP.
The FM quality detection circuit, in conjunction with the digital IF counter, enables the stop-station function in “seek” mode and MPX mute during reception. The combination of programmable level detector and IF counter allows reliable AM stop-station performance.
The Automatic Gain Control (AGC) operates on different signal bandwidths in order to optimize sensitivity and dynamic range.
I^2C-bus controls functions such as AGC, amplifier gains, PLL and counter settings.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{amb}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C
V_{CC}	Analog Supply Voltages (PLL, RF, IF1, IF2, OSC)	10.2	V
V_{DD}	Digital Supply Voltage	5.5	V

THERMAL DATA

Symbol	Parameter	Typ. Value	Unit
$R_{th\ j\text{-}amb,\ fa}$	Thermal Resistance Junction-Ambient, Free Air	68	°C/W
$R_{th\ j\text{-}amb,\ sol}$	Thermal Resistance Junction-Ambient, Soldered	55	°C/W

PIN DESCRIPTION

N.	Name	Function
1	AM MIX1 IN -	AM 1st mixer negative input (differential -)
2	AM MIX1 IN +	AM 1st mixer positive input (differential +)
3	FM MIX1 IN -	FM mixer negative input (differential -)
4	FM MIX1 IN +	FM mixer positive input (differential +)
5	FM RF AGC IN	RF AGC input
6	FM AGC OUT	FM AGC output voltage
7	RF GND	RF ground
8	VCO B	Local oscillator input to the transistor base
9	VCO E	Local oscillator input to the transistor emitter
10	OSC GND	Oscillator ground
11	XTAL D	Crystal oscillator MOS amplifier output
12	XTAL G	Crystal oscillator MOS amplifier input
13	OSC VCC	Oscillator positive supply
14	FM ANT ADJ	Tuning varicap voltage for antenna FM filter
15	FM RF ADJ	Tuning varicap voltage for RF FM filter
16	PLL VCC	PLL positive supply
17	LP OUT	Op Amp output to PLL loop filters
18	LP IN1	FM loop filter connection to op-amp inverting input
19	LP IN2	AM loop filter connection to op-amp inverting input

PIN DESCRIPTION (Continued)

N.	Name	Function
20	LP IN3	FM-HS loop filter connection to op-amp inverting input
21	PLL VREF	Voltage reference to Op Amp noninverting input
22	PLL GND	PLL ground
23	SLEEP	I^2C bus disconnect signal
24	SDA	I^2C bus data
25	SCL	I^2C bus clock
26	DIG VDD	Digital positive supply
27	DIG GND	Digital ground
28 (*)	IFC SSTOP AM STEREO OUT	IF-Counter stop signal or AM IF2 amplifier output
29	CLN GND	“Clean” ground
30	IF2 GND	IF2 ground
31	AM AGC2 TC	AM 2^{nd} AGC time constant
32	AM DET	AM detector capacitor
33	AM BPF	AM IF filter
34	AM REF	Reference voltage of AM IF amplifier
35	AM IF2 in	AM IF2 amplifier input
36	IF2 VCC	IF2 positive supply
37	FM QUAD -	FM quadrature detector tank (differential -)
38	FM QUAD +	FM quadrature detector tank (differential +)
39	AUDIO OUT	FM MPX/AM Audio output
40 (*)	FM SD AM SD	FM station detector output or AM station detector output
41 (*)	FM SMETER AM SMETER FM DET ADJ	FM S-meter output or AM S-meter output or FM detector adjustment output
42	FM MUTE DRIVE	FM mute time constant
43	FM BW TC	FM detuning detector time constant
44	IF1 GND	IF1 ground
45	FM LIM IN -	FM limiter negative input (differential -)
46	FM LIM IN +	FM limiter negative input (differential +)
47	IF1 VCC	IF1 positive supply
48	FM IF AMP2 OUT	FM 2^{nd} IF amplifier output

PIN DESCRIPTION (Continued)

N.	Name	Function
49	FM IF AMP2 IN -	FM 2nd IF amplifier negative input (differential -)
50	FM IF AMP2 IN +	FM 2nd IF amplifier positive input (differential +)
51	FM IF AMP1 OUT	FM 1st IF amplifier output
52	FM IF AMP IN -	FM 1st IF amplifier negative input (differential -)
53	FM IF AMP IN +	FM 1st IF amplifier positive input (differential +)
54	AM S-METER TC	AM S-meter time constant
55	AM MIX2 OUT	AM 2nd mixer output
56	RF VCC	RF positive supply
57	AM MIX2 IN -	AM 2nd mixer negative input (differential -)
58	AM MIX2 IN +	AM 2nd mixer positive input (differential +)
59	FM IF AGC IN	FM IF AGC input
60	MIX OUT -	FM/AM 1st mixer negative output (differential -)
61	MIX OUT +	FM/AM 1st mixer positive output (differential +)
62	AM AGC1 TC	AM 1st AGC time constant
63	AM AGC1 RF AMP	AM 1st AGC voltage output (to RF amplifier)
64	AM AGC1 PIN	AM 1st AGC current output (to antenna attenuation diodes)

(*) Pin function is user defined by software.

FM SECTION GLOBAL PERFORMANCES

Refer to Evaluation Circuit

– Input 98.1MHz, 40KHz dev., 1KHz mod., 60dBµV antenna level, mono.

– MPX Output, de-enphasis 50µs, BPF 200Hz-15KHz.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
FM I_{CC}	Total Supply Current Including Mixer			90		mA
S+N/N	Signal to Noise Ratio			66		dB
THD	Total Harmonic Distortion			0.3		%
$V_{O\ AF}$	Audio Output Level	75kHz Deviation		400		mV_{RMS}
US_1	Usable Sensitivity (40dB)	antenna level at which S+N/N = 40dB		0		dBµV
US_2	Usable Sensitivity (26dB)	antenna level at which S+N/N = 26dB		-6		dBµV
AGC_{SP}	AGC Starting point			55		dBµV

AM SECTION GLOBAL PERFORMANCES

Refer to Evaluation Circuit

- Input: fc = 999KHz, f mod = 400Hz, m = 30%, 74dBμV_{emf} antenna level unless otherwise specified.
- Audio Output + RC BPF (BPF 20Hz - 20KHz)

ΔMI_{CC}	Total supply current including mixers			80		mA
$V_{IN\ MIN}$	Maximum Sensitivity	ΔV_{AF} = - 20dB		13		dBµV (emf)
$V_{IN\ US}$	Usable Sensitivity	S+N/N = 20dB		27		dBµV (emf)
ΔV_{is}	AGC Range	ΔV_{AF} = -10dB		50		dB
S+N/N	Signal to Noise Ratio	V_{INRF} = 74dBu		54		dB
α_{IMAG}	Image Rejection	f_{im} = 22.399MHz, antenna level @ $V_{\Delta F}$ = -10dB				dB
α_{Tw}	Tweet, Δ(S+N/N)	f1 = 900KHz;f2 = 1350KHz		1.2		dB
THD	Total Harmonic Distortion			0.3		%
		m = 80%		1		%
		V_{INRF} = 120dBμV_{emf}		0.3		%
V_{AF}	Audio Output Level			107		mV_{RMS}
V_{AMST}	AM IF2 Output level			105		dBµV

ELECTRICAL CHARACTERISTICS

DC PARAMETERS (T_{amb} = 25°C; V_{CC} = 8V, V_{dd} = 5V, no RF input unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PLL V_{CC}	PLL Supply Voltage		7.5		10	V
PLL I_{CC}	PLL Supply Current	AM MODE		1.6		mA
		FM MODE		3.0		mA
		STBY MODE				mA
DIG V_{dd}	Digital Supply Voltage		4.75		5.25	V
DIG I_{dd}	Digital Supply Current	AM MODE		4.6		mA
		FM MODE		4.0		mA
		STBY MODE				mA
RF V_{CC}	RFSupply Voltage		7.5		10	V
RF I_{CC}	RF Supply Current	AM MODE		27.0		mA
		FM MODE		13.0		mA
		STBY MODE				
IF1 V_{CC}	IF1 Supply Voltage		7.5		10	V
IF1 I_{CC}	IF1 Supply Current	AM MODE		4.0		mA
		FM MODE		22.0		mA
		STBY MODE				mA
IF2 V_{CC}	IF2 Supply Voltage		7.5		10	V
IF2 I_{CC}	IF2 Supply Current	AM MODE		10.0		mA
		FM MODE		28.0		mA
		STBY MODE				mA
OSC V_{CC}	Oscillator Supply Voltage		7.5		10	V
OSC I_{CC}	Oscillator Supply Current	AM MODE		17.0		mA
		FM MODE		81.0		mA
		STBY MODE				mA

Voltage Controlled Oscillator (VCO)
Ref: FM Test Circuit, measure Vosc with high impedance FET probe

f_{VCOmin}	Minimum VCO Frequency	V_{tun} = 0 Europe/USA Japan		80.9 55	98.2 65.4	MHz
f_{VCOmax}	Maximum VCO Frequency	V_{tun} = V_{CC} Europe/USA Japan	123.2 79.2	128 90		MHz

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OSC}	Oscillator Amplitude	f_{OSC} = 108.8MHz, Europe/USA f_{OSC} = 72.3MHz Japan		110		dBµV
C/N	Carrier to Noise	1KHz offset		85		dBc/Hz

Reference Oscillator
Ref: AM Test Circuit, measureV_{XTAL} with high impedance FET probe

f_{XTAL}	Reference Frequency			10.25		MHz
V_{XTAL}	Oscillator Amplitude			108		dBµV

FM Front-end Electrical Adjustments
Ref: FM Test Circuit, measure V_{ANTADJ} and V_{RFADJ} referred to V_{PLLOUT}

ANTADJ MAX OFF	Maximum FM Antenna Filter Adjustment Voltage Offset	V_{PLLOUT} = 2.5V, ANA3-0 set to 1111	21	25	27	%
ANTADJ STEP OFF	FM Antenna Filter Adjustment Voltage Offset Step	V_{PLLOUT} = 2.5V, ANA3-0 set to 1001	2.8	3.6	4.4	%
RFADJ MAX OFF	Maximum FM RF Filter Adjustment Voltage Offset	VP_{LLOUT} = 2.5V, RFA3-0 set to 1111	21	25	27	%
RFADJ STEP OFF	FM RF Filter Adjustment Voltage Offset Step	V_{PLLOUT} = 2.5V, RFA3-0 set to 1001	2.8	3.6	4.4	%

FM Mixer
Ref: FM Test Circuit, measure input at $V_{MIXFMIN}$, output at V_{MIXOUT}

$R_{IN,MIX}$	Single-ended input resistance (pin 3, pin4)			12		Ω
G_{MIX}	Conversion Gain	f_{IN} = 98.1MHz		21.8		dB
$IP3_{MIX}$	3rd order intermodulation distortion intercept point	f_d = 98.1MHz; f_{u1} = 98.2MHz; f_{u2} = 98.3MHz;		108		dBµV
$CP1_{MIX}$	1dB compression point	f_{IN} = 98.1MHz		90		dBµV
CAdj1	Value of the minimum adjusting capacitance step	T1A3-0 set to 1000		0.38		pF

FM AGC
Ref: FM Test Circuit, measure input at $V_{FMRFAGCIN}$ and $V_{FMIFAGCIN}$, output at $V_{FMAGCOUT}$

$V_{RFAGCSTART}$	Open Loop RF AGC Starting Point	$f_{RFAGCIN}$ = 98.1MHz Value of $V_{FMRFAGCIN}$ at which $V_{FMAGCOUT}$ = 4V		80		dBµV
$R_{IN,RFAGC}$	Input Resistance			20		KΩ
$V_{IFAGCTART}$	Open Loop IF AGC Starting Point	$f_{IFAGCIN}$ = 10.7MHz Value of $V_{FMIFAGCIN}$ at which $V_{FMAGCOUT}$ = 4V FAGC2-0 set to 111		77		dBµV
$R_{IN,IFAGC}$	Input Resistance			20		KΩ
$R_{OUT,FMAGC}$	Output Resistance			10		KΩ

ELECTRICAL CHARACTERISTICS (Continued)

FM IF Amplifier 1
Ref: FM Test Circuit, measure input at $V_{FMAMP1IN}$, output at $V_{FMAMP1OUT}$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{IN,AMP1}$	Input Resistance			330		Ω
$R_{OUT,AMP1}$	Output Resistance			330		Ω
G_{AMP1}	Typical Gain	f_{IN} = 10.7MHz		18.5		dB
$IP3_{AMP1}$	3rd Order Intermodulation Distortion Intercept Point	f_d = 10.7MHz; f_{u1}= 10.8MHz; f_{u2}= 10.9MHz; FBH3-0 set to 0100				dBµV
$CP1_{AMP1}$	1dB Compression Point	f_{IN} = 10.7MHz; FBH3-0 set to 0100				dBµV

FM IF Amplifier 2
Ref: FM Test Circuit, measure input at $V_{FMAMP2IN}$, output at $V_{FMAMP2OUT}$

$R_{IN,AMP2}$	Input Resistance	f = 10.7MHz		330		Ω
$R_{OUT,AMP2}$	Output Resistance	f = 10.7MHz		330		Ω
$G_{MIN,AMP2}$	Minimum Gain	f_{IN} = 10.7MHz, FBL1-0 set to 01		6		dB
$G_{MAX,AMP2}$	Maximum Gain	f_{IN} = 10.7MHz, FBL1-0 set to 00		10		dB
$IP3_{AMP2}$	3rd Order Intermodulation Distortion Intercept Point	f_d = 10.7MHz; f_{u1}= 10.8MHz; f_{u2}= 10.9MHz; FBL3-0 set to 0100				dBµV
$CP1_{AMP2}$	1dB Compression Point	f_{IN} = 10.7MHz; FBL3-0 set to 0100				dBµV

FM Limiter, Field Strengh Meter and Demodulator
Ref: FM Test circuit, measure:
- Input at $V_{FMLIMIN}$, f_{IN} = 10.7MHz
- FS Meter output at $V_{FMSMETER}$ (FMADJ set to 0, FSL4-0 set to 00000)
- demodulator adjustment output at $V_{FSMETER}$ (FMADJ set to 1)

$R_{IN,LIM}$	Limiter Input Resistance			330		Ω
G_{LIM}	Limiter Gain			90		dB
LS	Limiting Sensitivity			23		dBµv
SM1	Smeter 1	$V_{FMLIMIN}$ = 40dBµV		1.1		V
SM2	Smeter 2	$V_{FMLIMIN}$ = 60dBµV		2.3		V
SM3	Smeter 3	$V_{FMLIMIN}$ = 80dBµV		3.7		V
SM4	Smeter 4	$V_{FMLIMIN}$ = 100dBµV		4.9		V
$SM_{MINSHIFT}$	Smeter Minimum Shift Voltage	$V_{FMLIMIN}$ = 70dBµV; FSL4-0 set to 00000		0.0		V
$SM_{MAXSHIFT}$	Smeter Maximum Shift Voltage	$V_{FMLIMIN}$ = 70dBµV; FSL4-0 set to 11111		1.5		V

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{DEM}	Demodulator Conversion Gain	$V_{FMLIMIN}$ > LS		2		mV_{RMS}/ KHz
G_{DEMADJ}	Demodulator Adjustment Conversion Gain	$V_{FMLIMIN}$ > LS		14		mV_{RMS}/ KHz
CAdjDem	Value of the minimum adjusting capacitance step	DEM6-0 set to 0000001		50		fF

FM Audio Amplifier

Ref: FM Test circuit, $V_{FMLIMIN}$, = 95dBµV, f_{IN} = 10.7MHz; measure:
- MPX output at V_{AUDIO}, BPF 200Hz to 15KHz, 50µs de-emphasis.
- muting voltage at $V_{MUTE, DRIVE}$

V_{MUTE}	Mute Voltage	$V_{MUTE,DRIVE}$ for which ΔV_{AF} = -11.5dB; AUM1-0 set to 11	2			V
V_{PLAY}	Play Voltage	$V_{MUTE,DRIVE}$ for which ΔV_{AF} = -1dB, AUM1-0 set to 11			0.3	V
$G_{AMP,PLAY}$	Audio Amplifier Gain in Play Conditions	$V_{MUTE,DRIVE}$ < V_{PLAY}		9		dB
$MUTEATT_{MIN}$	Minimum Mute Attenuation	$V_{MUTE,DRIVE}$ > V_{MUTE}; AUM1-0 set to 00		-5		dB
$MUTEATT_{MAX}$	Maximum Mute Attenuation	$V_{MUTE,DRIVE}$ > V_{MUTE}; AUM1-0 set to 11		-12.5		dB
V_{AF}	AF Output Level	f_{DEV} = 75KHz, F_{MOD} = 1KHz, $V_{MUTE,DRIVE}$ < V_{MUTE}		400		mV_{RMS}
THD	AF Total Harmonic distortion	f_{DEV} = 40KHz, FMOD = 1KHz, $V_{MUTE,DRIVE}$ < V_{MUTE}		0.3		%
S+N/N	AF Signal to Noise Ratio	f_{DEV} = 40KHz, F_{MOD} = 1KHz, $V_{MUTE,DRIVE}$ < V_{MUTE}		80		dB
AMR	Amplitude Modulation Rejection	AM modulation depht 30%, f_{MOD} = 1KHz, with respect to FM modulated signal with f_{DEV} = 40KHz, $V_{MUTE,DRIVE}$ < V_{MUTE}		67		dB
$AUDIO_{curr}$	Output Current Capability		5			mA
MUTE R_{out}	Mute Drive Output Resistance			1		KΩ

FM QUALITY DETECTORS

Field Strength Detector

Ref: FM Test Circuit, HDDIS and BWDIS set to 1, measure:
- Input at $V_{FMLIMIN}$, f_{IN} = 10.7MHz, CW
- output at $V_{MUTE,DRIVE}$

FSD_{MIN}	Field Strength Detector Minimum Threshold	$V_{FMLIMIN}$ level at which $V_{MUTE,DRIVE}$ = V_{MUTE}, FSM3-0 set to 0000				dBµV

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
FSD_{MAX}	Field Strength Detector Maximum Threshold	$V_{FMLIMIN}$ level at which $V_{MUTE,DRIVE} = V_{MUTE}$, FSM3-0 set to 1111		67.5		dBµV

Detuning Detector
Ref: FM Test Circuit; HDDIS and SMDIS set to 1, measure:
- Input at $V_{FMLIMIN}$, CW
- output at $V_{MUTE,DRIVE}$

DD_{START}	Detuning Detector Starting Point	frequency shift from 10.7MHz at which $V_{MUTE,DRIVE} = V_{PLAY}$		±23		KHz
$DD_{SLOPE,MIN}$	Detuning Detector Minimum Muting Slope	frequency shift from 10.7MHz + DD_{START} at which $V_{MUTE,DRIVE} = V_{MUTE}$, BWM2-0 set to 100, SEEK set to 0		30		KHz
$DD_{SLOPE,MAX}$	Detuning Detector Maximum Muting Slope	frequency shift from 10.7MHz + DD_{START} at which $V_{MUTE,DRIVE} = V_{MUTE}$, BWM2-0 set to 001, SEEK set to 0		10		KHz
DD_{TRC}	Detuning Detector Time Constant Ratio	ratio of "reception" mode integration time constant inside the Detuning Detector with respect to "seek" mode		34/6		s/s

Adjacent Channel Detector
Ref: FM Test Circuit; BWDIS and SMDIS set to 1, measure:
- Input at $V_{FMLIMIN}$: desired 10.7MHz, 95dBµV CW; undesired 10.8MHz CW
- output at $V_{MUTE,DRIVE}$

ACD_{MAX}	Adjacent Channel Quality Detector Maximum Sensitivity Threshold	amplitude of undesired signal at which $V_{MUTE,DRIVE} = V_{MUTE}$, HDM4-0 set to 11111		91		dBu
ACD_{MIN}	Adjacent Channel Quality Detector Minimum Sensitivity Threshold	amplitude of undesired signal at which $V_{MUTE,DRIVE} = V_{PLAY}$, HDM4-0 set to 00000		94.8		dBu

Field Strength Station Detector
Ref: FM Test Circuit; SEEK set to 1, HDDIS and BWDIS set to 1, measure:
- Input at $V_{FMLIMIN}$: desired 10.7MHz, CW
- output at V_{FMSD}

$FSSD_{MIN}$	Field Strength Station Detector Minimum Threshold	$V_{FMLIMIN}$ level at which V_{FMSD} = 2.5V; FSS4-0 set to 00000				dBµV
$FSSD_{MAX}$	Field Strength Station Detector Maximum Threshold	$V_{FMLIMIN}$ level at which V_{FMSD} = 2.5V; FSS4-0 set to 11111				dBµV

ELECTRICAL CHARACTERISTICS (Continued)

Detuning Station Detector
Ref: FM Test Circuit; SEEK set to 1, HDDIS and SMDIS set to 1, measure:
- Input at $V_{FMLIMIN}$, CW;
- output at V_{FMSD}

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DSD	Detuning Station Detector Threshold	frequency shift from 10.7MHz at which V_{FMSD} = 2.5V		±28		KHz

Adjacent Channel Station Detector
Ref: FM Test Circuit; SEEK set to 1, HDDIS and SMDIS set to 1, measure:
- Input at $V_{FMLIMIN}$: desired 10.7MHz, 95dBµV CW; undesired 10.8MHz CW
- output at V_{FMSD}

$ACSD_{MAX}$	Adjacent Channel Detector Maximum Sensitivity Threshold	amplitude of undesired signal at which V_{FMSD} = 2.5V, HDM4-0 set to 11111		92.5		dBµV
$ACSD_{MIN}$	Adjacent Channel Detector Minimum Sensitivity Threshold	amplitude of undesired signal at which V_{FMSD} = 2.5V, HDM4-0 set to 00000		94.9		dBµV

AM Mixer 1
Ref: AM Test Circuit, measure input at $V_{MIX1AMIN}$, output at V_{MIXOUT}

$R_{IN,MIX1}$	Input Resistance			1.2		KΩ
G_{MIX1}	Conversion Gain	f_{IN} = 1MHz		7.6		dB
$IP3_{MIX1}$	3rd Order Intermodulation Distortion Intercept Point	f_d = 1MHz; f_{u1} = 1.1MHz; f_{u2} = 1.2MHz		131		dBµV
$CP1_{MIX1}$	1dB Compression Point	f_{IN} = 1MHz		110		dBµV
CAdj1	Value of the minimum adjusting capacitance step	T1A3-0 set to 1000		0.38		pF

AM Wide & Narrow AGC
Ref: AM Test Circuit; measure input at $V_{MIX1AMIN}$ and $V_{MIX2AMIN}$, output at $V_{AMAGC1AMP}$ and $V_{AMAGC1PIN}$

$V_{WAGCMIN}$	Open Loop WIDE AGC Minimum Starting Point	f_{WAGCIN} = 999kHz, AAGW1-0 set to 11; $V_{MIX1AMIN}$ at which $V_{AMAGC1AMP}$ = 2.5V		95		dBµV
$V_{WAGCMAX}$	Open Loop WIDE AGC Maximum Starting Point	f_{WAGCIN} = 999kHz, AAGW1-0 set to 00; $V_{MIX1AMIN}$ at which $V_{AMAGC1AMP}$ = 2.5V		101		dBµV
$V_{NAGCMIN}$	Open Loop NARROW AGC Minimum Starting Point	f_{NAGCIN} = 10.7MHz, AAGN1-0 set to 11; $V_{MIX2AMIN}$ at which $V_{AMAGC1AMP}$ = 2.5V		81		dBµV
$V_{NAGCMAX}$	Open Loop NARROW AGC Maximum Starting Point	f_{NAGCIN} = 10.7MHz, AAGN3-0 set to 00; $V_{MIX2AMIN}$ at which $V_{AMAGC1AMP}$ = 2.5V		87		dBµV
$R_{OUTAMAGC1}$	Output Resistance			23.3		KΩ
$I_{AMAGC1PIN}$	Maximum Antenna Attenuation Diode Current	f_{WAGCIN} = 999kHz; $V_{MIX1AMIN}$ = 120dBµV; AAGW1-0 set to 00		1.4		mA

ELECTRICAL CHARACTERISTICS (Continued)

AM Mixer 2

Ref: AM Test Circuit; measure input at $V_{MIX2AMIN}$, output at $V_{MIX2OUT}$ (switches must be in position 2 for AGC measurements).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{IN,MIX2}$	Input Resistance			5		KΩ
G_{MIX2}	Maximum conversion Gain	f_{IN} = 10.7MHz		25		dB
$IP3_{MIX2}$	3rd Order Intermodulation Distortion Intercept Point	f_d = 10.7MHz; f_{u1} = 10.8MHz; f_{u2} = 10.9MHz		117		dBµV
$CP1_{MIX2}$	1dB Compression Point	f_{IN} = 10.7MHz		107		dBµV
CAdj2	Value of the minimum adjusting capacitance step	T2A3-0 set to 0001		1.57		pF
AGC_{MIXSP}	AGC2 Starting Point on Mixer 2	f_{IN} = 10.7MHz; Value of $V_{MIX2AMIN}$ for which $V_{MIX2OUT}$ is 1dB compressed; IF2A1-0 set to 10		48		dBµV
AGC_{MIXIS}	AGC2 intervention slope on Mixer 2	f_{IN} = 10.7MHz:$\Delta V_{MIX2OUT}$ for $\Delta V_{MIX2AMIN}$ = 1dB; IF2A1-0 set to 10		0.1		dB/dB
AGC_{MIXR}	AGC2 Range on Mixer 2	f_{IN} = 10.7MHz; Range of $V_{MIX2AMIN}$ above AGC_{MIXSP} for which $V_{MIX2OUT}$ is not increasing linearly with a 1dB/dB slope; IF2A1-0 set to 10	50			dB

AM IF2 Amplifier

Ref: AM Test Circuit; f_{IN} = 450KHz, measure input at $V_{IF2AMPIN}$, output at $V_{IF2AMPOUT}$ (switches must be in position 1).

$R_{IN,IF2AMP}$	Input Resistance			2		KΩ
$G_{IF2AMPMIN}$	Minimum Gain	$V_{IF2AMPIN}$ = 10dBµV; IF2A1-0 set to 00		50		dB
$G_{IF2AMPMAX}$	Maximum Gain	$V_{IF2AMPIN}$ = 10dBµV; IF2A1-0 set to 11		59		dB
AGC_{AMPSP}	AGC2 Starting Point on IF2 Amp	Value of $V_{IF2AMPIN}$ for which $V_{IF2AMPOUT}$ is 1dB compressed, IF2A1-0 set to 01		60		dBµV
AGC_{AMPR}	AGC2 Range on IF2 Amp	f_{IN} = 10.7MHzRange of $V_{IF2AMPIN}$ above AGC_{AMPSP} for which $V_{IF2AMPOUT}$ is not increasing linearly with a 1dB/dB slope; IF2A1-0 set to 01		33		dB
AGC_{AMPIS}	AGC2 intervention slope on IF2 Amp	f_{IN} = 10.7MHz; $\Delta V_{IF2AMPOUT}$ for $\Delta V_{IF2AMPIN}$ = 1dB; IF2A1-0 set to 1		0.1		dB/dB
AGC_{TCR}	AGC2 Time Constant Ratio	Ratio of AGC2 "reception" Time Constant and "seek" Time Constant		150/5		s/s

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IF_{AMST}	AM IF2 Output Level at pin 28	$VI_{F2AMPIN}$ = 72dBmV; AMSTEREO set to 1		106		dBµV
$IF_{AMSTcurr}$	Current Capability of pin 28	AMSTEREO set to 1		150		µA

AM Field Strength Meter and Field Strength Station Detector
Ref: AM Test Circuit; f_{IN} = 10.7MHz, measure input at $V_{MIX2AMIN}$, outputs at $V_{AMSMETER}$ and at V_{AMSD} (switches in position 2).

AMSM1	AM Smeter 1 at $V_{AMSMETER}$	$V_{MIX2AMIN}$ = 40dBµV		1.4		V
AMSM2	AM Smeter 2 at $V_{AMSMETER}$	$V_{MIX2AMIN}$ = 60dBµV		3.4		V
AMSM3	AM Smeter 3 at $V_{AMSMETER}$	$V_{MIX2AMIN}$ = 80dBµV		4.8		V
$AMSD_{MIN}$	Station Detector Minimum Threshold	$V_{MIX2AMIN}$ at which V_{AMSD} = 2.5V; ASS3-0 set to 0000, SEEK set to 1		27		dBµV
$AMSD_{MAX}$	Station Detector Maximum Threshold	$V_{MIX2AMIN}$ at which V_{AMSD} = 2.5V; ASS3-0 set to 1111, SEEK set to 1				dBµV

IF Counter Output
Ref: AM & FM Test Circuit, measure at pin 28

IFC_{FM}	FM IFC Sensitivity	$V_{FMLIMIN}$ at which Vpin 28 = 2.5V, SEEK set to 1, EW2-0 set to 101, IFS2-0 set to 010		34		dBµV
IFC_{AM}	AM IFC Sensitivity	$V_{IF2AMPIN}$ at which Vpin 28 = 2.5V, SEEK set to 1, EW2-0 set to 011, IF2-0 set to 100, AMFM STBY1-0 set to 10		29		dBµV
$IFC_{current}$	IFC Current Capability			150		µA

SD output Impedance
Measure output at V_{FMSD}

$SD_{IMP,ON}$	SD output impedance	SDDIS set to 0			700	Ω
$SD_{IMP,TS}$	SD output impedance (Tri-State)	SDDIS set to 1	7			MΩ

Loop Filter Input/Output
(LP_IN1, LP_IN2, LP_IN3, LP_OUT)

$-I_{IN}$	Input Leakage Current	V_{IN} = GND; PD_{out} = Tristate	-2	0	2	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD}; PD_{out} = Tristate	-2	0	2	µA
V_{OL}	Output Voltage Low	I_{IN} = -0.2mA; V_{CC} = 8.5V			0.5	V
V_{OH}	Output Voltage High	I_{OUT} = 0.2mA; V_{CC} = 8.5V	8			V
I_{OUT}	Output Current Sink	V_{PLL} = 8.5V;	10			mA
I_{OUT}	Output Current Source	V_{out} = 0.5 to 8V	10			mA

ELECTRICAL CHARACTERISTICS (Continued)

I^2C Bus Interface

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency			100	500	KHz
t_{AA}	SCL Low to SDA Data Valid			300		ns
t_{buf}	Time the Bus Must Be Free for the New Transmission			4.7		µs
t_{HD-STA}	START Condition hold Time			4.0		µs
t_{LOW}	Clock Low Period			4.7		µs
t_{HIGH}	Clock High Period			4.0		µs
t_{SU-SDA}	Start Condition Setup Time			4.7		µs
t_{HD-DAT}	Data Input Hold Time			0		µs
t_{SU-DAT}	Date Input Setup Time			250		ns
t_R	SDA & SCL Rise Time					µs
t_F	SDA & SCL Full Time					µs
t_{SU-STO}	Stop Condition Setup Time			4.7		µs
t_{DH}	DATA OUT Time			300		ns
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V

Figure 1. AM Test Circuit

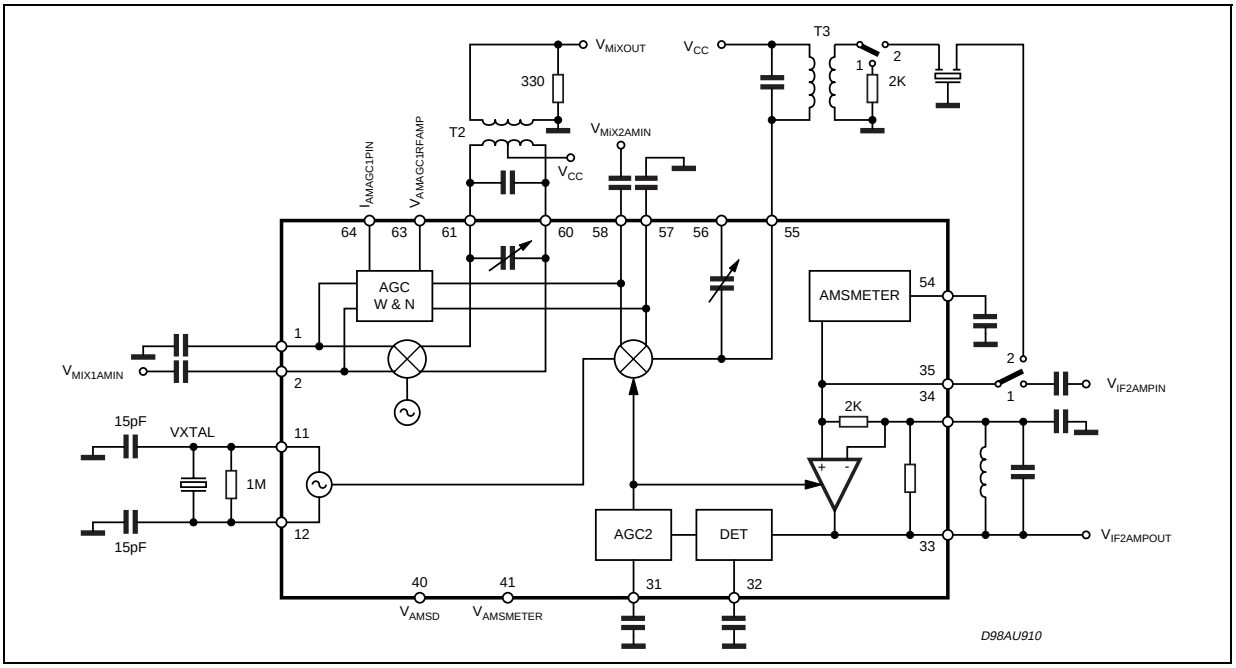
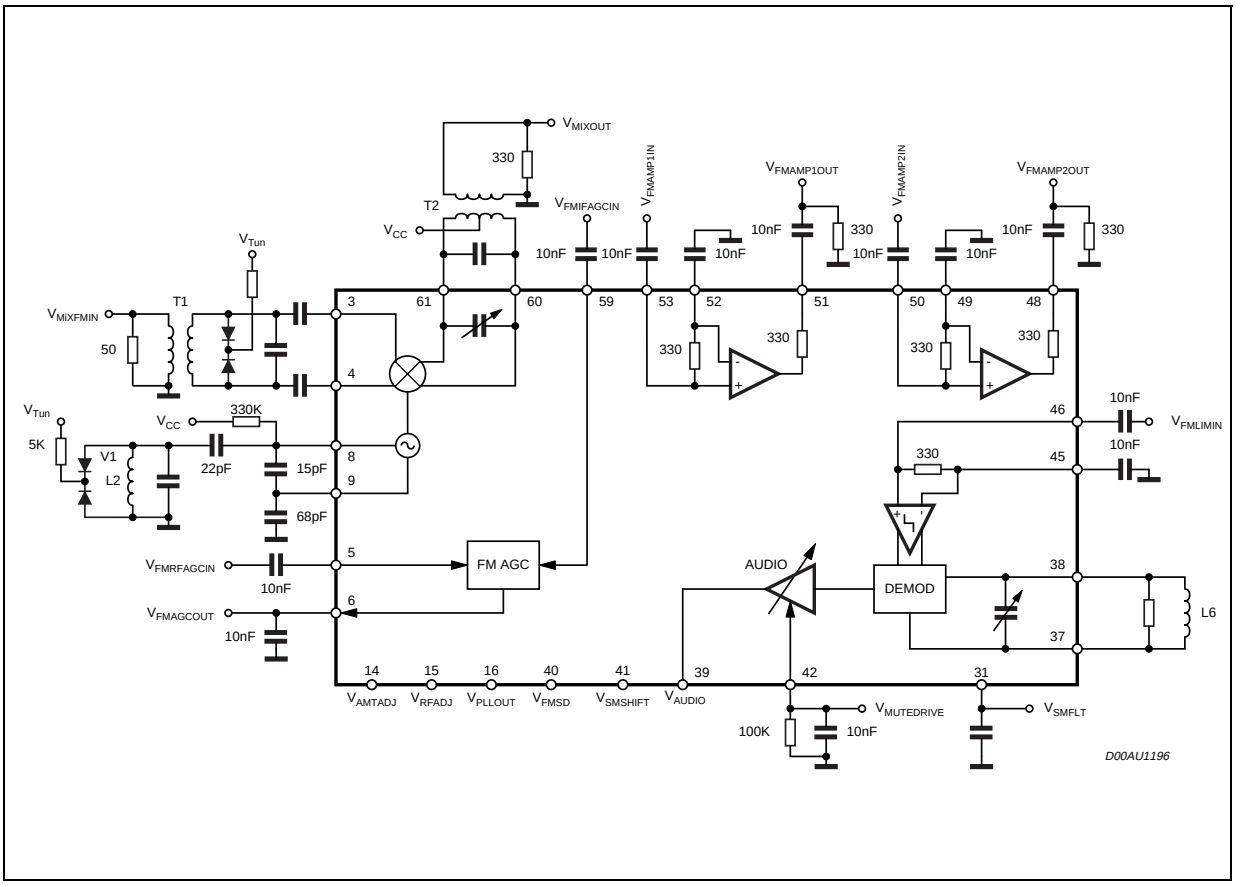


Figure 2. FM Test Circuit



1.0 FM SECTION

Featuring a single conversion configuration, it comprises a multi-stage IF limiter whose gain is I^2C controlled and a quadrature demodulator with detuning and adjacent channel detectors. Signal meter and stop station functions are also supported

2.0 AM SECTION

AM signal is converted by means of UP-DOWN configuration (IF1 = 10.7MHz, IF2 = 450KHz) and MW/LW bands are covered.

3.0 PLL SECTION

Three operating modes are available:

PM0	PM1	Operating Mode
0	0	Standby
1	0	AM
0	1	not used
1	1	FM

They are user programmable with the mode PM registers.

3.1 Standby mode

It stops all functions. This allows low current consumption without loss of information in all registers. The pin LP-OUT is forced to 0V in power on. All data registers are set to FE (11111110). The oscillator does not run in stand-by mode.

3.2 FM and AM Operation

The FM or AM signal applies to a 32/33 prescaler, which is controlled by a 5 bit counter (A). The 5 bit register (PC0 to PC4) controls this divider.
The output of the prescaler connects to a 11 bit divider (B). The 11 bit register (PC5 to PC15) controls the divider 'B'.

3.2.1 THREE STATE PHASE COMPARATOR

The phase comparator generates a phase error signal according to phase difference between fSYN and fREF. This phase error signal drives the charge pump current generator.

3.2.2 CHARGE PUMP CURRENT GENERATOR

This stage generates signed pulses of current. The phase error signal decides the duration and polarity of those pulses.The current absolute values are programmable by A0, A1, A2 registers for high current and B0, B1 registers for low current.

3.2.3 LOW NOISE CMOS OP-AMP

An internal voltage divider at pin VREF connects the positive input of the low noise Op-Amp.The charge pump output connects the negative input. This internal amplifier in cooperation with external components can provide an active filter. The negative input is switchable to three input pins (LPIN 1, LPIN 2 and LPIN 3), to increase the flexibility in application.This feature allows two separate active filters for different applications.A logical "1" in the LPIN 1/2 register activates pin LPIN 1, otherwise pin LPIN 2 is active. While the high current mode is activated LPIN 3 is switched on.

3.2.4 INLOCK DETECTOR

The charge pump is switched in low current mode as the truth table and the related figure shows.

CURRHIGH	LOCKENA	LOCK (by inlock detector)	Charge PumpCurrent
0	X	X	low current
1	1	1	low current
1	1	0	High current
1	0	1	High current
1	0	0	High current

The charge pump is forced in low current mode when a phase difference of 10-40 usec is reached.
A phase difference larger than the programmed values will switch the charge pump immediately in the high current mode.
Few programmable delays are available for inlock detection.

4.0 IF COUNTER SYSTEM FOR AM/FM

The IF counter mode is controlled by IFCM register:

IFCM1	IFCM0	FUNCTION
0	0	NOT USED
0	1	FM MODE
1	0	AM MODE
1	1	NOT USED

A sample timer to generate the gate signal for the main counter is built with a 14 bit programmable counter to have the possibility to use any frequency. In FM mode a 6.25 KHz, in AM mode a 1KHz signal is generated. This counter is followed by an asynchronous divider to generate several sampling times.

ADDRESS ORGANIZATION (PLL and IF Counter)

		MSB							LSB
FUNCTION	**SUBAD**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
PLL CHARGE PUMP	00H	LPIN1/2	CURRH	B1	B0	A3	A2	A1	A0
LL COUNTER	01H	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
PLL COUNTER	02H	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
LL REF COUNTER	03H	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
LL REF COUNTER	04H	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8
LL LOCK DETECT	05H	LDENA	-	D3	D2	D1	D0	PM1	PM0
FC REF COUNTER	06H	IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0
FC REF COUNTER	07H	IFCM1	IFCM0	IRC13	IRC12	IRC11	IRC10	IRC9	IRC8
FC CONTROL	08H	IFENA	-	-	-	-	EW2	EW1	EW0
C CONTROL	09H	IFS2	IFS1	IFS0	CF4	CF3	CF2	CF1	CF0

4.1 Intermediate Frequency Main Counter (IFMC)

This counter is a 13-21 bit synchronous autoreload down-counter. Four bits are programmable to have the possibility for an adjust to the frequency of the IF filter.The counter length is automatically adjusted to the chosen sampling time and the counter mode. At the start the counter will be loaded with a defined value which is an equivalent to the divider value (tsample fIF).If a correct frequency is applied to the IF counter frequency inputs IF-AM and IF-FM, at the end of the sampling time the main counter is changing its state from 0 to 1FFFFFH.This is detected by a control logic. The frequency range inside which a successful count results is detected is adjustable setting bits EW 0, 1, 2.

4.2 Up-down counter filter

The information coming from the IF main counter control logic is shifted into a 5 bit up down counter circuit clocked by the sampling time signal. At the start (rising edge of the IFENA signal) the counter is set to 10H and the SSTOP signal is forced to "1".Only when the counter reaches the value 10H - step, SSTOP goes to "0".SSTOP will be "1" again, if the counter reaches the value 10h + step.

Figure 3. Charge Punp Logic

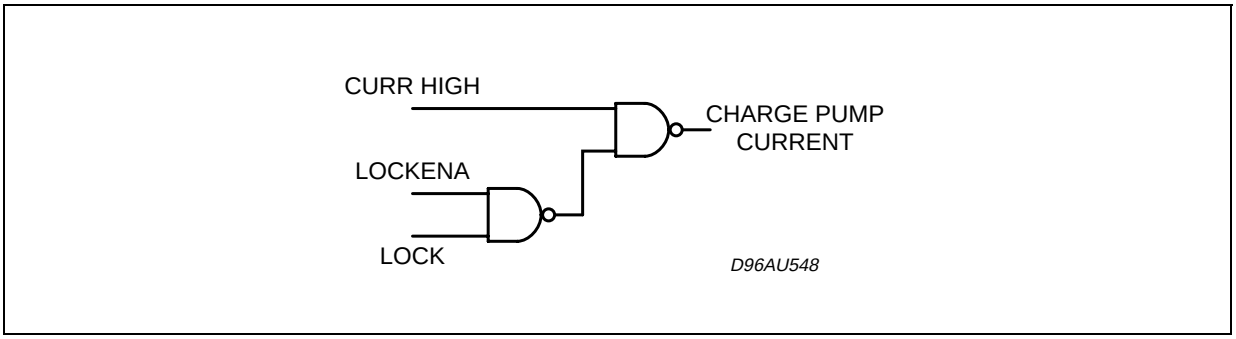
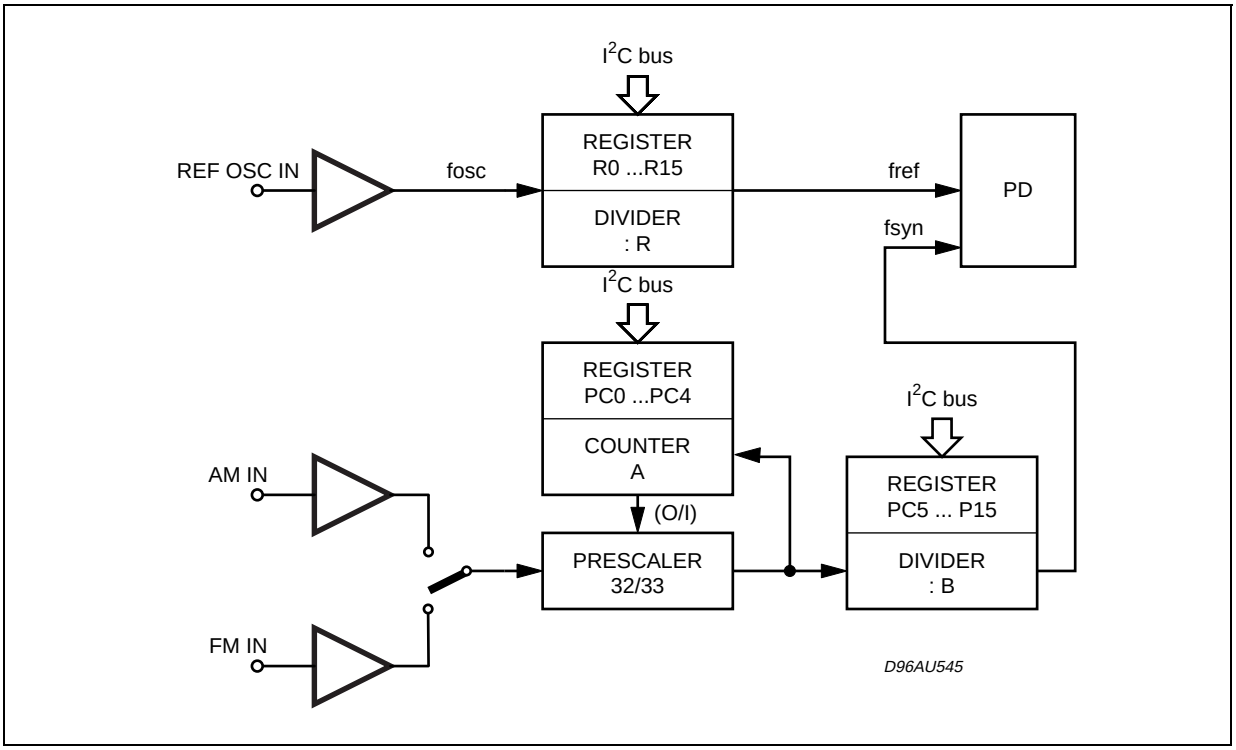
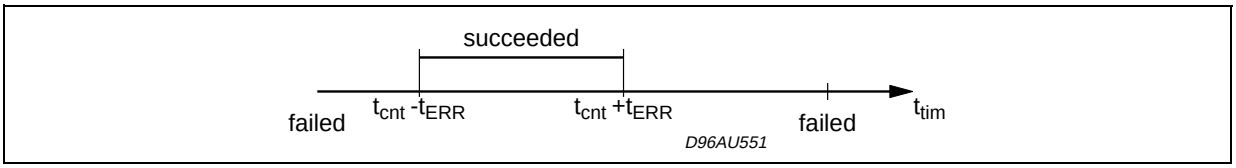


Figure 4. FM and AM operation (swallow mode)



ttim = (IFRC + 1) / fosc
tcnt = (CF + 1697) / fIF FM mode
tcnt = (CF + 44) / fIF AM mode
Counter result succeeded:
ttim > tcnt - terr and
ttim > tcnt + terr
Counter result failed:
ttim< tcnt + terr or
ttim > tcnt - terr
where:
ttim = IF time cycle time
tcnt = IF counter cycle time
terr = discrimination window (controlled by the EW registers)



The precision of the measurements is adjustable by controlling the discrimination window. This is adjustable by programming the control registers EW0...EW2.
The measurement time per cycle is adjustable by setting the register IFS0 - IFS2.
The center frequency of the discrimination window is adjustable by the control register "CF0" to "CF4". The available values are reported in databyte specification

5.0 I²C BUS INTERFACE

5.1 General Description

The TDA7421N supports the I2C bus protocol. This protocol defines the devices sending data into the bus as transmitter and the receiving device as the receiver.
The device that controls the transfer is a master and the device being controlled is the slave. The master will always initiates data transfer and provide the clock to transmit or receive operations.

5.2 Data Transition

Data transition on the SDA line must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as START or STOP condition.

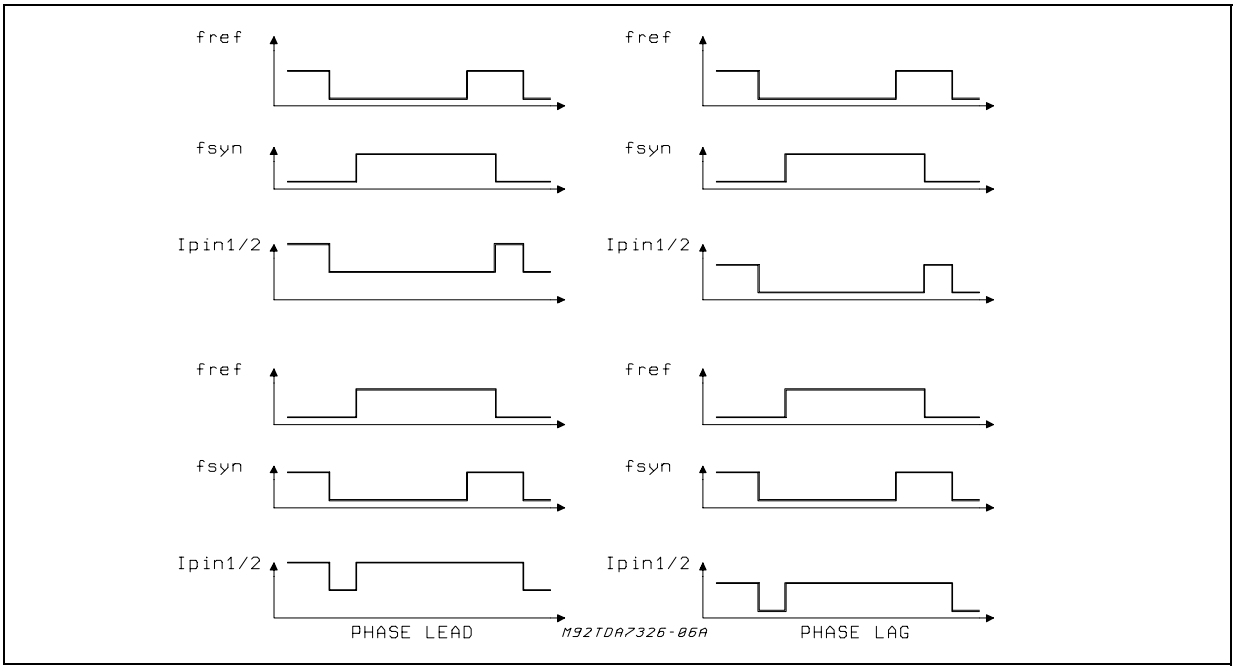
5.3 Start Condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus.The TDA7421N continuously monitors the SDA and SCL lines for a valid START and will not response to any command if this condition has not been met.

5.4 Stop condition

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminate the communication between the devices and force's the bus interface of the TDA7421N into the initial condition.

Figure 5. Phase Comparator



5.5 Acknowledge

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it has received the eight bits of data correctly.

5.6 Data transfer

During data transfer the TDA7421N samples the SDA line on the leading edge of the SCL clock, Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

5.7 Device Addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device it is addressing. The most significant 6 bits of the slave address identify the device type.
The TDA7421N device code is fixed as "110001".
The next significant bit is used either to address the tuner section (1) or the PLL section (0) of the chip.
Following a START condition the master sends slave address word; the TDA7421N will "acknowledge" after this first transmission and wait for a second word (the word address field).This 8 bit address field provides an access to any of the 8 internal addresses. Upon receipt of the word address the TDA7421N slave device will respond with an "acknowledge".
At this time, all the following words transmits to the TDA7421N will be considered as data.The internal address will be automatically incremented. After each word receipt the TDA7421N will answer with an "acknowledge".
The interface protocol comprises:

– a subaddress byte
– a sequence of data (N-bytes + acknowledge)
– a stop condition (P)
– a start condition (S)
– a chip address byte

CONTROL REGISTER FUNCTION

REGISTER NAME	FUNCTION
PC	Programmable Counter for VCO Frequency
RC	Reference Counter PLL
IRC	Reference Counter IF
IFCM	IF Counter Mode
EW	Frequency Error Window
IFENA	Enable IF Counter
CF	Center Frequency IF Counter
IFS	Sampling Time IF Counter
PM	Stby, FM, AM, AM swallow mode (PLL Mode)
D	Programmable Delay for Lock Detector
LPIN1/2	Loop Filter Input Select
A	Charge Pump High Current
B	Charge Pump Low Current
LDENA	Lock Detector Enable
CURRH	Set Current High

Figure 6. IF Counter Block Diagram

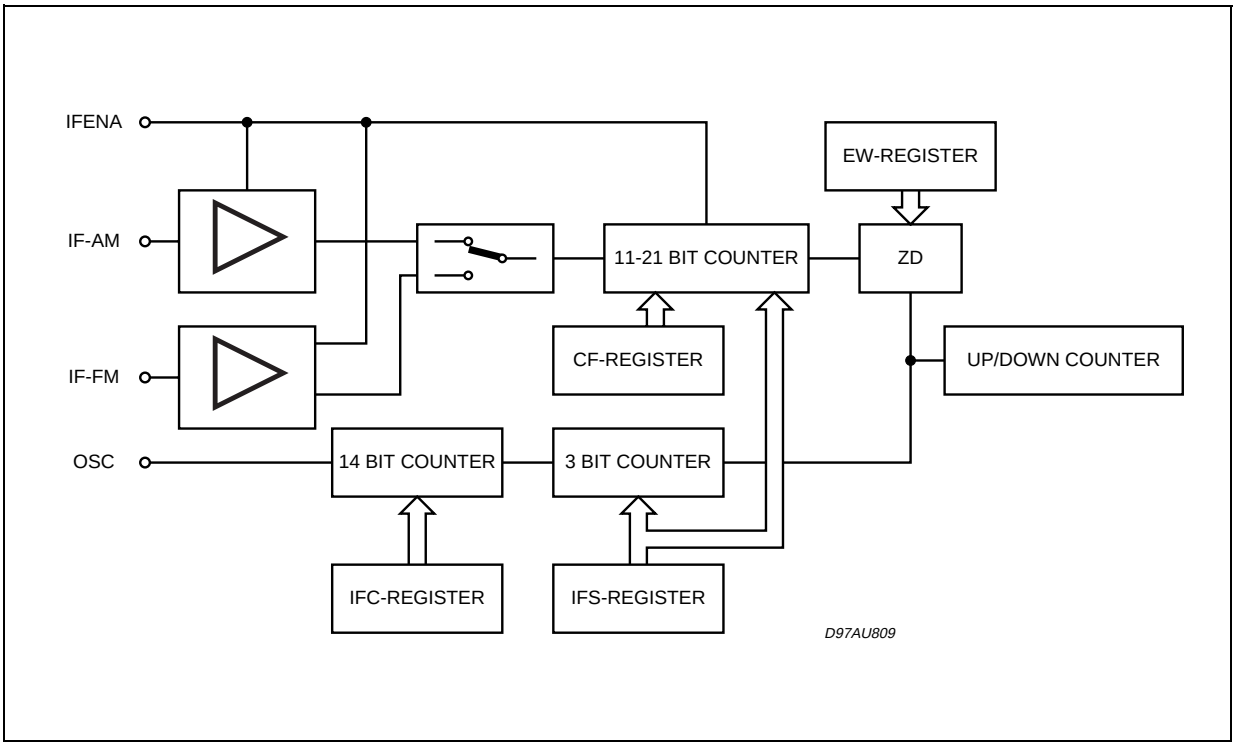
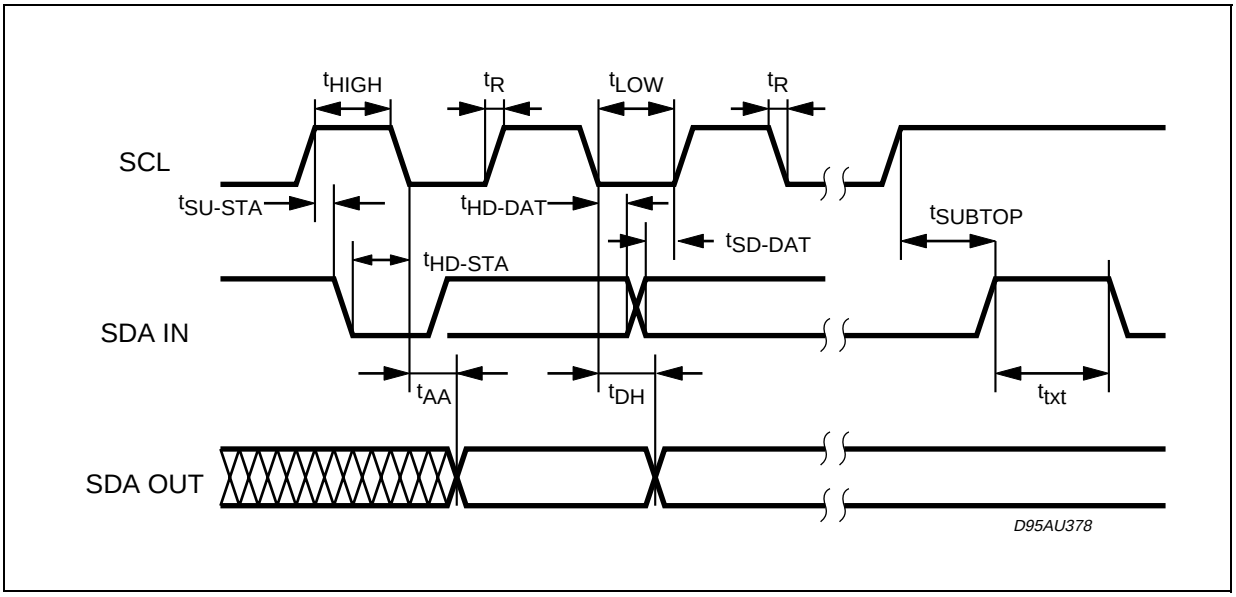
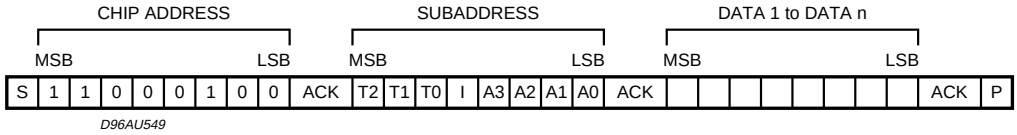


Figure 7. I²C Bus Timing Diagram

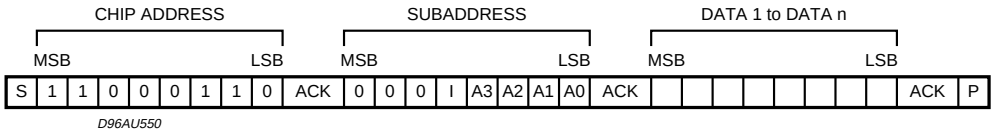


5.8 Frame Example

For addressing the PLL part:



for the TUNER part:



ACK:	Acknowledge
S:	Start
P:	Stop
I:	Page mode
T2, T1, T0:	used in test mode (for PLL only, for TUNER addressing they must be 0)
A3, A2, A1, A0:	Mode selection

5.9 TUNER SUBADDRESS

MSB							LSB	FUNCTION
X	X	X	I	A3	A2	A1	A0	
				0	0	0	0	STATUS
				0	0	0	1	FM STOP STATION/FM IF AGC
				0	0	1	0	FM SMETER SLIDER/ AM IF2 AMP
				0	0	1	1	AM AGC1/AM STOP STATION
				0	1	0	0	IFT1/IFT2
				0	1	0	1	FRONT END ADJUSTMENT
				0	1	1	0	FM DEMOD ADJUSTMENT
				0	1	1	1	FM AUDIO MUTE GAIN/FM IF BUFFERS/ FM SOFT MUTE
				1	0	0	0	FM HOLE DETECTOR/FM DETUNING
				1	0	0	1	TUNER TESTING
			0					Page mode disabled
			1					Page mode enabled
0	0	0						must be "0"

5.10 PLL SUBADDRESS

MSB							LSB	FUNCTION
T3	T2	T1	I	A3	A2	A1	A0	
				0	0	0	0	Charge pump control
				0	0	0	1	PLL counter 1 (LSB)
				0	0	1	0	PLL counter 2 (MSB)
				0	0	1	1	PLL reference counter 1 (LSB)
				0	1	0	0	PLL reference counter 2 (MSB)
				0	1	0	1	PLL lockdetector control and PLL mode select
				0	1	1	0	IFC reference counter 1 (LSB)
				0	1	1	1	IFC reference counter 2 (MSB) and IFC mode select
				1	0	0	0	IF counter control 1
				1	0	0	1	IF counter control 2
			0					Page mode disabled
			1					Page mode enabled

T1, T2, T3 are used for testing the PLL, in application mode they have to be "0".

6.0 PLL DATA BYTE SPECIFICATION

6.1 CHARGE PUMP CONTROL

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	High current = 0mA
				0	0	0	1	High current = 0.5mA
				0	0	1	0	High current = 1.0mA
				0	0	1	1	High current = 1.5mA
				0	1	0	0	High current = 2.0mA
				0	1	0	1	High current = 2.5mA
				0	1	1	0	High current = 3.0mA
				0	1	1	1	High current = 3.5mA
				1	0	0	1	High current = 4.5mA
				1	0	1	0	High current = 5.0mA
				1	0	1	1	High current = 5.5mA
				1	1	0	0	High current = 6.0mA
				1	1	0	1	High current = 6.5mA
				1	1	1	0	High current = 7.0mA
				1	1	1	1	High current = 7.5mA
		0	0					Low current = 0µA
		0	1					Low current = 15µA
		1	0					Low current = 100µA
		1	1					Low current = 115µA
	0							Select low Current
	1							Select high Current
0								Select loop filter 1
1								Select loop filter 2
LPIN1/2	CURRH	B1	B0	A3	A2	A1	A0	Subaddress = 00H

6.2 PLL COUNTER 1 (LSB)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
all combinations allowed								
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Bit name Subaddress = 01H

6.3 PLL COUNTER 2 (MSB)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
all combinations allowed								
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536
PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	Bit name Subddress = 02H

Swallow mode: fvco/fsyn = LSB + MSB + 32

6.4 PLL REFERENCE COUNTER 1 (LSB)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
all combinations allowed								
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	Bit name Subaddress =03H

6.5 PLL REFERENCE COUNTER 2 (MSB)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
all combinations allowed								
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536
RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8	Bit name Subddress = 04H

fOSC/fREF = LSB + MSB + 1

6.6 LOCK DETECTOR & PLL MODE CONTROL

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
						0	0	PLL standby mode
						0	1	PLL AM
						1	0	not used
						1	1	PLL FM mode
				0	0			PD phase difference threshold 10ns
				0	1			PD phase difference threshold 20ns
				1	0			PD phase difference threshold 30ns
				1	1			PD phase difference threshold 40ns
		0	0					Not used in application mode
		0	1					Activation delay = $4 \cdot f_{ref}$
		1	0					Activation delay = $6 \cdot f_{ref}$
		1	1					Activation delay = $8 \cdot f_{ref}$
0								No lock detector controlled chargepump
1								Lock detector controlled chargepump
LDENA		D3	D2	D1	D0	PM1	PM0	Bit name Subaddress = 05H

6.7 IF COUNTER REFERENCE CONTROL 1 (LSB)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
all combinations allowed								
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255
IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0	Bit name Subaddress = 06H

6.8 IF COUNTER REFERENCE CONTROL 2 (MSB) AND IF COUNTER MODE SELECT

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
all combinations allowed								
		1	1	1	1	0	1	MSB = 15616
		1	1	1	1	1	0	MSB = 15872
		1	1	1	1	1	1	MSB = 16128
0	0							NOT USED IN APPLICATION MODE
0	1							IF counter FM mode
1	0							IF counter AM mode
1	1							not used
IFCM1	IFCM0	IRC13	IRC12	IRC11	IRC10	IRC9	IRC8	Bit name Subaddress = 07H

fosc/ftim = LSB + MSB + 1

6.9 IF COUNTER CONTROL 1

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	don't use
					0	0	1	don't use
					0	1	0	don't use
					0	1	1	EW delta f = ±6.25KHz (FM); ±1KHz (AM)
					1	0	0	EW delta f = ±12.5KHz (FM); ±2KHz (AM)
					1	0	1	EW delta f = ±25KHz (FM); ±4KHz (AM)
					1	1	0	EW delta f = ±50KHz (FM); ±8KHz (AM)
					1	1	1	EW delta f = ±100KHz (FM); ±16KHz (AM)
0								IF counter disabled / stand by
1								IF counter enabled
IFENA					EW2	EW1	EW0	Bit name Subaddress = 08H

6.10 IF COUNTER CONTROL 2

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
			0	0	0	0	0	fcenter = 10.60000MHz (FM) 448KHz (AM)
			0	0	0	0	1	fcenter = 10.60625MHz (FM) 449KHz (AM)
			0	0	0	1	0	fcenter = 10.61250MHz (FM) 450KHz (AM)
			0	0	0	1	1	fcenter = 10.61875MHz (FM) 451KHz (AM)
			0	0	1	0	0	fcenter = 10.62500MHz (FM) 452KHz (AM)
			0	0	1	0	1	fcenter = 10.63125MHz (FM) 453KHz (AM)
			0	0	1	1	0	fcenter = 10.63750MHz (FM) 454KHz (AM)
			0	0	1	1	1	fcenter = 10.64375MHz (FM) 455KHz (AM)
			0	1	0	0	0	fcenter = 10.65000MHz (FM) 456KHz (AM)
			0	1	0	0	1	fcenter = 10.65625MHz (FM) 457KHz (AM)
			0	1	0	1	0	fcenter = 10.66250MHz (FM) 458KHz (AM)
			0	1	0	1	1	fcenter = 10.66875MHz (FM) 459KHz (AM)
			0	1	1	0	0	fcenter = 10.67500MHz (FM) 460KHz (AM)
			0	1	1	0	1	fcenter = 10.68125MHz (FM) 461KHz (AM)
			0	1	1	1	0	fcenter = 10.68750MHz (FM) 462KHz (AM)
			0	1	1	1	1	fcenter = 10.69375MHz (FM) 463KHz (AM)
			1	0	0	0	0	fcenter = 10.70000MHz (FM) 464KHz (AM)
			1	0	0	0	1	fcenter = 10.70625MHz (FM) 465KHz (AM)
			1	0	0	1	0	fcenter = 10.71250MHz (FM) 466KHz (AM)
			1	0	0	1	1	fcenter = 10.71875MHz (FM) 467KHz (AM)
			1	0	1	0	0	fcenter = 10.72500MHz (FM) 468KHz (AM)
			1	0	1	0	1	fcenter = 10.73125MHz (FM) 469KHz (AM)
			1	0	1	1	0	fcenter = 10.73750MHz (FM) 470KHz (AM)
			1	0	1	1	1	fcenter = 10.74375MHz (FM) 471KHz (AM)
			1	1	0	0	0	fcenter = 10.75000MHz (FM) 472KHz (AM)
			1	1	0	0	1	fcenter = 10.75625MHz (FM) 473KHz (AM)
			1	1	0	1	0	fcenter = 10.76250MHz (FM) 474KHz (AM)
			1	1	0	1	1	fcenter = 10.76875MHz (FM) 475KHz (AM)
			1	1	1	0	0	fcenter = 10.77500MHz (FM) 476KHz (AM)
			1	1	1	0	1	fcenter = 10.78125MHz (FM) 477KHz (AM)
			1	1	1	1	0	fcenter = 10.78750MHz (FM) 478KHz (AM)
			1	1	1	1	1	fcenter = 10.79375MHz (FM) 479KHz (AM)
0	0	0						tsample = 20.48ms (FM mode); 128ms (AM; MODE)
0	0	1						tsample = 10.24ms (FM mode); 64ms (AM; MODE)
0	1	0						tsample = 5.12ms (FM mode); 32ms (AM; MODE)
0	1	1						tsample = 2.56ms (FM mode); 16ms (AM; MODE)
1	0	0						tsample = 1.28ms (FM mode); 8ms (AM;MODE)
1	0	1						tsample = 640ms (FM mode); 4ms (AM;MODE)
1	1	0						tsample = 320ms (FM mode); 2ms (AM; MODE)
1	1	1						tsample = 160ms (FM mode); 1ms (AM; MODE)
IFS2	IFS1	IFS0	CF4	CF3	CF2	CF1	CF0	bit name Subaddress = 09H

7.0 TUNER DATA BYTE SPECIFICATION

7.1 ADDRESS ORGANIZATION (Tuner AM/FM)

FUNCTION	SUBAD	MSbit							LSbit
		B7	B6	B5	B4	B3	B2	B1	B0
STATUS	00H	N.U.	FMMUTE	FMADJ	AM STEREO	SEEK	AM/FM/ STBY	AM/FM/ STBY	AM/FM/ STBY
FM STOP STATION/ FM IF AGC	01H	FAG2	FAG1	FAG0	FSS4	FSS3	FSS2	FSS1	FSS0
FM SMETER SLIDER/ AM IF2 AMP	02H	FSL4	FSL3	FSL2	FSL1	FSL0	IF2A1	IF2A0	N.U.
AM AGC1/AM STOP STATION	O3H	ASS3	ASS2	ASS1	ASS0	AAGN1	AAGN0	AAGW1	AAGW0
IFT1/IFT2	04H	T2A3	T2A2	T2A1	T2A0	T1A3	T1A2	T1A1	T1A0
FRONT END ADJUSTMENT	05H	ANA3	ANA2	ANA1	ANA0	RFA3	RFA2	RFA1	RFA0
FM DEMOD ADJUSTMENT	06H	N.U.	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0
FM AUDIO MUTE GAIN/FM IF BUFFERS/ FM SOFT MUTE	07H	FSM3	FSM2	FSM1	FSM0	FFBL1	FBL0	AUM1	AUM0
FM HOLE DETECTOR/ FM DETUNING	08H	BWM2	BWM1	BWM0	HDM4	HDM3	HDM2	HDM1	HDM0
TUNER TESTING	09H	PLLTEST	T2	T1	T0	SDDIS	BWDIS	HDDID	SMDIS

7.2 STATUS (subaddress 00H)

MSB							LSB	FUNCTION
	S6	S5	S4	S3	S2	S1	S0	
	FMMUTE	FMADJ	AMSTEREO	SEEK	AM/FM/ STBY	AM/FM/ STBY	AM/FM/ STBY	
					0	0	0	Stand by
					0	0	1	FM on
					0	1	0	AM on (/6)
					1	1	0	AM on (/10)
					1	0	0	AM on (/8)
				0				RECEPTION
				1				SEEK
			0		AM	AM	AM	AM IFC Out
			1		AM	AM	AM	AM Stereo OUT
	0	1			FM	FM	FM	FM on for demodulator adjustment, demod on
	1	1			FM	FM	FM	FM on for demodulator adjustment, demod muted

7.3 FM STOP STATION / FM IF AGC (subaddress 01H)

MSB							LSB	FUNCTION
FAG2		FAG1	FAG0	FSS4	FSS3	FSS2	FSS1	FSS0
FM ifagc MSB	FM ifagc	FM ifagc LSB	FM stopstation MSB	FM stopstation	FM stopstation	FM stopstation	FM stopstation LSB	**FM STOP STATION THRESHOLD**
			0	0	0	0	0	Maximum sensitivity
			X	X	X	X	X	
			1	1	1	1	1	Minimum sensitivity
			all combinations allowed					
								FM IF AGC THRESHOLD
0	0	0						Maximum sensitivity
X	X	X						
1	1	0						Minimum sensitivity
1	1	1						Keyed AGC disabled
all combinations allowed								

7.4 FM SMETER SLIDER\IF2 AMPLIFIER (subaddress 02H)

MSB							LSB	FUNCTION
FSL4	FSL3	FSL2	FSL1	FSL0	IF2A1	IF2A0		
FMsmeter slider MSB	FMsmeter slider	FMsmeter slider	FMsmeter slider	FMsmeter sliderr LSB	AM if2Amp MSB	AM if2Amp LSB		**FM SMETERSLIDING (mV)**
0	0	0	0	0				0
0	0	0	0	1				48
X	X	X	X	X				
1	1	1	1	1				1500
all combinations allowed								
								IF2 AMPLIFIER GAIN
					0	0		50dB
					0	1		53dB
					1	0		56dB
					1	1		59dB

7.5 AM STOP STATION / AM AGC1 (subaddress 03H)

MSB							LSB	FUNCTION
ASS3	ASS2	ASS1	ASS0	AAGN1	AAGN0	AAGW1	AAGW0	
AM stopstation MSB	AM stopstation	AM stopstation	AM stopstation LSB	AMnagc MSB	AMnagc LSB	AMwagc MSB	AMwagc LSB	**AM WAGC THRESHOLD**
						0	0	Minimum sensitivity
						X	X	
						1	1	Maximum sensitivity
						all comb. allowed		
								AM NAGC THRESHOLD
				0	0			Minimum sensitivity
				X	X			
				1	1			Maximum sensitivity
				all comb. allowed				
								AM STOP STATION THRESHOLD
0	0	0	0					Maximum sensitivity
X	X	X	X					
1	1	1	1					Minimum sensitivity
all combinations allowed								

7.6 IFT1/IFT2 (subaddress 04H)

MSB							LSB	FUNCTION
T2A3	T2A2	T2A1	T2A0	T1A3	T1A2	T1A1	T1A0	
IFT2adjust MSB	IFT2adjust	IFT2adjust	IFT2adjust LSB	IFT1adjust MSB	IFT1adjust	IFT1adjust	IFT1adjust LSB	**ADJUSTMENT CAPACITOR**
				0	0	0	0	15Cift1
				0	1	1	1	8Cift1
				1	0	1	0	4Cift1
				1	1	0	1	2Cift1
				1	1	1	0	Cift2 (= 380pF)
				1	1	1	1	0
				all combinations allowed				
0	0	0	0					0
0	0	0	1					Cift1 (= 1.57pF)
0	0	1	0					2Cift2
0	1	0	0					4Cift2
1	0	0	0					8Cift2
1	1	1	1					15Cift2
all combinations allowed								

7.7 FRONT END ADJUSTMENT (subaddress 05H)

MSB							LSB	FUNCTION
ANA3	ANA2	ANA1	ANA0	RFA3	RFA2	RFA1	RFA0	
ANT adjustm ±	ANT adjustm MSB	ANT adjustm	ANT adjustm LSB	RF adjustm ±	RF adjustm MSB	RF adjustm	RF adjustm LSB	**Voffset RF varicap / VPLL**
				X	0	0	0	0
				0	0	0	1	-3.6%
				0	0	1	0	-7.2%
				0	1	0	0	-14.3%
				0	1	1	1	-25%
				1	0	0	1	3.6%
				1	0	1	0	7.2%
				1	1	0	0	14.3%
				1	1	1	1	25%
				all combinations allowed				
								Voffset antenna varicap / VPLL
X	0	0	0					0
0	0	0	1					-3.6%
0	0	1	0					-7.2%
0	1	0	0					-14.3%
0	1	1	1					-25%
1	0	0	1					3.6%
1	0	1	0					7.2%
1	1	0	0					14.3%
1	1	1	1					25%
all combinations allowed								

7.8 FM DEMODULATOR ADJUSTMENT (subaddress 06H)

MSB							LSB	FUNCTION
	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0	
	demadj MSB	demadj	demadj	demadj	demadj	demadj	demadj LSB	**ADJUSTMENT CAPACITOR**
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	$C_{demod\ (= 50fF)}$
	0	0	0	0	0	1	0	$2C_{demod}$
	0	0	0	0	1	0	0	$4C_{demod}$
	0	0	0	1	0	0	0	$8C_{demod}$
	0	0	1	0	0	0	0	$16C_{demod}$
	0	1	0	0	0	0	0	$32C_{demod}$
	1	0	0	0	0	0	0	$64C_{demod}$
	1	1	1	1	1	1	1	$127C_{demod}$
	all combinations allowed							

7.9 FM SOFT MUTE / FM IF AMPLIFIER/FM AUDIO MUTE GAIN (subaddress 07H)

MSB							LSB	FUNCTION
FSM3	FSM2	FSM1	FSM0	FBL1	FBL0	AUM1	AUM0	
FM softmute MSB	FM softmute	FM softmute	FM softmute LSB	buff2 gain	buff2 gain	Mute Depth MSB	Mute Depth LSB	FM SOFT MUTE THRESHOLD
0	0	0	0					Maximum sensitivity
X	X	X	X					
1	1	1	1					Minimum sensitivity
all combinations allowed								
								Audio max mute attenuation
						0	0	-5
						0	1	-7.5
						1	0	-10
						1	1	-12.5
						all comb. allowed		
								Buffer 2 Gain (dB)
				0	0			10
				0	1			6
				1	0			8
				all else not allowed				

7.10 FM HOLE DETECTOR / FM DETUNING DETECTOR (subaddress 08H)

MSB							LSB	FUNCTION
BWM2	BWM1	BWM0	HDM4	HDM3	HDM2	HDM1	HDM0	
BW Slope 30kHz	BW Slope 15kHz	BW Slope 10kHz	Hole det MSB	Hole det	Hole det	Hole det	Hole det LSB	**MUTING SENSITIVITY(hole depth)**
			0	0	0	0	0	Minimum (deep hole)
			X	X	X	X	X	
			1	1	1	1	1	Maximum (shallow hole)
			all combinations allowed					
RECEPTION								**DETUNING MUTE RANGE (KHz)**
0	0	1						10
0	1	0						15
1	0	0						30
all else not allowed								
SEEK								**CLAMPING WINDOW**
0	0	X						Not allowed
0	1	0						Faster Clamping Window (±1KHz over Threshold)
X	X	X						
1	1	1						Slower Clamping Window (±4KHz over Threshold)
all combinations allowed								

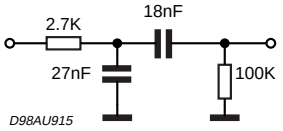
7.11 TUNER TESTING (subaddress 9H)

MSB							LSB	FUNCTION
PLL TEST	T2	T1	T0	SDDIS	BWDIS	HDDIS	SMDIS	
Test mode PLL	Test mode MSB	Test mode	Test mode LSB	SD output Disable	Bandwidth Disable	Hole detector Disable	Soft Mute Disable	
0	0	0	0	0	0	0	0	no test
								TEST MODES
					1	1	0	Soft Mute Test
					1	0	1	Hole Detector Test
					0	1	1	Bandwidth Test
					1	1	1	Audio Mute and SD Disabled
					all else not allowed			

7.11 TUNER TESTING (subaddress 9H)

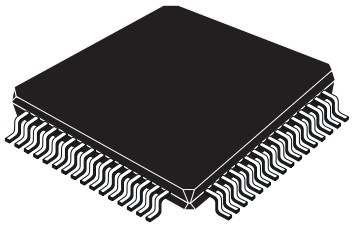
MSB							LSB	FUNCTION
	0	0	1					AMSSDAC Test
	0	1	0					FMSSDAC Test
	0	1	1					FMSMDAC Test
	1	0	0					FMHDDAC Test
	1	1	0					FMIFAGCDAC Test
	all else not allowed							
1								PLL Test

8.0 COMPONENT DESCRIPTION

CF1	Ceramic filter 10.7MHz, 180KHz BW
CF3-CF4	Ceramic filter 10.7MHz, 150KHz BW
CF2	Ceramic filter 450KHz, 6KHz BW
T1	FM RF transformer Unloaded Q= 69 3-1= 3 3/4T - 6-4= 3T 0.12f2UEW CTUNING(3-1)= 26.6pF @ 100MHz
T2	AM/FM IF1 transformer Unloaded Q= 70 1-3= 12T - 1-5= 6 - 5-3= 6 - 4-6= 2T 0.08f2UEW CINT(1-3) = 51pF; CEXT(1-3) = 5pF
T3	AM IF2 transformer Unloaded Q= 40 1-3= 178T - 1-2= 89T - 2-3= 89T - 4-6= 33T 0.05f2UEW CINT(1-3) = 180pF; CEXT(1-3) = 20pF
L2	Oscillator coil Unloaded Q= 8 06-4= 2 1/2T 0.12f2UEW CTUNING(6-4)= 36.8pF @ 100MHz
L6	Demodulator Coil Unloaded Q= 35 6-4= 27T 0.1f2UEW CINT(4-6)= 47pF; CEXT(4-6) = 13.5pF
AM BPF RC	

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP64