

## HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage ( $\varphi_1$ )
- internal key pulse for phase detector ( $\varphi_1$ ) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage ( $\varphi_2$ )
- larger catching range obtained by coincidence detector ( $\varphi_3$ ; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

### QUICK REFERENCE DATA

Supply voltage	V <sub>1-16</sub>	typ.	12 V
Supply current	I <sub>1</sub>	typ.	30 mA
<b>Input signals</b>			
Sync separator input voltage (peak-to-peak value)	V <sub>9-16(p-p)</sub>		3 to 4 V
Noise separator input voltage (peak-to-peak value)	V <sub>10-16(p-p)</sub>		3 to 4 V
Pulse duration switch input voltage			
at t = 7 $\mu$ s (thyristor driving)	V <sub>4-16</sub>		9,4 to V <sub>1-16</sub> V
at t = 14 $\mu$ s + t <sub>d</sub> (transistor driving)	V <sub>4-16</sub>		0 to 3,5 V
at t = 0 (input 4 open or V <sub>3-16</sub> = 0)	V <sub>4-16</sub>		5,4 to 6,6 V
<b>Output signals</b>			
Vertical sync output pulse (peak-to-peak value)	V <sub>8-16(p-p)</sub>	typ.	11 V
Burst gating output pulse (peak-to-peak value)	V <sub>7-16(p-p)</sub>	typ.	11 V
Line drive pulse (peak-to-peak value)	V <sub>3-16(p-p)</sub>	typ.	10,5 V

### PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

## Supply voltage

at pin 1 (voltage source)

 $V_{1-16}$  max. 13,2 V

at pin 2

 $V_{2-16}$  max. 18 V

## Voltages

Pin 4

 $V_{4-16}$  max. 13,2 V

Pin 9

 $\pm V_{9-16}$  max. 6 V

Pin 10

 $\pm V_{10-16}$  max. 6 V

Pin 11

 $V_{11-16}$  max. 13,2 V

## Currents

Pins 2 and 3 (thyristor driving) (peak value)

 $I_{2M}, -I_{3M}$  max. 650 mA

Pins 2 and 3 (transistor driving) (peak value)

 $I_{2M}, -I_{3M}$  max. 400 mA

Pin 4

 $I_4$  max. 1 mA

Pin 6

 $\pm I_6$  max. 10 mA

Pin 7

 $-I_7$  max. 10 mA

Pin 11

 $I_{11}$  max. 2 mA

Total power dissipation

 $P_{tot}$  max. 800 mW

Storage temperature

 $T_{stg}$  -25 to + 125 °C

Operating ambient temperature

 $T_{amb}$  0 to + 70 °C**CHARACTERISTICS** at  $V_{1-16} = 12$  V;  $T_{amb} = 25$  °C; measured in Fig. 1**Sync separator**

Input switching voltage

 $V_{9-16}$  typ. 0,8 V

Input keying current

 $I_g$  5 to 100  $\mu$ AInput leakage current at  $V_{9-16} = -5$  V $I_g$  < 1  $\mu$ A

Input switching current

 $I_g$   $\leq$  5  $\mu$ A

Switch off current

 $I_g$  > 100  $\mu$ A  
typ. 150  $\mu$ A

Input signal (peak-to-peak value)

 $V_{9-16(p-p)}$  3 to 4 V\*

\* Permissible range 1 to 7 V.

**Noise separator**

Input switching voltage	$V_{10-16}$	typ.	1,4 V
Input keying current	$I_{10}$		5 to 100 $\mu\text{A}$
Input switching current	$I_{10}$	>	100 $\mu\text{A}$
		typ.	150 $\mu\text{A}$
Input leakage current at $V_{10-16} = -5 \text{ V}$	$I_{10}$	<	1 $\mu\text{A}$
Input signal (peak-to-peak value)	$V_{10-16(p-p)}$		3 to 4 V*
Permissible superimposed noise signal (peak-to-peak value)	$V_{10-16(p-p)}$	<	7 V

**Line flyback pulse**

Input current	$I_6$	typ.	1 mA
			0,02 to 2 mA
Input switching voltage	$V_{6-16}$	typ.	1,4 V
Input limiting voltage	$V_{6-16}$		-0,7 to + 1,4 V

**Switching on VCR**

Input voltage	$V_{11-16}$		0 to 2,5 V
	$V_{11-16}$		9 to $V_{1-16}$ V
Input current	$-I_{11}$	<	200 $\mu\text{A}$
	$I_{11}$	<	2 mA

**Pulse duration switch**For  $t = 7 \mu\text{s}$  (thyristor driving)

Input voltage	$V_{4-16}$		9,4 to $V_{1-16}$ V
Input current	$I_4$	>	200 $\mu\text{A}$

For  $t = 14 \mu\text{s} + t_d$  (transistor driving)

Input voltage	$V_{4-16}$		0 to 3,5 V
Input current	$-I_4$	>	200 $\mu\text{A}$

For  $t = 0$ ;  $V_{3-16} = 0$  or input pin 4 open

Input voltage	$V_{4-16}$		5,4 to 6,6 V
Input current	$I_4$	typ.	0 $\mu\text{A}$

\* Permissible range 1 to 7 V.

<b>Vertical sync pulse (positive-going)</b>			
Output voltage (peak-to-peak value)	$V_{8-16(p-p)}$	>	10 V
		typ.	11 V
Output resistance	$R_8$	typ.	2 k $\Omega$
Delay between leading edge of input and output signal	$t_{on}$	typ.	15 $\mu s$
Delay between trailing edge of input and output signal	$t_{off}$	typ.	$t_{on}$ $\mu s$
<b>Burst gating pulse (positive-going)</b>			
Output voltage (peak-to-peak value)	$V_{7-16(p-p)}$	>	10 V
		typ.	11 V
Output resistance	$R_7$	typ.	70 $\Omega$
Pulse duration; $V_{7-16} = 7$ V	$t_p$	typ.	4 $\mu s$
			3,7 to 4,3 $\mu s$
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7-16} = 7$ V	$t$	typ.	2,65 $\mu s$
			2,15 to 3,15 $\mu s$
Output trailing edge current	$I_7$	typ.	2 mA
<b>Line flyback-blanking pulse (positive-going)</b>			
Output voltage (peak-to-peak value)	$V_{7-16(p-p)}$		4 to 5 V
Output resistance	$R_7$	typ.	70 $\Omega$
Output trailing edge current	$I_7$	typ.	2 mA
<b>Line drive pulse (positive-going)</b>			
Output voltage (peak-to-peak value)	$V_{3-16(p-p)}$	typ.	10,5 V
Output resistance			
for leading edge of line pulse	$R_3$	typ.	2,5 $\Omega$
for trailing edge of line pulse	$R_3$	typ.	20 $\Omega$
Pulse duration (thyristor driving)			
$V_{4-16} = 9,4$ to $V_{1-16}$ V	$t_p$	typ.	7 $\mu s$
			5,5 to 8,5 $\mu s$
Pulse duration (transistor driving)			
$V_{4-16} = 0$ to 4 V; $t_{fp} = 12$ $\mu s$	$t_p$		14 + $t_d$ $\mu s^*$
Supply voltage for switching off the output pulse	$V_{1-16}$	typ.	4 V
<b>Overall phase relation</b>			
Phase relation between middle of sync pulse and the middle of the flyback pulse	$t$	typ.	2,6 $\mu s^{**}$
Tolerance of phase relation	$ \Delta t $	<	0,7 $\mu s$

\*  $t_d$  = switch-off delay of line output stage.\*\* Line flyback pulse duration  $t_{fp} = 12$   $\mu s$ .

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control  $\varphi_2$ .

If additional adjustment is applied it can be arranged by current supply at pin 5 such that

$$\Delta I_5 / \Delta t \quad \text{typ.} \quad 30 \mu\text{A}/\mu\text{s}$$

#### Oscillator

Threshold voltage low level

$$V_{14-16} \quad \text{typ.} \quad 4,4 \text{ V}$$

Threshold voltage high level

$$V_{14-16} \quad \text{typ.} \quad 7,6 \text{ V}$$

Discharge current

$$\pm I_{14} \quad \text{typ.} \quad 0,47 \text{ mA}$$

Frequency; free running ( $C_{\text{Osc}} = 4,7 \text{ nF}$ ;  
 $R_{\text{Osc}} = 12 \text{ k}\Omega$ )

$$f_o \quad \text{typ.} \quad 15,625 \text{ kHz}$$

Spread of frequency

$$\Delta f_o / f_o < \pm 5 \%^*$$

Frequency control sensitivity

$$\Delta f_o / \Delta I_{15} \quad \text{typ.} \quad 31 \text{ Hz}/\mu\text{A}$$

Adjustment range of network in circuit (Fig. 1)

$$\Delta f_o / f_o \quad \text{typ.} \quad \pm 10 \%$$

Influence of supply voltage on frequency

$$\frac{\Delta f_o / f_o}{\Delta V / V_{\text{nom}}} < \pm 0,05 \%^*$$

Change of frequency when  $V_{1-16}$  drops to 5 V

$$\Delta f_o < \pm 10 \%^*$$

Temperature coefficient of oscillator frequency

$$< \pm 10^{-4} \text{ Hz/K}^*$$

#### Phase comparison $\varphi_1$

Control voltage range

$$V_{13-16} \quad 3,8 \text{ to } 8,2 \text{ V}$$

Control current (peak value)

$$\pm I_{13M} \quad 1,9 \text{ to } 2,3 \text{ mA}$$

Output leakage current  
at  $V_{13-16} = 4 \text{ to } 8 \text{ V}$

$$I_{13} < 1 \mu\text{A}$$

Output resistance

at  $V_{13-16} = 4 \text{ to } 8 \text{ V}$

at  $V_{13-16} < 3,8 \text{ V}$  or  $> 8,2 \text{ V}$

$$R_{13} \quad \text{high ohmic} \quad **$$

$$R_{13} \quad \text{low ohmic} \quad \blacktriangle$$

Control sensitivity

$$\text{typ.} \quad 2 \text{ kHz}/\mu\text{s}$$

Catching and holding range ( $82 \text{ k}\Omega$  between pins 13 and 15)

$$\Delta f \quad \text{typ.} \quad \pm 780 \text{ Hz}$$

Spread of catching and holding range

$$\Delta(\Delta f) \quad \text{typ.} \quad \pm 10 \%^*$$

\* Excluding external component tolerances.

\*\* Current source.

▲ Emitter follower.

**Phase comparison  $\varphi_2$  and phase shifter**

Control voltage range	$V_{5-16}$	5,4 to 7,6 V
Control current (peak value)	$\pm I_{5M}$	typ. 1 mA
Output resistance		high ohmic *
at $V_{5-16} = 5,4$ to $7,6$ V		
at $V_{5-16} < 5,4$ V or $> 7,6$ V	$R_5$	typ. 8 k $\Omega$
Input leakage current		
$V_{5-16} = 5,4$ to $7,6$ V	$I_5$	$<$ 5 $\mu$ A
Permissible delay between leading edge of output pulse and leading edge of flyback pulse ( $t_{fp} = 12 \mu$ s)	$t_d$	$<$ 15 $\mu$ s
Static control error	$\Delta t/\Delta t_d$	$<$ 0,2 %

**Coincidence detector  $\varphi_3$** 

Output voltage	$V_{11-16}$	0,5 to 6 V
Output current (peak value)		
without coincidence	$I_{11M}$	typ. 0,1 mA
with coincidence	$-I_{11M}$	typ. 0,5 mA

**Time constant switch**

Output voltage	$V_{12-16}$	typ. 6 V
Output current (limited)	$\pm I_{12}$	$<$ 1 mA
Output resistance		
at $V_{11-16} = 2,5$ to $7$ V	$R_{12}$	typ. 0,1 k $\Omega$
at $V_{11-16} < 1,5$ V or $> 9$ V	$R_{12}$	typ. 60 k $\Omega$

**Internal gating pulse**

Pulse duration	$t_p$	typ. 7,5 $\mu$ s
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\* Current source.