TA8102P

POWER DRIVE IC FOR CD PLAYER.

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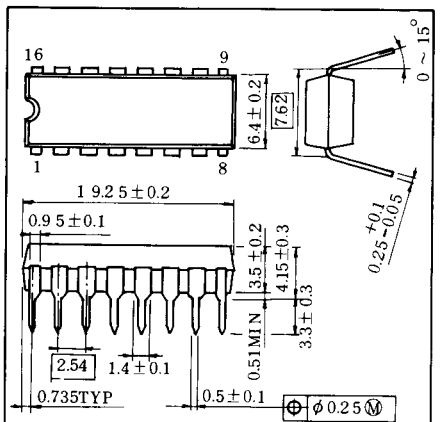
This is the most suitable for the power driver of the general-purpose motor.

- Two operation amplifiers with bootstrap terminals are incorporated.
- BTL Application also available.
  (BTL Application is realized with single 5V power supply)
- High output current : $I_{O(peak)}$=1A
- High input impedance is realized by built-in buffer amplifier.
- Built-in thermal shut down.

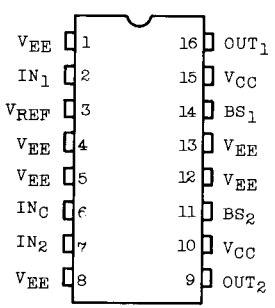
Unit in mm



Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.

JEDEC	—
TOSHIBA	DIP16-P-300A

PIN CONNECTIONS



MAXIMUM RATINGS (Ta=25°C)

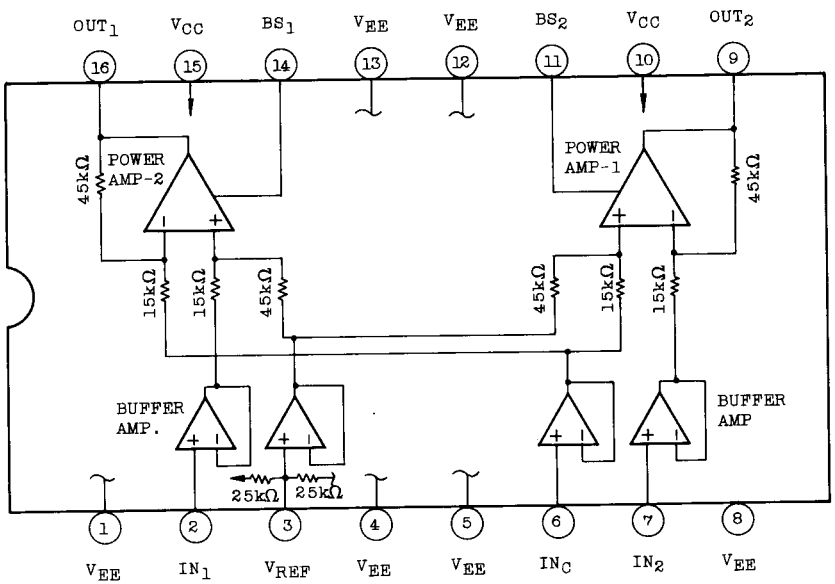
CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	15	V
Output Current	$I_{O(peak)}$	1	A
Power Dissipation	P_D	1.4*	W
Operating Temperature	Topr	-25~75	°C
Storage Temperature	Tstg	-55~150	°C

* Derated above Ta=25°C in the proportion of 11.2mW/°C.

Note: Output protection circuit is not incorporated.

Care should be taken not to short between { Output - V_{CC} / Output - GND / Output - Output }

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC}=5V, V_{EE}=-5V, 2ch Amp. operation, without bootstrap, R_L=∞, R_g=0Ω, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Power Supply Voltage		V_{CC}-V_{EE}			4.5	-	12	V
Quiescent Current		I_{CCQ}		IN_1=IN_2=IN_C=2.1V	5	11	18	mA
Input Offset Current		$\|I_{IO}\|$		IN_1, IN_2	-	100	300	nA
Input Bias Current		I_I		IN_1, IN_2	-	500	1500	nA
Output Offset Voltage		$\|V_{IO}\|$		IN_1=IN_2=IN_C=2.1V $R_{in}C$=20kΩ	-	-	60	mV
Output Voltage		V_{OH}		DC 350mA Load	2.8	-	-	V
		V_{OL}			-	-	-3.8	
Gain		G_V		R_L=5Ω, V_{IN}=100mVrms f=1kHz	8.5	9.5	10.5	dB
Frequency Range		f_C		R_L=5Ω, V_{IN}=100mVrms G=-3dB	50	-	-	kHz
Total Harmonics Distortion		THD		R_L=5Ω, f=1kHz V_{OUT}=5Vp-p	-	-50	-	dB
Slew Rate		SR		R_L=5Ω, V_{OUT}=2Vp-p	-	0.5	-	V/μs
Output Noise Voltage		V_{NO}		R_g=10kΩ	-	0.1	-	mVrms
Cross Talk		C.T		R_L=5Ω, R_g=10kΩ f=1kHz, V_O=0dBm CH1↔CH2	-	60	-	dB
Ripple Rejection Ratio	V_{CC} Side	RR_C		R_L=5Ω, R_g=10kΩ	-	65	-	dB
	V_{EE} Side	RR_E		f_R=100Hz, -20dBm	-	65	-	
Thermal Shut Down Operating Temperature		ON		Tj	-	140	-	°C
		OFF			-	130	-	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC}=5V, BTL operation, With bootstrap, R_L=∞, R_g=0Ω, R_{INC}=0Ω, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Power Supply Voltage	V_{CC}			4.5	-	12	V
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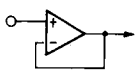
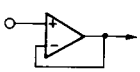
Input Offset Current	$\|I_{IO}\|$		IN_1, IN_2	-	100	300	nA
Input Bias Current	I_I		IN_1, IN_2	-	500	1500	nA
Output Offset Voltage	$\|V_{IO}\|$		IN_1=IN_2=IN_C=2.1V R_g=10kΩ, R_{INC}=20kΩ	-	-	60	mV
Output Voltage	V_{OH}		DC 350mA Load	4.0	-	-	V
	V_{OL}			-	-	1.2	
	V_O		R_L=8Ω, f=1kHz	-	8.5	-	Vp-p
Gain	G_V		R_L=5Ω, V_{IN}=100mVrms f=1kHz	14.5	15.5	16.5	dB
Frequency Range	f_C		R_L=5Ω, V_{IN}=100mVrms G=-3dB	50	-	-	kHz
Total Harmonic Distortion	THD		R_L=5Ω, f=1kHz V_{OUT}=5Vp-p	-	-50	-	dB
Slew Rate	SR		R_L=5Ω, V_{OUT}=2Vp-p	-	0.5	-	V/μs
Output Noise Voltage	V_{NO}		R_g=10kΩ	-	0.1	-	mVrms
Ripple Rejection Ratio	RR		R_L=5Ω, R_g=10kΩ f_R=100Hz, -20dBm	-	60	-	dB

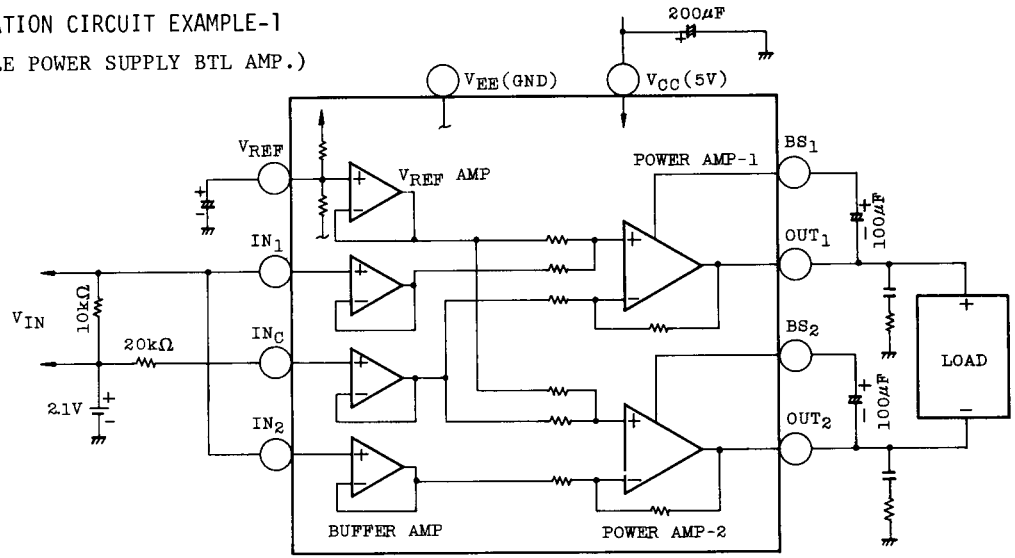
FUNCTIONAL DESCRIPTION OF EACH TERMINAL

PIN No.	SYMBOL	I/O	FUNCTION	REMARKS
1	V_{EE}	-	Negative power supply terminal.	Connect to pins 4,5,8,12 and 13
2	IN_1	I	Power amp.-1 Control signal input terminal.	 Buffer amp.
3	V_{REF}	-	Reference voltage source terminal.	
4 5	V_{EE}	-	Negative power supply voltage terminal.	Connect to pins 1 and 8.
6	IN_C	I	Power amp.-1 and 2 common control signal input terminal.	
7	IN_2	I	Power amp.-2 control signal input terminal.	 Buffer amp.
8	V_{EE}	-	Negative power supply voltage terminal.	Connect to pins 1, 4 and 5.
9	OUT_2	O	Power amp.-2 output terminal. Error signal amp. output of IN_2 and IN_C.	
10	V_{CC}	-	Positive power supply voltage terminal.	Connect to 15 pin
11	BS_2	-	Bootstrap terminal -2.	
12 13	V_{EE}	-	Negative power supply voltage terminal.	
14	BS_1	-	Bootstrap terminal -1.	
15	V_{CC}	-	Positive power supply voltage terminal.	Connect to 10 pin
16	OUT_1	O	Power amp.-1 output terminal. Error signal amp. output of IN_2 and IN_C.	

Note: Outside IC, connect to { V_{CC} terminal (10,15 pins)
V_{EE} terminal (1,4,5,8,12,13 pins)

APPLICATION CIRCUIT EXAMPLE-1

(SINGLE POWER SUPPLY BTL AMP.)

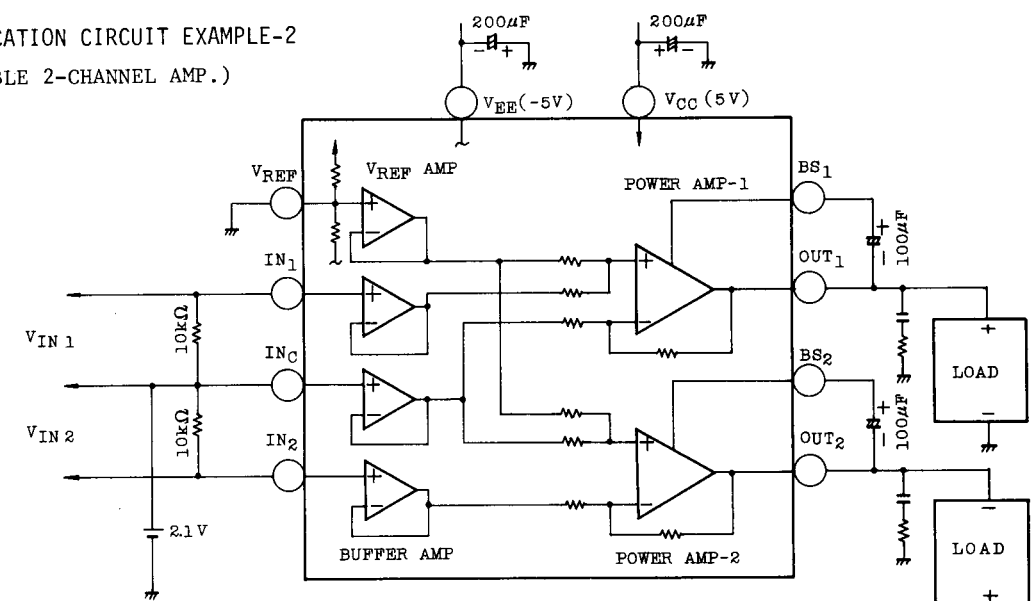


. Through connecting resistance to V_{REF} terminal, reference electric potential can be freely set.

. Gain is G_V=15.5dB fixed.

APPLICATION CIRCUIT EXAMPLE-2

(DOUBLE 2-CHANNEL AMP.)



. Take precautions for the polarity of the operating load of the power-amp.-1 as a non-inverting amplifier and of the power-amp.-2 as a inverting amplifier.

. Gain is fixed at G_V=9.5dB.

SILICON MONOLITHIC

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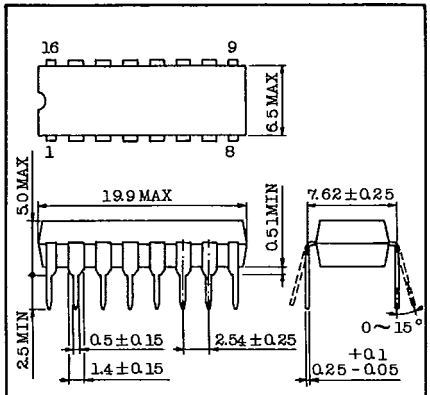
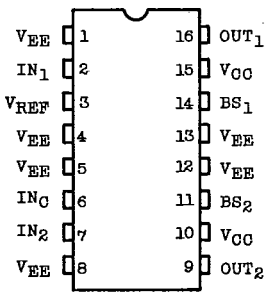


Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

JEDEC	—
TOSHIBA	3D16A-P

PIN CONNECTIONS



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