

MULTISYNC ON-SCREEN DISPLAY FOR MONITOR

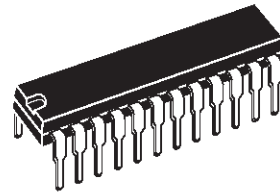
- CMOS SINGLE CHIP OSD FOR MONITOR
- BUILT IN 1 KBYTE RAM HOLDING :
 - PAGES' DESCRIPTORS
 - CHARACTER CODES
 - USER DEFINABLE CHARACTERS
- 128 ALPHANUMERIC CHARACTERS OR GRAPHIC SYMBOLS IN INTERNAL ROM (12 x 18 DOT MATRIX)
- UP TO 26 USER DEFINABLE CHARACTERS
- INTERNAL HORIZONTAL PLL (15 TO 120kHz)
- PROGRAMMABLE VERTICAL HEIGHT OF CHARACTER WITH A SLICE INTERPOLATOR TO MEET MULTI-SYNCH REQUIREMENTS
- PROGRAMMABLE VERTICAL AND HORIZONTAL POSITIONING
- FLEXIBLE SCREEN DESCRIPTION
- CHARACTER BY CHARACTER COLOR SELECTION (UP TO 8 DIFFERENT COLORS)
- PROGRAMMABLE BACKGROUND (COLOR, TRANSPARENT OR WITH SHADOWING)
- 50MHz MAXIMUM PIXEL CLOCK
- 2-WIRES ASYNCHRONOUS SERIAL MCU INTERFACE (I²C PROTOCOL)
- 8 x 8 BITS PWM DAC OUTPUTS (STV9425)
4 x 8 BITS PWM DAC OUTPUTS (STV9425B)
- SINGLE POSITIVE 5V SUPPLY

DESCRIPTION

The STV9425/25B/26 is an ON SCREEN DISPLAY for monitor. It is built as a slave peripheral connected to a host MCU via a serial I²C bus. It includes a display memory, controls all the display attributes and generates pixels from the data read in its on chip memory. The line PLL and a special slice interpolator allow to have a display aspect which does not depend on the line and frame frequencies. I²C interface allows MCU to make transparent internal access to prepare the next pages during the display of the current page. Toggle from one page to another by programming only one register.

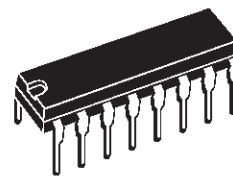
8 x 8 bits or 4 x 8 bits PWM DAC are available to provide DC voltage control to other peripherals.

The STV9425/25B/26 provides the user an easy to use and cost effective solution to display alphanumeric or graphic information on monitor screen.



SHRINK24
(Plastic Package)

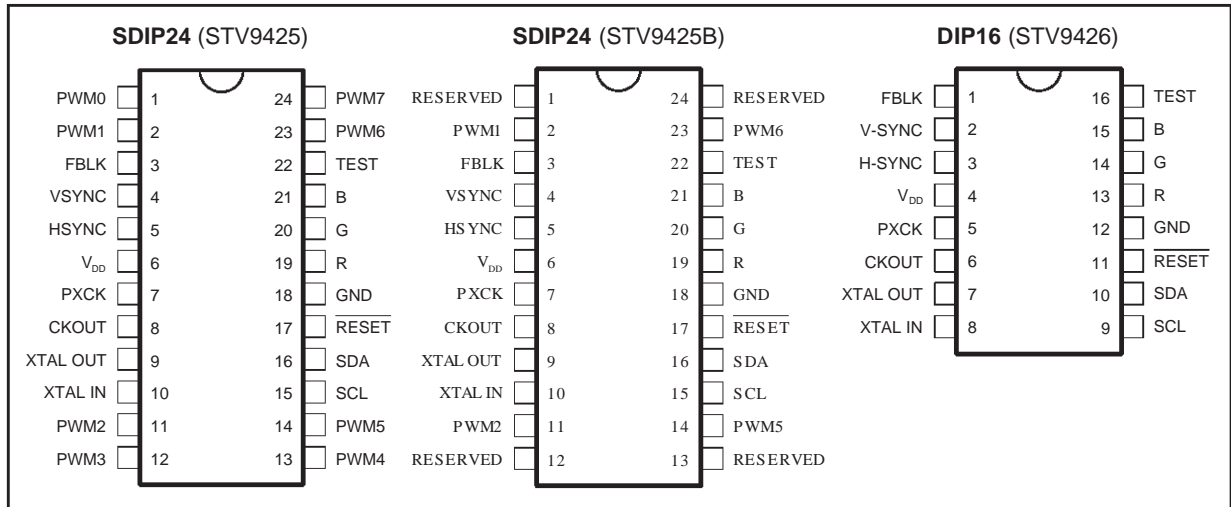
ORDER CODES : STV9425 - STV9425B



DIP16
(Plastic Package)

ORDER CODE : STV9426

PIN CONNECTIONS



9425-01 LEFS /9425B-01 LEFS/ 9426-01 LEFS

PIN DESCRIPTION

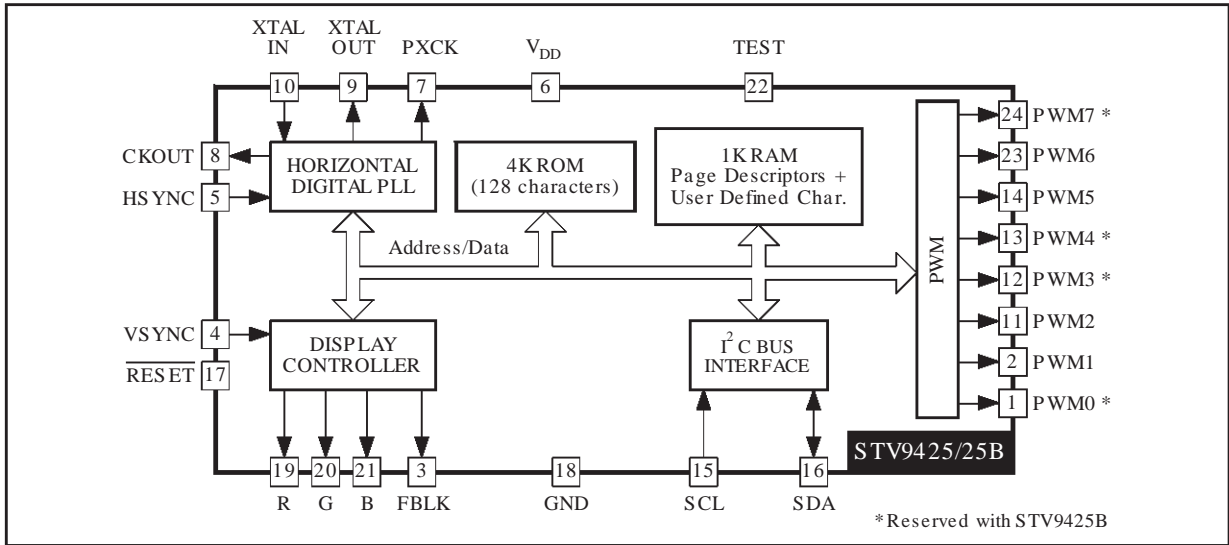
| Symbol | Pin Number | | I/O | Description |
|-----------------|------------|-------|-----|---|
| | SDIP24 | DIP16 | | |
| PWM0 | 1 * | - | O | DAC0 Output |
| PWM1 | 2 | - | O | DAC1 Output |
| FBLK | 3 | 1 | O | Fast Blanking Output |
| V-SYNC | 4 | 2 | I | Vertical Sync Input |
| H-SYNC | 5 | 3 | I | Horizontal Sync Input |
| V _{DD} | 6 | 4 | S | +5V Supply |
| PXCK | 7 | 5 | O | Pixel Frequency Output |
| CKOUT | 8 | 6 | O | Clock Output |
| XTAL OUT | 9 | 7 | O | Crystal Output |
| XTAL IN | 10 | 8 | I | Crystal or Clock Input |
| PWM2 | 11 | - | O | DAC2 Output |
| PWM3 | 12 * | - | O | DAC3 Output |
| PWM4 | 13 * | - | O | DAC4 Output |
| PWM5 | 14 | - | O | DAC5 Output |
| SCL | 15 | 9 | I | Serial Clock |
| SDA | 16 | 10 | I/O | Serial Input/Output Data |
| RESET | 17 | 11 | I | Reset Input (Active Low) |
| GND | 18 | 12 | S | Ground |
| R | 19 | 13 | O | Red Output |
| G | 20 | 14 | O | Green Output |
| B | 21 | 15 | O | Blue Output |
| TEST | 22 | 16 | I | Reserved (grounded in Normal Operation) |
| PWM6 | 23 | - | O | DAC6 Output |
| PWM7 | 24 * | - | O | DAC7 Output |

* Reserved with STV9425B (not to be connected)

9425-01.TBL

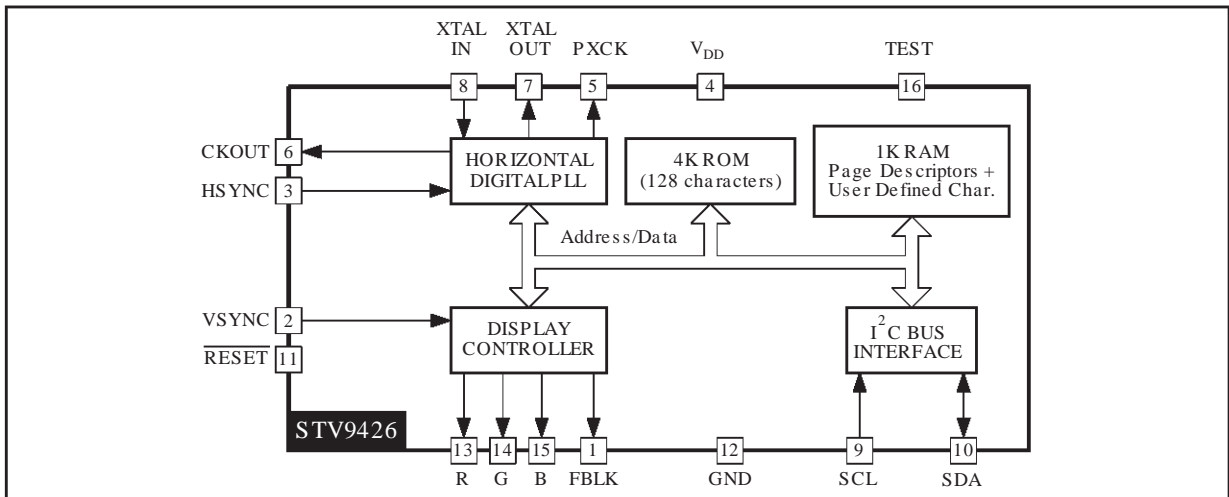
BLOCK DIAGRAMS

STV9425



9425-02.EPS

STV9426



9426-02.EPS

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-------------------|-------------------------------|------------|------|
| V _{DD} | Supply Voltage | -0.3, +7.0 | V |
| V _{IN} | Input Voltage | -0.3, +7.0 | V |
| T _{oper} | Operating Ambient Temperature | 0, +70 | °C |
| T _{stg} | Storage Temperature | -40, +125 | °C |

9425-02.TBL

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = 0V, T_A = 0 to 70°C, F_{XTAL} = 8 to 15MHz, TEST = 0 V, unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|-----------|------|------|------|------|
|--------|-----------|------|------|------|------|

SUPPLY

| | | | | | |
|-----------------|----------------|------|----|------|----|
| V _{DD} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| I _{DD} | Supply Current | - | 50 | 70 | mA |

INPUTS

| SCL, SDA, TEST, $\overline{\text{RESET}}$, V-SYNC and H-SYNC | | | | | |
|---|-----------------------|--------------------|--|-----|----|
| V _{IL} | Input Low Voltage | | | 0.8 | V |
| V _{IH} | Input High Voltage | 0.8V _{DD} | | | V |
| I _{IL} | Input Leakage Current | -20 | | +20 | μA |

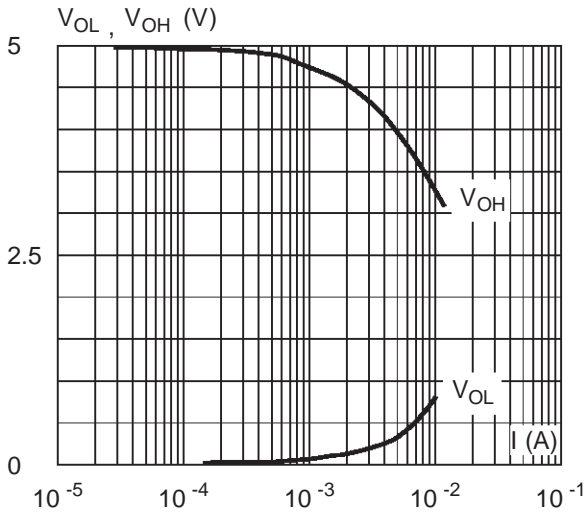
OUTPUTS

| R, G, B, FBLK, SDA, CKOUT, PXCK and PWMi (i = 0 to 7) | | | | | |
|---|--|--------------------|--|-----------------|---|
| V _{OL} | Output Low Voltage (I _{OL} = 1.6mA) | 0 | | 0.4 | V |
| V _{OH} | Output High Voltage (I _{OL} = -0.1mA) | 0.8V _{DD} | | V _{DD} | V |

9425-03.TBL

For R, G, B and FBLK outputs, see Figure 1.

Figure 1 : Typical R, G, B Outputs Characteristics



9425-17.EPS

TIMINGS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|-----------|------|------|------|------|
|--------|-----------|------|------|------|------|

OSCILATOR INPUT : XT1 (see Figure 2)

| | | | | | |
|------------|------------------|-----|--|----|-----|
| T_{WH} | Clock High Level | 20 | | | ns |
| T_{WL} | Clock Low Level | 20 | | | ns |
| F_{XTAL} | Clock Frequency | TBD | | 15 | MHz |
| F_{PXL} | Pixel Frequency | | | 50 | MHz |

RESET

| | | | | | |
|-----------|-----------------------|---|--|--|---------|
| T_{RES} | Reset Low Level Pulse | 4 | | | μ s |
|-----------|-----------------------|---|--|--|---------|

R, G, B, FBLK ($C_{LOAD} = 30pF$)

| | | | | | |
|------------|-------------------------------------|--|---|--|----|
| T_{RISE} | Rise Time (Note 1) | | 5 | | ns |
| T_{FALL} | Fall Time (Note 1) | | 5 | | ns |
| T_{SKEW} | Skew between R, G, B, FBLK (Note 1) | | 5 | | ns |

I²C INTERFACE : SDA AND SCL (see Figure 3)

| | | | | | |
|-------------|--|---|--|----|-----|
| F_{SCL} | SCL Clock Frequency | 0 | | 1 | MHz |
| T_{BUF} | Time the bus must be free between 2 access | 500 | | | ns |
| T_{HDS} | Hold Time for Start Condition | 500 | | | ns |
| T_{SUP} | Set up Time for Stop Condition | 500 | | | ns |
| T_{LOW} | The Low Period of Clock | 400 | | | ns |
| T_{HIGH} | The High Period of Clock | 400 | | | ns |
| T_{HDAT} | Hold Time Data | 0 | | | ns |
| T_{SUDAT} | Set up Time Data | 375 | | | ns |
| T_F | Fall Time of SDA | | | 20 | ns |
| T_R | Rise Time of Both SCL and SDA | Depend on the pull-up resistor and the load capacitance | | | |

Note 1 : These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches coming from corners of our processes and also temperature characterization.

Figure 2

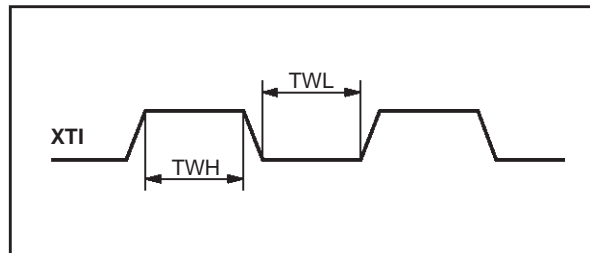
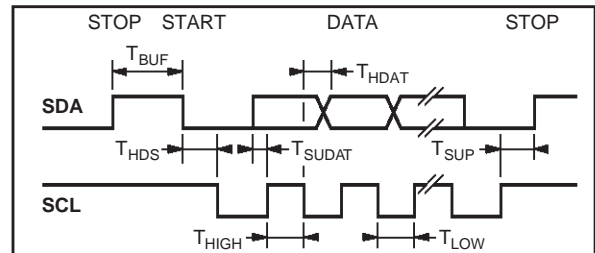


Figure 3



FUNCTIONAL DESCRIPTION

The STV9425/25B/26 display processor operation is controlled by a host MCU via the I²C interface. It is fully programmable through 16 internal read/write registers and performs all the display functions by generating pixels from data stored in its internal memory. After the page downloading from the MCU, the STV9425/25B/26 refreshes screen by its built in processor, without any MCU control (access). In addition, the host MCU has a direct access to the on chip 1Kbytes RAM during the display of the current page to make any update of its contents.

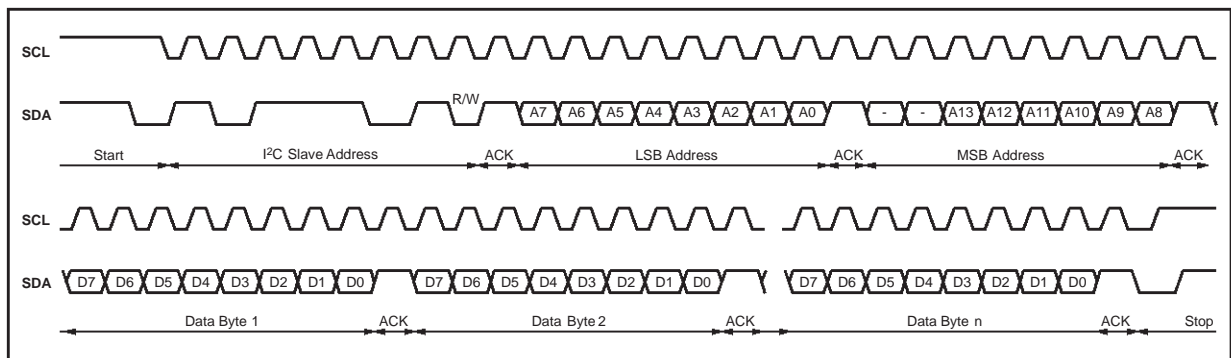
With the STV9425/25B/26, a page displayed on the screen is made of several strips which can be of 2 types : spacing or character and which are described by a table of descriptors and character codes in RAM. Several pages can be downloaded at the same time in the RAM and the choice of the current display page is made by programming the CONTROL register.

I - Serial Interface

The 2-wires serial interface is an I²C interface. To be connected to the I²C bus, a device must own its slave address ; the slave address of the STV9425/25B/26 is BA (in hexadecimal).

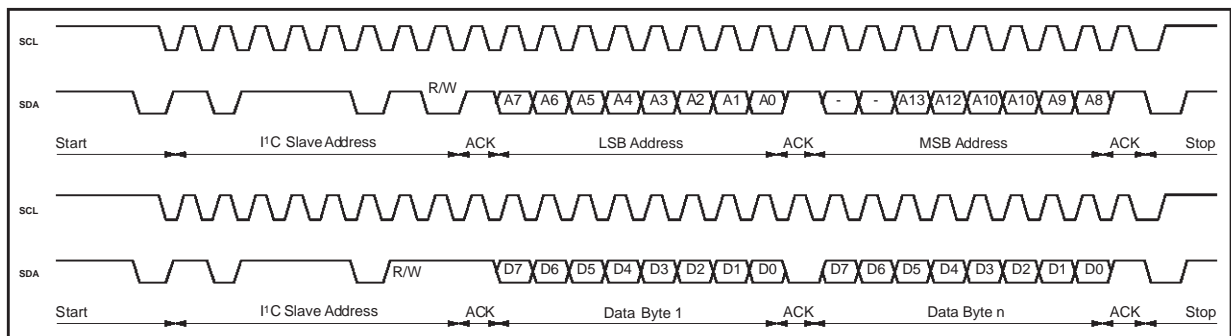
| | | | | | | | |
|----|----|----|----|----|----|----|-----|
| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|-----|

Figure 3 : STV9425/25B/26/I²C Write Operation



9425-06.AI

Figure 4 : STV9425/25B/26/I²C Read Operation

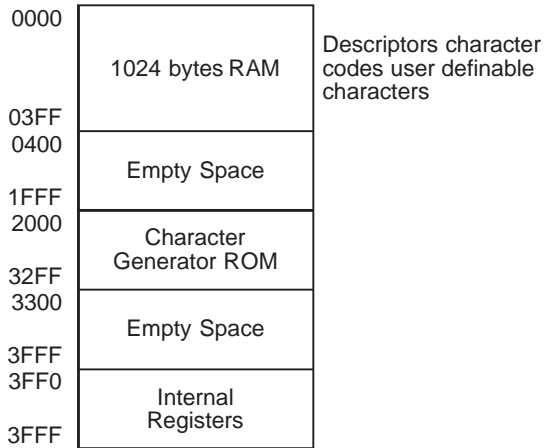


9425-06.EPS

FUNCTIONAL DESCRIPTION (continued)

I.3 - Addressing Space

STV9425/25B/26 registers, RAM and ROM are mapped in a 16Kbytes addressing space. The mapping is the following :



I.4 - Register Set

LINE DURATION

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FF0 | VSP | HSP | LD5 | LD4 | LD3 | LD2 | LD1 | LD0 |
| * | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

- VSP : V-SYNC active edge selection
= 0 : falling egde, = 1 : rising edge
- HSP : H-SYNC active edge selection
= 0 : falling egde, = 1 : rising edge
- LD[5:0] : LINE DURATION
(number of pixel period per line divided by 12 ie. Unit = 12 pixel periods).

HORIZONTAL DELAY

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FF1 | DD7 | DD6 | DD5 | DD4 | DD3 | DD2 | DD1 | DD0 |
| * | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

DD[7:0] : HORIZONTAL DISPLAY DELAY from the H-SYNC reference falling edge to the 1st pixel position of the character strips. Unit = 3 pixel periods.

CHARACTERS HEIGHT

| | | | | | | | | |
|------|---|---|-----|-----|-----|-----|-----|-----|
| 3FF2 | - | - | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
| * | - | - | 0 | 1 | 0 | 0 | 1 | 0 |

CH[5:0] : HEIGHT of the character strips in scan lines. For each scan line, the number of the slice which is displayed is given by :
 SLICE-NUMBER = $\text{round}\left(\frac{\text{SCAN-LINE-NUMBER} \times 18}{\text{CH}[5:0]}\right)$
 SCAN-LINE-NUMBER = Number of the current scan line of the strip.

DISPLAY CONTROL

| | | | | | | | | |
|------|-----|-----|-----|-----|---|----|----|----|
| 3FF3 | OSD | FBK | FL1 | FL0 | - | P8 | P7 | P6 |
| * | 0 | 0 | 0 | 0 | - | 0 | 0 | 0 |

- OSD : ON/OFF (if 0, R, G, B and FBLK are 0).
- FBK : Fast blanking control :
= 1 : FBLK = 1, forcing black where there is no display,
= 0 : FBLK is active only during character display.
- FL[1:0] : Flashing mode :
- 00 : No flashing. The character attribute is ignored,
- 01 : 1/1 flashing (a duty cycle = 50%),
- 10 : 1/3 flashing,
- 11 : 3/1 flashing.
- P[8:6] : Address of the 1st descriptor of the current displayed pages.
P[13:9] and P[5:0] = 0 ; up to 8 different pages can be stored in the RAM.

LOCKING CONDITION TIME CONSTANT

| | | | | | | | | |
|------|----|-----|-----|-----|---|-----|-----|-----|
| 3FF4 | FR | AS2 | AS1 | AS0 | - | BS2 | BS1 | BS0 |
| * | 0 | 0 | 1 | 0 | - | 0 | 1 | 0 |

- FR : Free Running ; if = 1 PLL is disabled and the pixel frequency keeps its last value.
- AS[2:0] : Phase constant during locking conditions.
- BS[2:0] : Frequency constant during locking conditions.

CAPTURE PROCESS TIME CONSTANT

| | | | | | | | | |
|------|---|-----|-----|-----|---|-----|-----|-----|
| 3FF5 | - | AF2 | AF1 | AF0 | - | BF2 | BF1 | BF0 |
| * | - | 0 | 1 | 1 | - | 0 | 1 | 1 |

- AF[2:0] : Phase constant during the capture process.
- BF[2:0] : Frequency constant during the capture process.

INITIAL PIXEL PERIOD

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FF6 | PP7 | PP6 | PP5 | PP4 | PP3 | PP2 | PP1 | PP0 |
| * | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

PP[7:0] : Value to initialize the pixel period of the PLL.

FREQUENCY MULTIPLIER

| | | | | | | | | |
|------|---|---|---|---|-----|-----|-----|-----|
| 3FF7 | - | - | - | - | FM3 | FM2 | FM1 | FM0 |
| * | - | - | - | - | 1 | 0 | 1 | 0 |

FM[3:0] : Frequency multiplier of the crystal frequency to reach the high frequency used by the PLL to derive the pixel frequency.

FUNCTIONAL DESCRIPTION (continued)

PULSE WIDTH MODULATOR 0

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FF8 | V07 | V06 | V05 | V04 | V03 | V02 | V01 | V00 |
| * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

V0[7:0] : Digital value of the 1st PWM D to A converter (Pin1).

PULSE WIDTH MODULATOR 1

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FF9 | V17 | V16 | V15 | V14 | V13 | V12 | V11 | V10 |
| * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

V1[7:0] : Digital value of the 2nd PWMDAC (Pin2).

PULSE WIDTH MODULATOR 2

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FFA | V27 | V26 | V25 | V24 | V23 | V22 | V21 | V20 |
| * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

V2[7:0] : Digital value of the 3rd PWM DAC (Pin11).

PULSE WIDTH MODULATOR 3

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FFB | V37 | V36 | V35 | V34 | V33 | V32 | V31 | V30 |
| * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

V3[7:0] : Digital value of the 4th PWM DAC (Pin12).

PULSE WIDTH MODULATOR 4

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FFC | V47 | V46 | V45 | V44 | V43 | V42 | V41 | V40 |
| * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

V4[7:0] : Digital value of the 5th PWM DAC (Pin13).

PULSE WIDTH MODULATOR 5

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FFD | V57 | V56 | V55 | V54 | V53 | V52 | V51 | V50 |
| * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

V5[7:0] : Digital value of the 6th PWM DAC (Pin14).

PULSE WIDTH MODULATOR 6

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FFE | V67 | V66 | V65 | V64 | V63 | V62 | V61 | V60 |
| * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

V6[7:0] : Digital value of the 7th PWM DAC (Pin23).

PULSE WIDTH MODULATOR 7

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 3FFF | V77 | V76 | V75 | V74 | V73 | V72 | V71 | V70 |
| * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

V7[7:0] : Digital value of the 8th PWM DAC (Pin24).

Note : * is power on reset value.

II - Descriptors

SPACING

| | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| MSB | 0 | - | - | - | - | - | - | - |
| LSB | SL7 | SL6 | SL5 | SL4 | SL3 | SL2 | SL1 | SL0 |

SL[7:0] : The number of the scan lines of the spacing strip (1 to 255).

CHARACTER

| | | | | | | | | |
|-----|----|----|----|----|----|----|----|----|
| MSB | 1 | DE | - | ZY | - | - | C9 | C8 |
| LSB | C7 | C6 | C5 | C4 | C3 | C2 | C1 | 0 |

C[9:0] : The address of the first character code of the strip (even).

DE : Display enable :

- DE = 0, R = G = B = 0 and FBLK = FBK (display control register) on whole strip,
- DE = 1, display of the characters.

ZY : Zoom, ZY = 1 all the scan lines are repeated once.

III - Code Format

| | | | | | | | | |
|-----|-----|------------------|-----|-----|----|----|----|----|
| MSB | SET | CHARACTER NUMBER | | | | | | |
| LSB | BK3 | BK2 | BK1 | BK0 | FL | RF | GF | BF |

SET : The set CHARACTER NUMBER

- If SET = 0 : ROM character,
- If SET = 1 :

- If CHARACTER NUMBER is 0 to 25, a user redefinable character (UDC) located in RAM at the address equal to :
38 x CHARACTER NUMBER,
- If CHARACTER NUMBER is 26 to 63, space character,
- If CHARACTER NUMBER > 63, end of line.

FL : Flashing attribute (the flashing mode is defined in the DISPLAY CONTROL register).

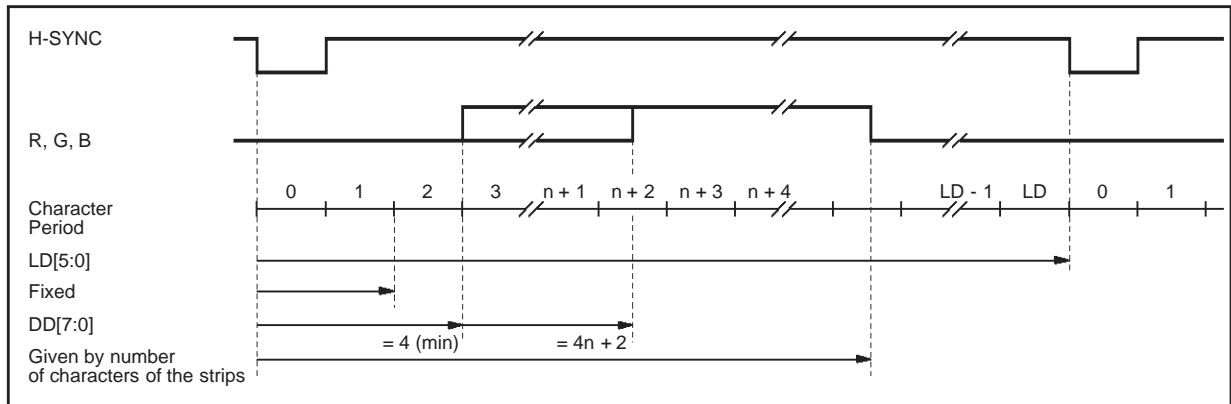
RF, GF, BF: Foreground color.

BK[3:0] : Background :

- If BK3 = 0, BK[2:0] = background color R, G and B,
- If BK3 = 1, shadowing :
BK1 : horizontal shadowing.
(if BK1 = 0, the background is transparent).
BK2 and BK0 must be equal to 0.

FUNCTIONAL DESCRIPTION (continued)

Figure 5 : Horizontal Timing



IV - Clock and Timing

The whole timing is derived from the XTALIN and the SYNCHRO (horizontal and vertical) input frequencies. The XTALIN input frequency can be an external clock or a crystal signal thanks to XTALIN/XTALOUT pins. The value of this frequency can be chosen between 8 and 15MHz, it is available on the CKOUT pin and is used by the PLL to generate a pixel clock locked on the horizontal synchro input signal.

IV.1 - Horizontal Timing (see Figure 5)

The number of pixel periods is given by the LINE DURATION register and is equal to :

$$[LD[5:0] + 1] \times 12.$$

(LD[5:0] : value of the LINE DURATION register).

This value allows to choose the horizontal size of the characters. The horizontal left margin is given by the HORIZONTAL DELAY register and is equal to :

$$[DD[7:0] + 8] \times 3 \times T_{PXCK}$$

(DD[7:0] : value of the DISPLAY DELAY register and T_{PXCK} : pixel period).

This value allows to choose the horizontal position of the characters on the screen. The value of DD[7:0] must be equal or greater than 4 (the minimum value of the horizontal delay is $36 \times T_{PXCK} = 3$ character periods). The length of the active area, where R, G, B are different from 0, depends on the number of characters of the strips.

IV.2 - D to A Timing

The D to A converters of the STV9425/25B/26 are pulse width modulator converter. The frequency of the output signal is :

$$\frac{F_{XTAL}}{256}$$

and the duty cycle is : $\frac{Vi[7:0]}{256}$ per cent.

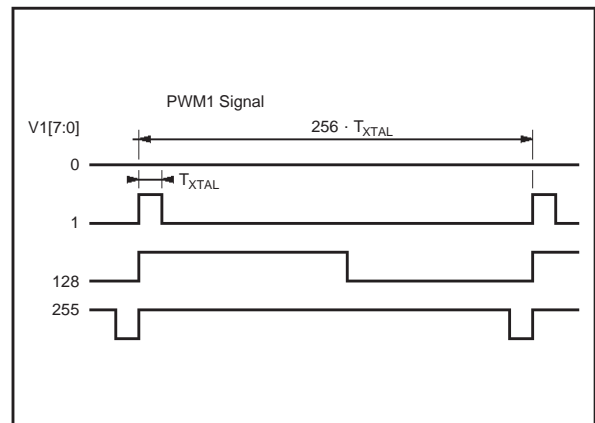
After a low pass filter, the average value of the output is : $\frac{Vi[7:0]}{256} \cdot V_{DD}$

V - Display Control

A screen is composed of successive scanlines gathered in several strips. Each strip is defined by a descriptor stored in memory. A table of descriptors allows screen composition and different tables can be stored in memory at the page addresses (8 possible \neq addresses). Two types of strips are available :

- Spacing strip : its descriptor (see II) gives the number of black (FBK = 1 in DISPLAYCONTROL register) or transparent (FBK = 0) lines.
- Character strip : its descriptor gives the memory address of the character codes corresponding to the 1st displayed character. The characters and attributes (see code format III) are defined by a succession of codes stored in the RAM at addresses starting from the 1st one given by the descriptor. A character strip can be displayed or not by using the DE bit of its descriptor. A zoom can be made on it by using the ZY bit.

Figure 6 : PWM Timing



FUNCTIONAL DESCRIPTION (continued)

After the falling edge on V-SYNC, the first strip descriptor is read at the top of the current table of descriptors at the address given by P[9:0] (see DISPLAY CONTROL register).

If it is a spacing strip, SL[7:0] black or transparent scan lines are displayed.

If it is a character strip, during CH[5:0] x (I + ZY)

scan lines (CH[5:0] given by the CHARACTER HEIGHT register), the character codes are read at the addresses starting from the 1st one given by the descriptor until a end of line character or the end of the scan line.

The next descriptor is then read and the same process is repeated until the next falling edge on V-SYNC.

Figure 7 : Relation between Screen/Address Page/Character Code in RAM

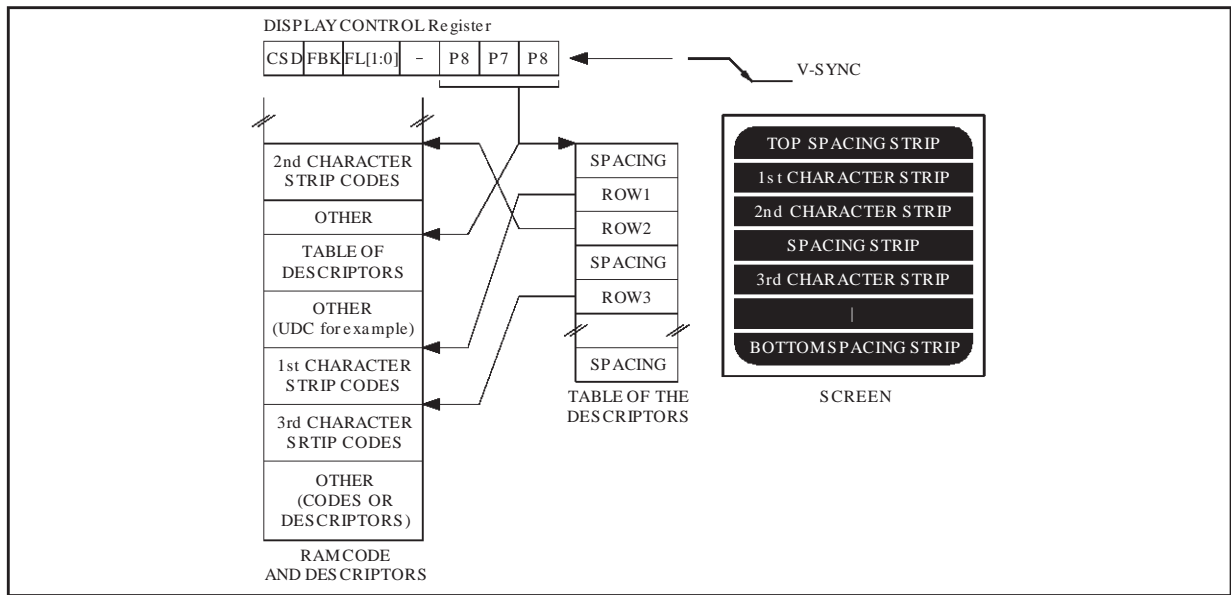
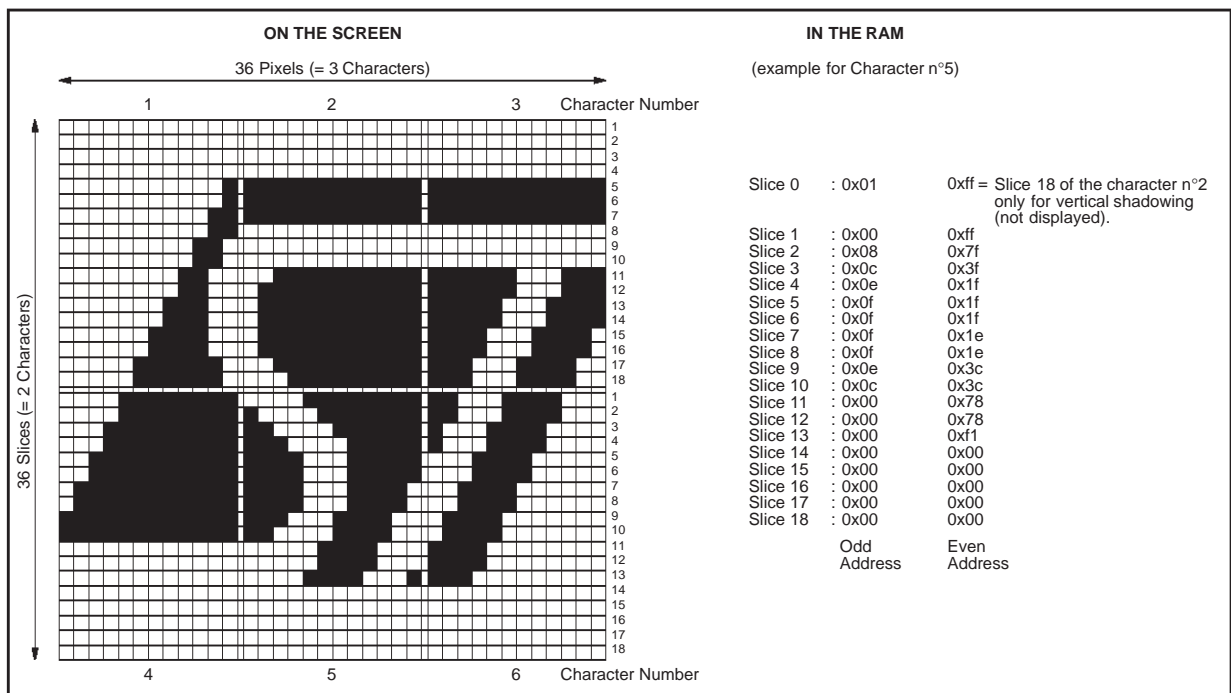


Figure 8 : User Definable Character



FUNCTIONAL DESCRIPTION (continued)

Table 1 : ROM Character Generator

| CHARACTER NUMBER C(6:0) | | C(6:4) | | | | | | | |
|-------------------------|--|--------|---|---|---|---|---|---|---|
| C(3:0) | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | | à | á | â | ã | ä | å | æ | ç |
| 1 | | è | é | ê | ë | ì | í | î | ï |
| 2 | | ò | ó | ô | õ | ö | ÷ | ¸ | ¹ |
| 3 | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| 4 | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| 5 | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| 6 | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| 7 | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| 8 | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| 9 | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| a | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| b | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| c | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| d | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| e | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |
| f | | ² | ³ | ´ | µ | ¶ | · | ¸ | ¹ |

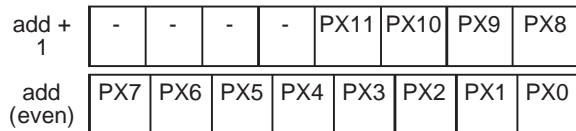
9425-11.EPS

FUNCTIONAL DESCRIPTION (continued)

VI - User Definable Character

The STV9425/25B/26 allows the user to dynamically define character(s) for his own needs (for a special LOGO for example). Like the ROM characters, a UDC is made of a 12 pixels x 18 slices dot matrix, but one more slice is added for the vertical shadowing when several UDCs are gathered to make a special great character (see Figure 8).

In a UDC, each pixel is defined with a bit, 1 refers to foreground, and 0 to background color. Each slice of a UDC uses 2 bytes :



PX11 is the left most pixel. Character slice address :
 SLICEADDRESS = 38 x (CHARACTER NUMBER)
 + (SLICE NUMBER).

Where :

- CHARACTER NUMBER is the number given by the character code,
- SLICE NUMBER is the number given by the slice interpolator (n° of the current slice of the strip : 1 < n < 18)

VII - ROM Character Generator

The STV9425/25B/26 includes a ROM character generator which is made of 128 alphanumeric or graphic characters (see Table 1)

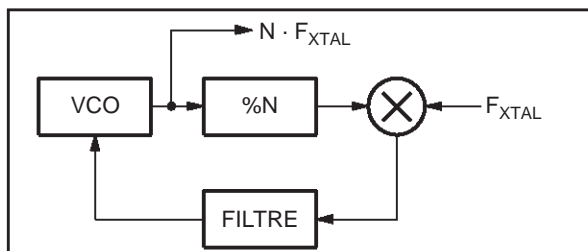
VIII - PLL

The PLL function of the STV9425/25B/26 provides the internal pixel clock locked on the horizontal synchro signal and used by the display processor to generate the R, G, B and fast blanking signals. It is made of 2 PLLs. The first one analogic (see Figure 9), provides a high frequency signal locked on the crystal frequency. The frequency multiplier is given by :

$$N = 2 \cdot (FM[3:0] + 3)$$

Where FM[3:0] is the value of the FREQUENCY MULTIPLIER register.

Figure 9 : Analogic PLL

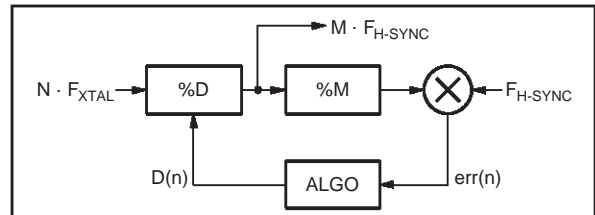


The second PLL, full digital (see Figure 10), provides a pixel frequency locked on the horizontal synchro signal. The ratio between the frequencies of these 2 signals is :

$$M = 12 \times (LD[5:0] + 1)$$

Where LD[5:0] is the value of the LINE DURATION register.

Figure 10 : Digital PLL



VIII.1 - Programming of the PLL Registers

Frequency Multiplier (@3FF7)

This register gives the ratio between the crystal frequency and the high frequency of the signal used by the 2nd PLL to provide, by division, the pixel clock. The value of this high frequency must be near to 200MHz (for example if the crystal is a 8MHz, the value of FM must be equal to 10) and greater than 6 x (pixel frequency).

Initial Pixel Period (@3FF6)

This register allows to increase the speed of the convergence of the PLL when the horizontal frequency changes (new graphic standart). The relationship between FM[3:0], PP[7:0], LD[5:0], F_HSYNC and F_XTAL is :

$$PP[7:0] = \text{round} \left(8 \cdot \frac{2 \cdot (FM[3:0] + 3) \cdot F_{XTAL}}{12 \cdot (LD[5:0] + 1) \cdot F_{H-SYNC}} - 24 \right)$$

Locking Condition Time Constant (@ 3FF4)

This register gives the constants AS[2:0] and BS[2:0] used by the algo part of the PLL (see Figure 10) to calculate, from the phase error, err(n), the new value, D(n), of the division of the high frequency signal to provide the pixel clock. These two constants are used only in locking condition, which is true, if the phase error is less than a fixed value during at least, 4 scan lines. If the phase error becomes greater than the fixed value, the PLL is not in locking condition but in capture process. In this case, the algo part of the PLL used the other constants, AF[2:0] and BF[2:0], given by the next register.

Capture Process Time Constant (@ 3FF5)

The choice between these two time constants (locking condition or capture process) allows to decrease the capture process time by changing the time response of the PLL.

FUNCTIONAL DESCRIPTION (continued)

VIII.2 - How to choose the value of the time constant ?

The time response of the PLL is given by its characteristic equation which is :

$$(x - 1)^2 + (\alpha + \beta) \cdot (x - 1) + \beta = 0.$$

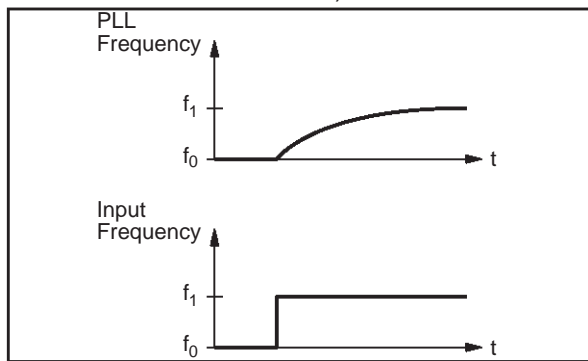
Where :

$\alpha = 3 \cdot LD[5:0] \cdot 2^{A-11}$ and $\beta = 3 \cdot LD[5:0] \cdot 2^{B-19}$.
 (LD[5:0] = value of the LINE DURATION register, A = value of the 1st time constant, AF or AS and B = value of the 2^d time constant, BF or BS).

As you can see, the solution depend only on the LINE DURATION and the TIME CONSTANTS given by the I²C registers.

If $(\alpha + \beta)^2 - 4\beta \geq 0$ and $2\alpha - \beta < 4$, the PLL is stable and its response is like this presented on Figure 11.

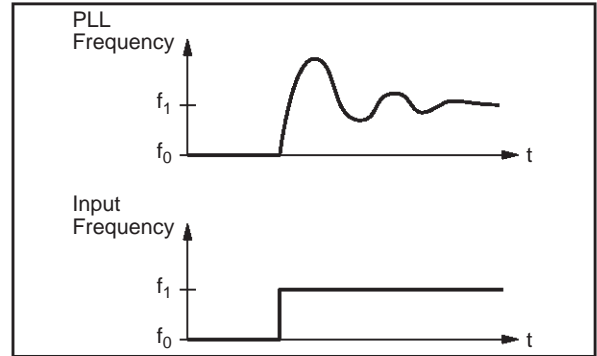
Figure 11 : Time Response of the PLL/Characteristic Equation Solutions (with Real Solutions)



If $(\alpha + \beta)^2 - 4\beta \leq 0$, the response of the PLL is like this presented on Figure 12.

In this case the PLL is stable if $\tau > 0.7$ damping coefficient).

Figure 12 : Time Response of the PLL/Characteristic Equation Solutions (with Complex Solutions)



The Table 2 gives some good values for A and B constants for different values of the LINE DURATION.

Summary

For a good working of the PLL :

- A and B time constants must be chosen among values for which the PLL is stable,
- B must be equal or greater than A and the difference between them must be less than 3,
- The greater (A, B) are, the faster the capture is.

An optimal choice for the most of applications might be :

- For locking condition : AS = 0 and BS = 1,
- For capture process : AS = 2 and BS = 4.

But for each application the time constants can be calculated by solving the characteristic equation and choosing the best response.

Table 2 : Valid Time Constants Examples

| B \ A | 0 | 1 | 2 | 3 | 4 | 5 | 6 |
|-------|------|---------------------|------|------|------|------|------|
| 0 | YYYY | YYYY | YYYY | YYYN | YNNN | NNNN | NNNN |
| 1 | YYYY | YYYY | YYYY | YYYN | YNNN | NNNN | NNNN |
| 2 | NYYY | YYYY | YYYY | YYYN | YNNN | NNNN | NNNN |
| 3 | NNNY | YYYY | YYYY | YYYN | YNNN | NNNN | NNNN |
| 4 | NNNN | NYYY ⁽¹⁾ | YYYY | YYYN | YNNN | NNNN | NNNN |
| 5 | NNNN | NNNY | YYYY | YYYN | YNNN | NNNN | NNNN |
| 6 | NNNN | NNNN | NYYY | YYYN | YNNN | NNNN | NNNN |
| 7 | NNNN | NNNN | NNNY | YYYN | YNNN | NNNN | NNNN |

Note : 1. Case of A[2:0] = 1 (001) and B[2:0] = 4 (100) :

| LD | 16 | 32 | 48 | 63 |
|----------------------|----|----|----|----|
| Valid Time Constants | N | Y | Y | Y |

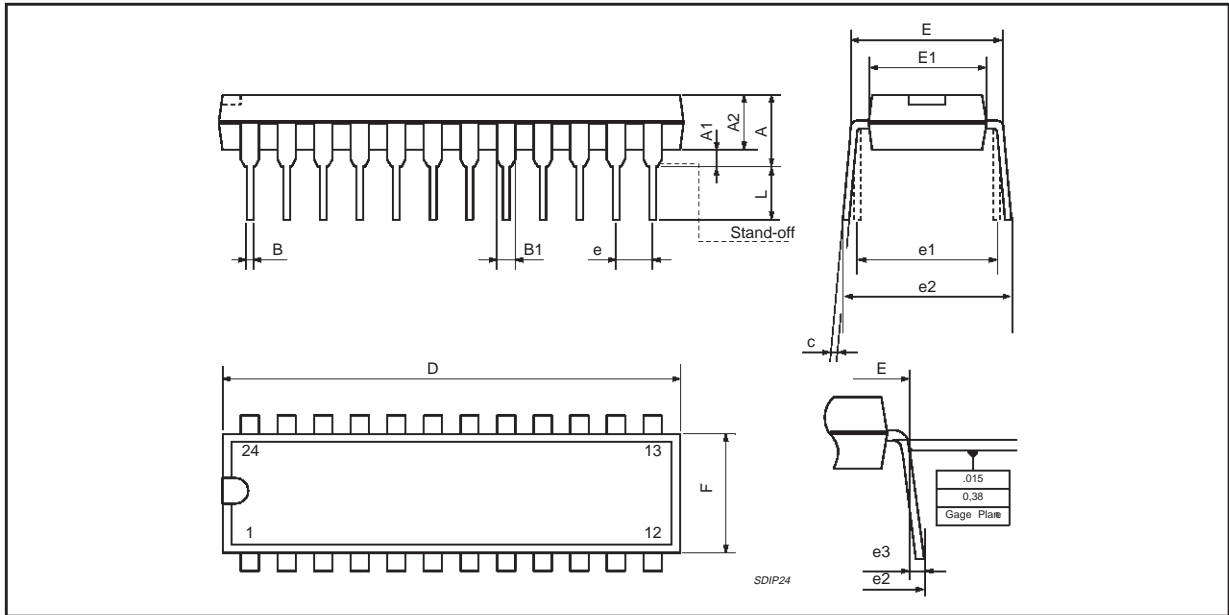
Value of LINE DURATION Register (@ 3FF0) :

LD = 16 : LD[5:0] = 010000
 LD = 32 : LD[5:0] = 100000
 LD = 48 : LD[5:0] = 110000
 LD = 63 : LD[5:0] = 111111

Table meaning :
 N = No possible capture
 Y = PLL can lock

STV9425 - STV9425B - STV9426

PACKAGE MECHANICAL DATA (STV9425- STV9425B) 24 PINS - PLASTIC SHRINK DIP

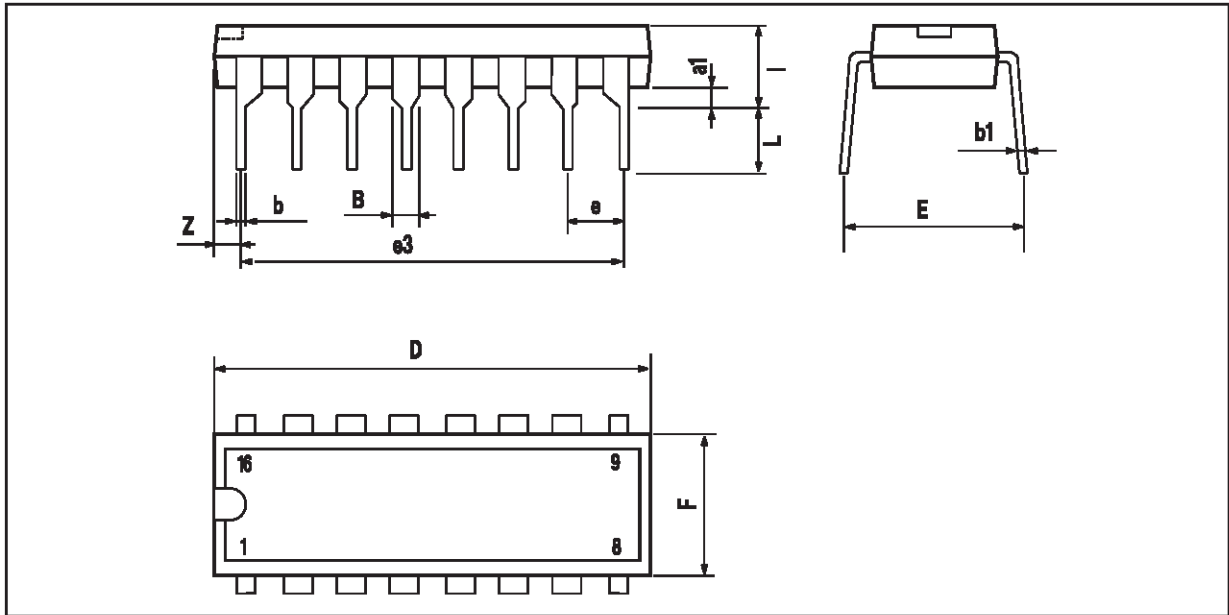


PMSDIP24.EPS

| Dimensions | Millimeters | | | Inches | | |
|------------|-------------|-------|-------|--------|--------|--------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 5.08 | | | 0.20 |
| A1 | 0.51 | | | 0.020 | | |
| B | 3.05 | 3.30 | 4.57 | 0.120 | 0.130 | 0.180 |
| B1 | 0.36 | 0.46 | 0.56 | 0.0142 | 0.0181 | 0.0220 |
| C | 0.76 | 1.02 | 1.14 | 0.030 | 0.040 | 0.045 |
| D | 0.23 | 0.25 | 0.38 | 0.0090 | 0.0098 | 0.0150 |
| E | 22.61 | 22.86 | 23.11 | 0.890 | 0.90 | 0.910 |
| E1 | 7.62 | | 8.64 | 0.30 | | 0.340 |
| e | 6.10 | 6.40 | 6.86 | 0.240 | 0.252 | 0.270 |
| e1 | | 1.778 | | | 0.070 | |
| e2 | | 7.62 | | | 0.30 | |
| e3 | | | 10.92 | | | 0.430 |
| L | | | 1.52 | | | 0.060 |
| L | 2.54 | 3.30 | 3.81 | 0.10 | 0.130 | 0.150 |

SDIP24.TBL

PACKAGE MECHANICAL DATA (STV9426)
 16 PINS - PLASTIC DIP



PM-DIP16.EPS

| Dimensions | Millimeters | | | Inches | | |
|------------|-------------|-------|------|--------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| l | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |

DIP16.TBL

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