Video Signal Driver for DVD Player
Monolithic IC MM1623XFBE

Outline

This 6ch video driver IC was developed for use in DVD players/recorders.
The LPF that attenuates the DAC noise element has a built-in switching function to handle both progressive and interlace signals. In addition, the driver structure is 6db, 75Ω x 2 lines.
Also, the number of external ESD protection diodes has been reduced thanks to the S1/S2 DC superimpose function and reinforced output pin ESD protection element.

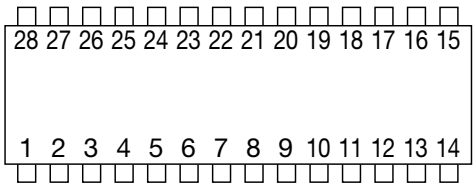
Features

1. 75W driver can drive 2 lines.
2. S/N=83dB typ.
3. Built-in 6dB amp.
4. Built-in filter switching function for progressive/interlace signal
5. Built-in high performance 4th LPF.
6. 6.75MHz/100kHz max. ±1.0dB 27MHz/100kHz typ. −40dB
7. +/− 15KV ESD for aerial discharge.
8. S1/S2 Built-in DC superimpose function.
9. Control pin allows component circuit to handle RGB signals.

Package

SOP-28

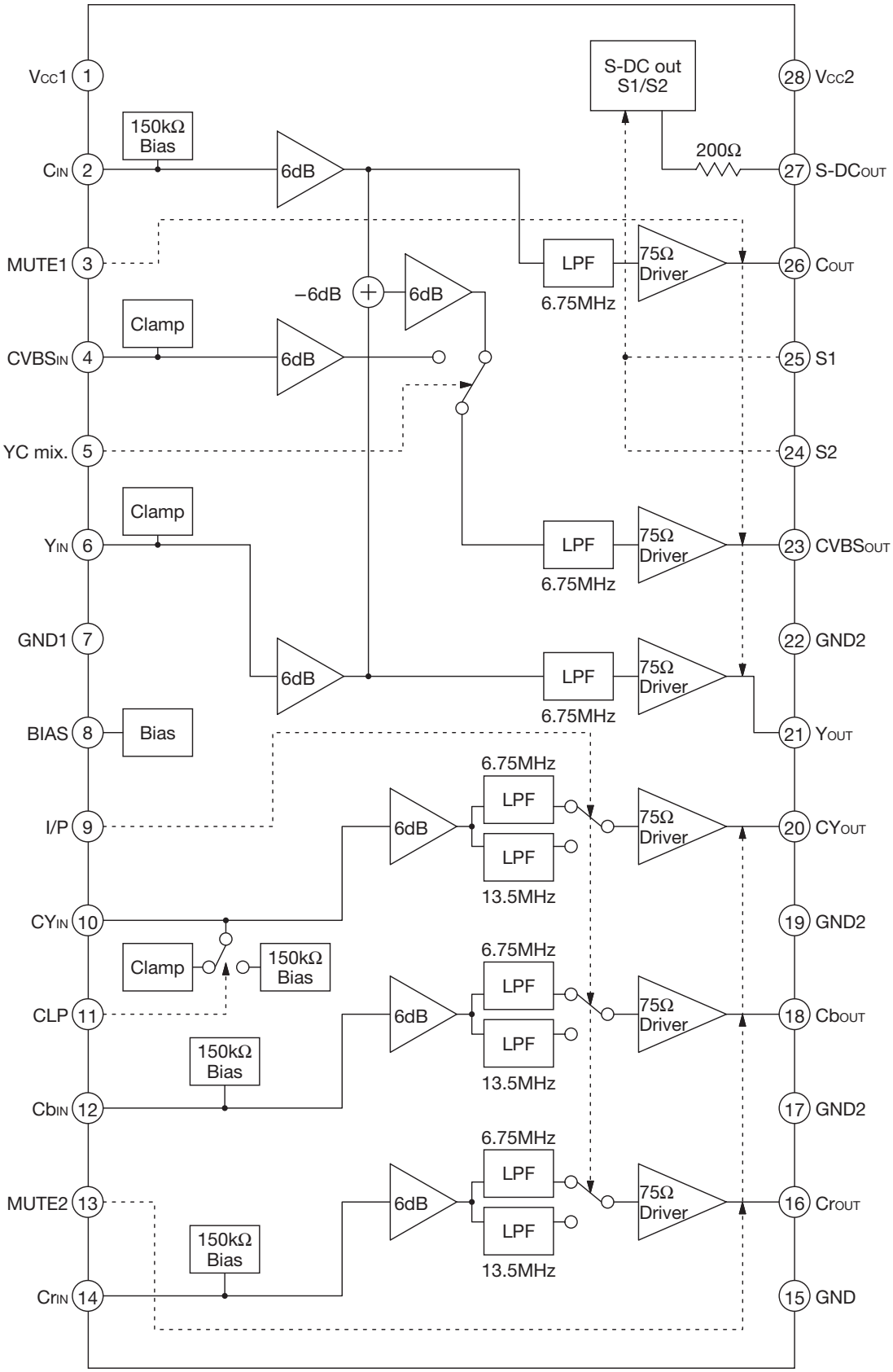
Pin Assignment



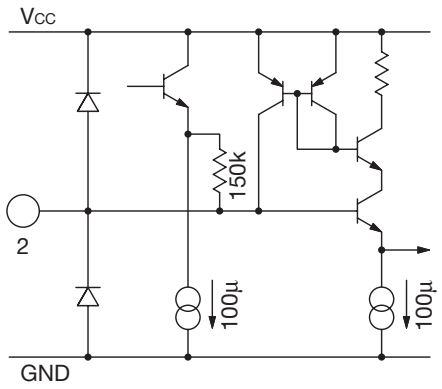
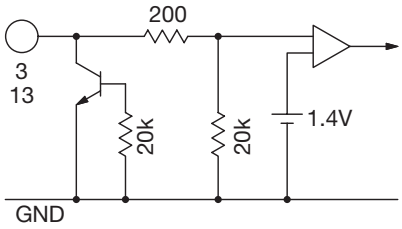
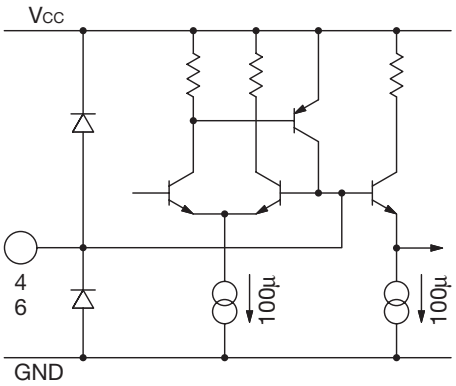
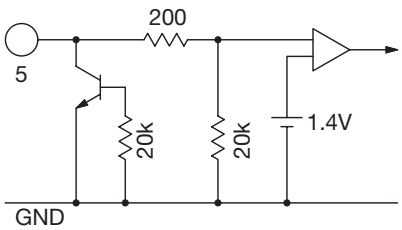
SOP-28
(TOP VIEW)

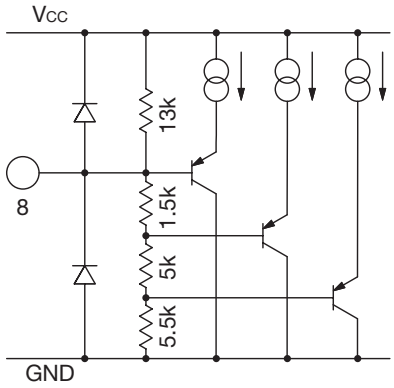
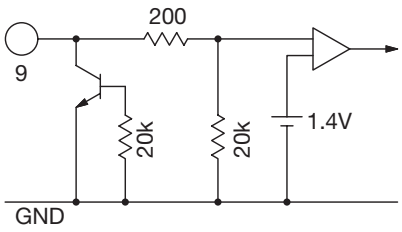
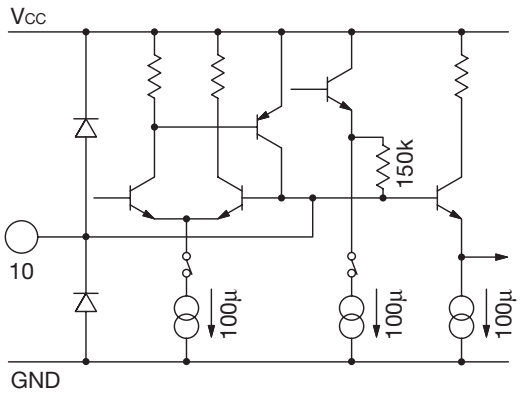
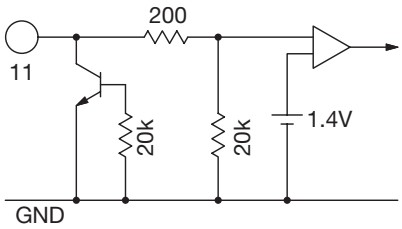
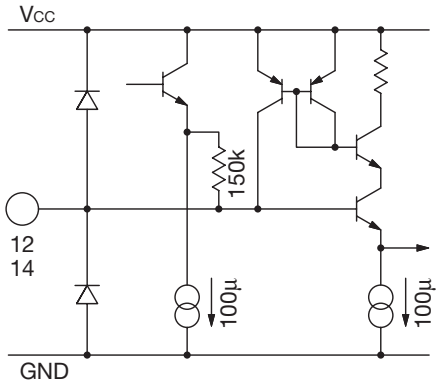
1	$V_{CC}1$	15	GND2
2	C_{IN}	16	Cr_{OUT}
3	MUTE1	17	GND2
4	$CVBS_{IN}$	18	Cb_{OUT}
5	YC MIX.	19	GND2
6	Y_{IN}	20	CY_{OUT}
7	GND1	21	Y_{OUT}
8	BIAS	22	GND2
9	I/P	23	$CVBS_{OUT}$
10	CY_{IN}	24	S2
11	CLP	25	S1
12	Cb_{IN}	26	C_{OUT}
13	MUTE2	27	S-DC_{OUT}
14	Cr_{IN}	28	$V_{CC}2$

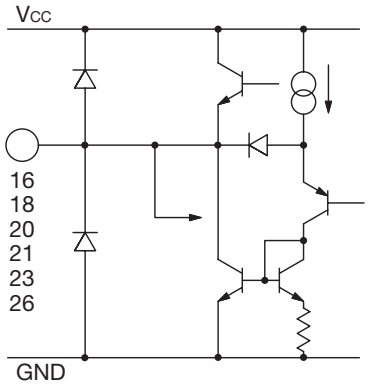
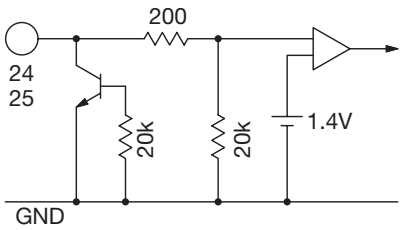
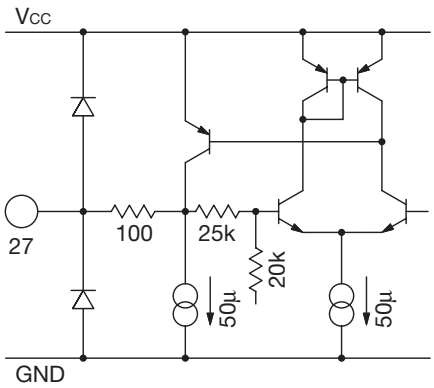
Block Diagram



Pin Description

Pin no.	Pin name	Function	Internal equivalent circuit diagram
1 28	$V_{CC}1$ $V_{CC}2$	V_{CC} $V_{CC}2$ is power supply for 75Ω driver.	
2	C_{IN}	Croma signal input	
3 13	MUTE1 MUTE2	Mute select Using of MUTE and POWER-SAVING.	
4 6	$CVBS_{IN}$ Y_{IN}	Video signal input (Composite video or Y) Sync tip clamp input	
5	YC mix.	YC MIX select	
7 15 17 19 22	GND1 GND2 GND2 GND2 GND2	GND GND2 is ground for 75Ω driver.	

Pin no.	Pin name	Function	Internal equivalent circuit diagram
8	BIAS	Bias	
9	I/P	Interlace / Progressive select	
10	CYIN	Luminance input The input can select Sync tip clamp or Bias. Input signal : Y or G	
11	CLP	Input clamp select	
12 14	CbIN CrIN	Component input Input signal : Cb or B Cr or R	

Pin no.	Pin name	Function	Internal equivalent circuit diagram
16 18 20 21 23 26	CROUT CBOUT CYOUT YOUT CVBSOUT COUT	Signal output	
24 25	S1 S2	S1/S2 select	
27	S-DCOUT	S1/S2 DC output	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	–65~+150	°C
Operating temperature	T_{OPR}	–40~+85	°C
Supply Voltage	V_{CC} max.	7	V
Allowable loss *	Pd	1.4	W

* Board mounting power dissipation. Board size 100 ×100 ×1.6mm

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	–40~+85	°C
Operating voltage	V_{CCOP}	4.5~5.5	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C,V_{CC}=5V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Supply current 1		$I_{CC}1$	No signal	77	110	143	mA
Supply current 2		$I_{CC}2$	No signal, Mute1: ON	39	56	73	mA
Supply current 3		$I_{CC}3$	No signal, Mute2: ON	39	56	73	mA
Supply current 4		$I_{CC}4$	No signal, Mute1 and Mute2: ON	1	3	5	mA
Croma input		V_{CIN}	2 PIN	1.9	2.4	2.9	V
Composite video input		V_{CVBSIN}	4 PIN	0.9	1.1	1.3	V
Luminance input		$V_{YIN, CYIN}$	6, 10 PIN	0.9	1.1	1.3	V
Component input		V_{CbIN}, $_{CrIN}$	12, 14 PIN	1.9	2.4	2.9	V
Croma output		V_{COUT}	26 PIN		2.4		V
Composite video output		$V_{CVBSOUT}$	23 PIN		1.1		V
Luminance output		$V_{YOUT, CYOUT}$	21, 20 PIN		1.1		V
Component output		V_{CbOUT}, $_{CrOUT}$	18, 16 PIN		2.4		V
Control terminal input current	H	I_{IHm} (*1)	3, 5, 9, 11, 13, 24, 25 PIN V_H=4.5V			350	µA
	L	I_{ILm} (*1)	3, 5, 9, 11, 13, 24, 25 PIN V_L=0.4V			35	µA
Control terminal input voltage	H	V_{thHm} (*1)		2.1			V
	L	V_{thLm} (*1)				0.7	V
S-DC out terminal output voltage	L	V_{DCOUTL}	R_L=10kΩ+100kΩ		0.1	0.5	V
	M	V_{DCOUTM}	R_L=10kΩ+100kΩ	1.6	2.1	2.4	V
	H	V_{DCOUTH}	R_L=10kΩ+100kΩ	4.3	4.6		V
Input impedance		$Z_{CIN, CbIN, CrIN}$	2, 12, 14 PIN	100	150	200	kΩ
Output impedance		$Z_{S-DCOUT}$	27 PIN		200		Ω
Voltage gain		$G1_n$ (*2)	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Frequency characteristic 1 (C, CVBS, Y)	$f1_{1\sim5}$ (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 6.75MHz/100kHz	–1.5	–0.5	0.5	dB
	$f2_{1\sim5}$ (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 27MHz/100kHz		–33	–27	dB
Frequency characteristic 2 (CY, Cb, Cr) at Interlace select	$f3_{6\sim8}$ (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 6.75MHz/100KHz	–0.5	0.5	1.5	dB
	$f4_{6\sim8}$ (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 27MHz/100kHz		–28	–22	dB
Frequency characteristic 3 (CY, Cb, Cr) at Progressive select	$f5_{6\sim8}$ (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 13.5MHz/100kHz	–1.5	–0.5	0.5	dB
	$f6_{6\sim8}$ (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 54MHz/100kHz		–28	–22	dB
Differential gain	$DG_{1\sim3}$ (*2)	Staircase signal 1V		1.0	1.5	%
Differential phase	$DP_{1\sim3}$ (*2)	Staircase signal 1V		1.0	1.5	°
Output dynamic range	$DR_{1,4,7,8}$ (*2)	SIN wave; 100kHz, THD=1.0%	2.6	3.0		V
	$DR_{2,3,5,6}$ (*2)	SIN wave; 100kHz, THD=1.0%	2.6	2.8		V
Crosstalk	CT_n (*2)	f=4.43MHz, 1V		–60	–55	dB
S/N1	$SN1_{4\sim8}$ (*2)	BW: 100k~6MHz		–83		dB
S/N2	$SN2_{1\sim3}$ (*2)	BW: 100k~6MHz at mix. OUT		–77		dB
Group delay 1	$t1_{GD1\sim5}$ (*2)	at 100kHz		40	80	ns
Group delay 2	$t2_{GD6\sim8}$ (*2)	Interlace select at 100kHz		35	80	ns
Group delay 3	$t3_{GD6\sim8}$ (*2)	Progressive select at 100kHz		22	50	ns
Group delay deviation 1 (C, CVBS Y)	$\Delta t1_{GD1\sim5}$ (*2)	to 3.58MHz		4	10	ns
		to 4.42MHz		6	10	ns
		to 6MHz		12	20	ns
Group delay deviation 2 (CY, Cb Cr) at Interlace select	$\Delta t2_{GD6\sim8}$ (*2)	to 1MHz		1	10	ns
		to 4MHz		4	10	ns
		to 6MHz		10	20	ns
Group delay deviation 3 (CY, Cb Cr) at Progressive select	$\Delta t3_{GD6\sim8}$ (*2)	to 2MHz		1	10	ns
		to 8MHz		4	10	ns
		to 12MHz		10	20	ns
Between channel Group delay deviation 1	$\Delta t1_{chGD}$	Between C and Y at 3.58MHz		1	10	ns
Between channel Group delay deviation 2	$\Delta t2_{chGD}$	Between CY and Cb (Cr) at 1MHz (Interlace)		1	10	ns
Between channel Group delay deviation 3	$\Delta t3_{chGD}$	Between CY and Cb (Cr) at 2MHz (Progressive)		1	10	ns

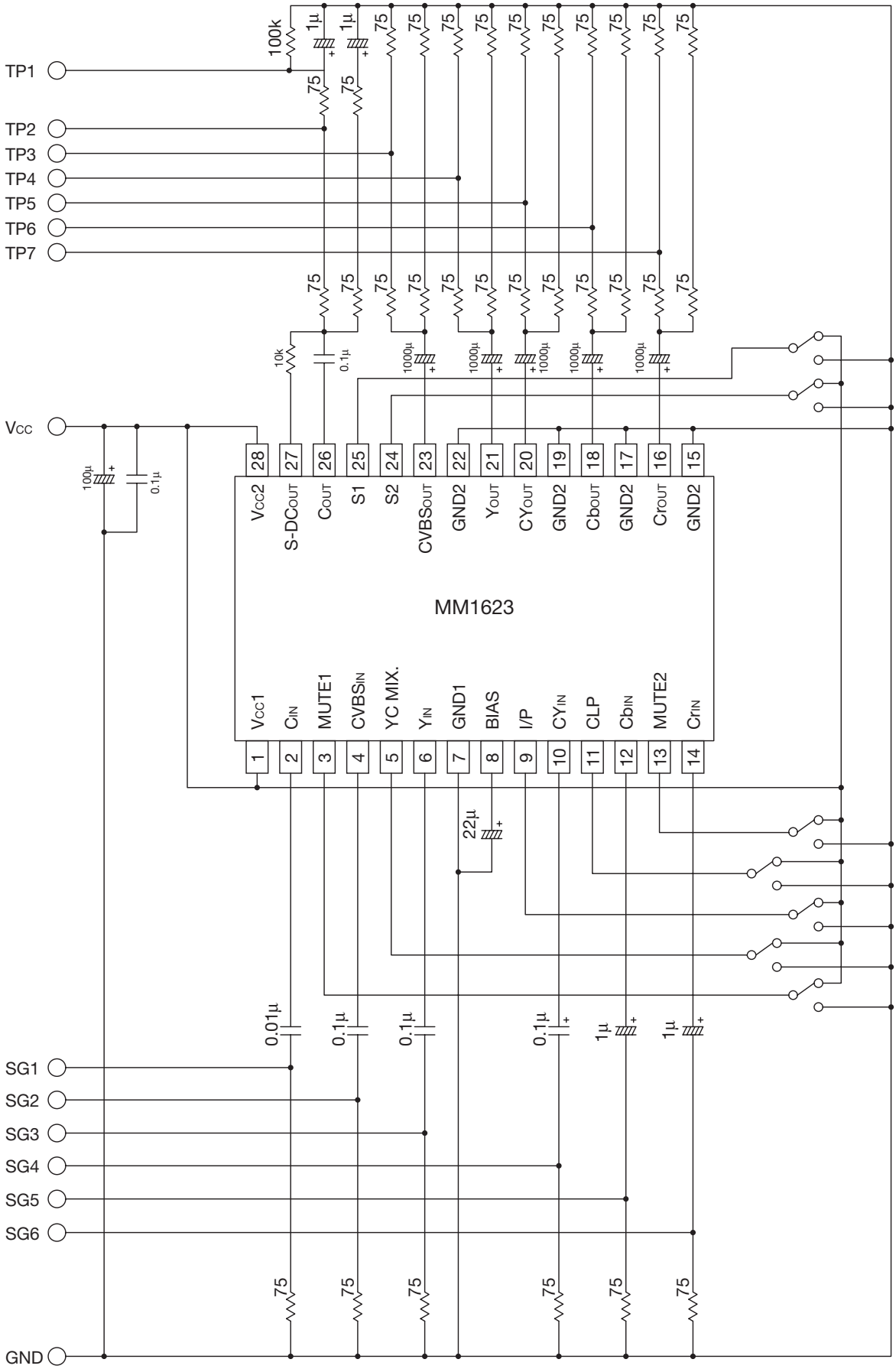
Note: *1 The subscript number "m" is the terminal of right table.

m	Terminal
1	MUTE1
2	MUTE2
3	YC mix.
4	I/P
5	CLP
6	S1
7	S2

Note: *2 The subscript number "n" is the combination of right table.

n	Input	Output
1	C_{IN}	$CVBS_{OUT}$
2	$CVBS_{IN}$	
3	Y_{IN}	
4	C_{IN}	C_{OUT}
5	Y_{IN}	Y_{OUT}
6	CY_{IN}	CY_{OUT}
7	Cb_{IN}	Cb_{OUT}
8	Cr_{IN}	Cr_{OUT}

Measuring Circuit



Switch Control Table

Input select	Output terminal	Control terminal			
		MUTE1	YC MIX.	MUTE2	CLP
MUTE	COUT	Low	*	*	*
CIN		High	*	*	*
MUTE	CVBSOUT	Low	*	*	*
YIN+CIN		High	Low	*	*
CVBSIN			High	*	*
MUTE	YOUT	Low	*	*	*
YIN		High	*	*	*
MUTE	CYOUT	*	*	Low	*
CYIN (CLAMP)		*	*	High	Low
CYIN (Bias)		*	*		High
MUTE	CbOUT	*	*	Low	*
CbIN		*	*	High	*
MUTE	CrOUT	*	*	Low	*
CrIN		*	*	High	*

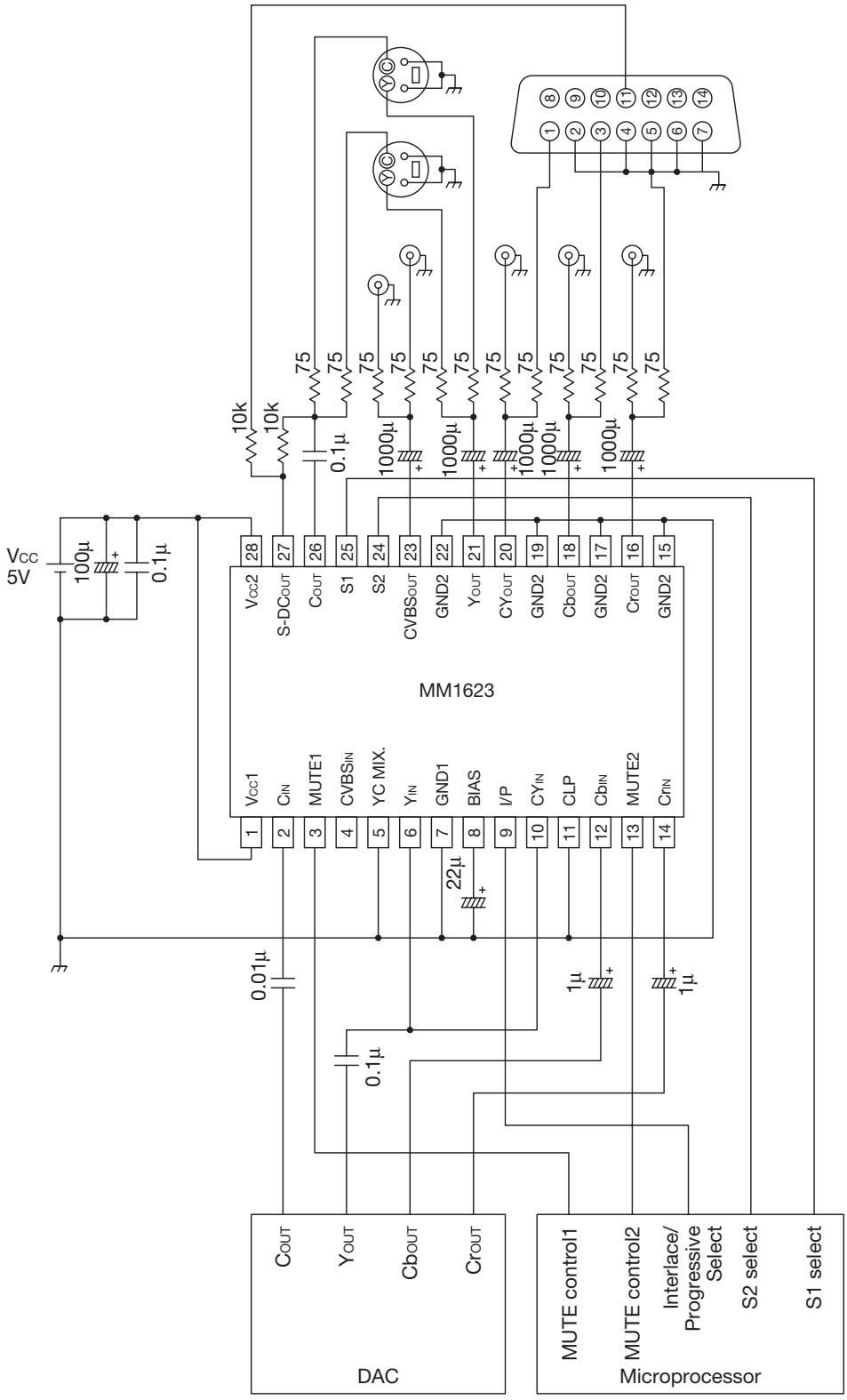
*: Don't care

Control terminal	Status	CY, Cb, Cr LPF Bandwidth
I/P	Low	13.5MHz (Progressive)
	High	6.75MHz (Interlace)

Control terminal		S-DC OUT Output Voltage	Signal Mode
S1	S2		
Low	Low	0V	4:3 Normal
Low	High	2.1V	4:3 Letter box
High	High		
High	Low	4.6V	16:9 Squeeze

*: R_L=10kΩ+100kΩ

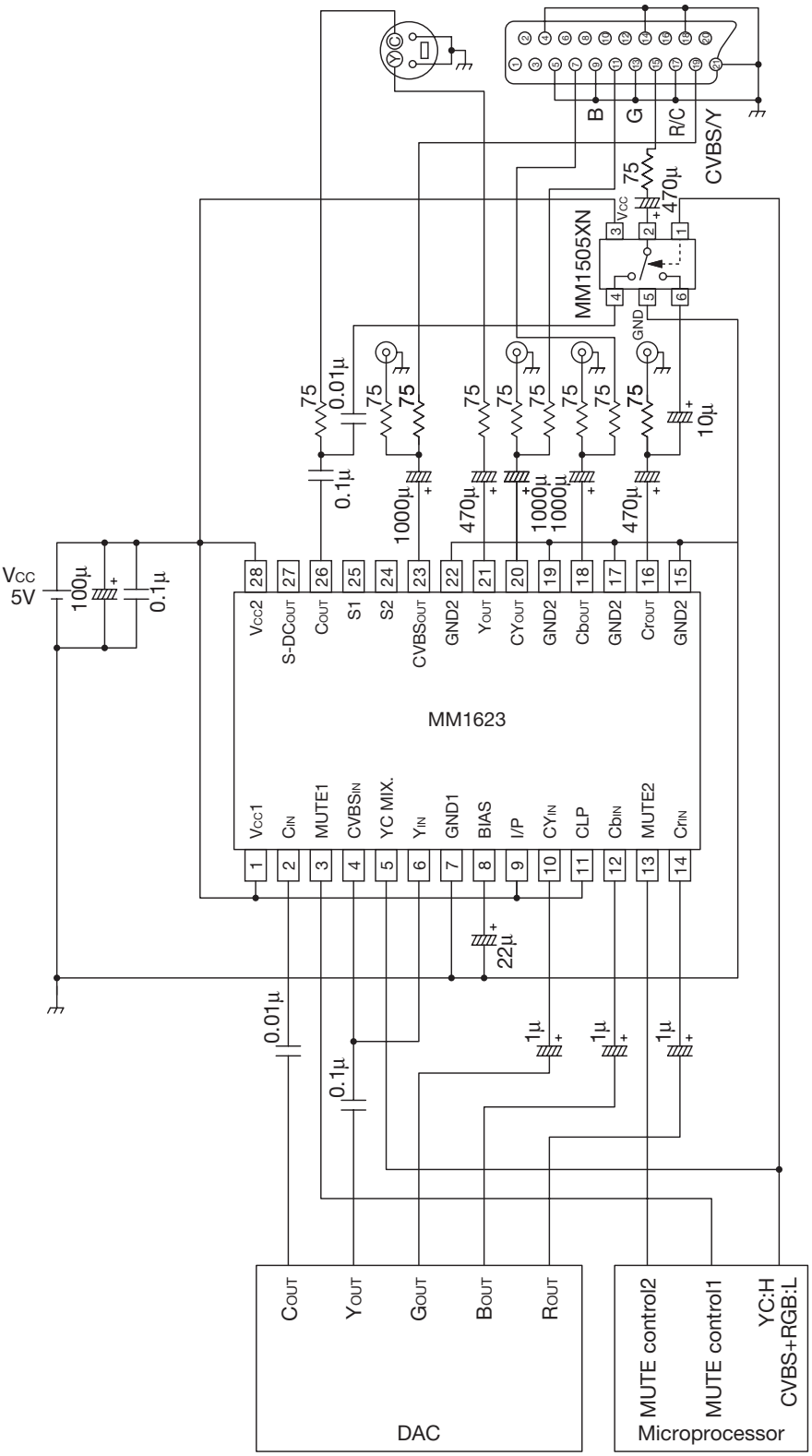
Application Circuit 1



Note 1 Please arrange power supply bypass capacitor near the $V_{CC}2$ terminal (28pin).

Note 2 Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

Application Circuit 2

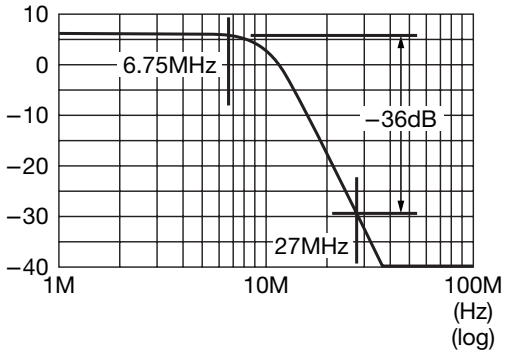


Note 1 Please arrange power supply bypass capacitor near the $V_{CC}2$ terminal (28pin).

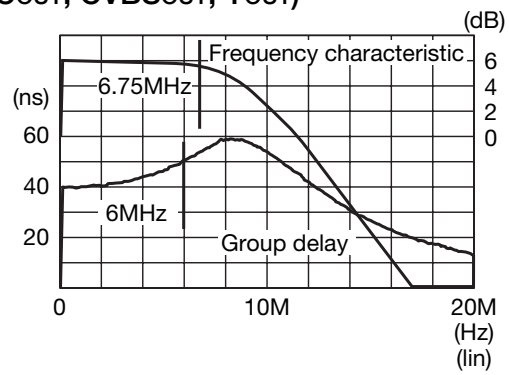
Note 2 Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

Characteristics

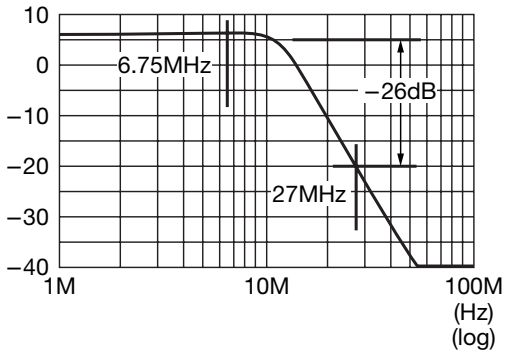
Frequency characteristic (COUT, CVBSOUT, YOUT)



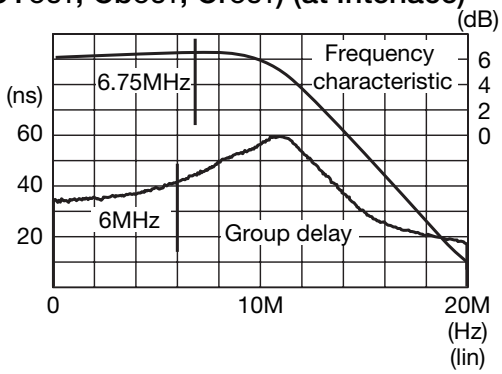
Group delay (COUT, CVBSOUT, YOUT)



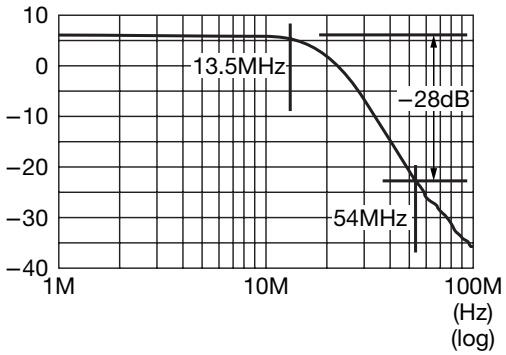
Frequency characteristic (CYOUT, CBOUT, CROUT) (at Interlace)



Group delay (CYOUT, CBOUT, CROUT) (at Interlace)



Frequency characteristic (CYOUT, CBOUT, CROUT) (at Progressive)



Group delay (CYOUT, CBOUT, CROUT) (at Progressive)