MC34014

Specifications and Applications Information

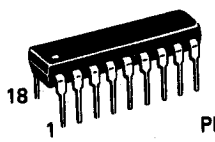
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, a dc loop interface circuit, tone dialer interface, and a regulated output voltage for a pulse/tone dialer. Also included is an equalization circuit which compensates gains for line length variations. The conversion from 2-to-4 wire is accomplished with a supply voltage as low as 1.5 volts. The MC34014 is packaged in a standard 18-pin (0.3" wide) plastic DIP and a 20-pin SOIC package.

- Transmit, Receive, and Sidetone Gains Set by External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher

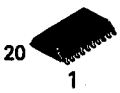
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

SILICON MONOLITHIC INTEGRATED CIRCUIT

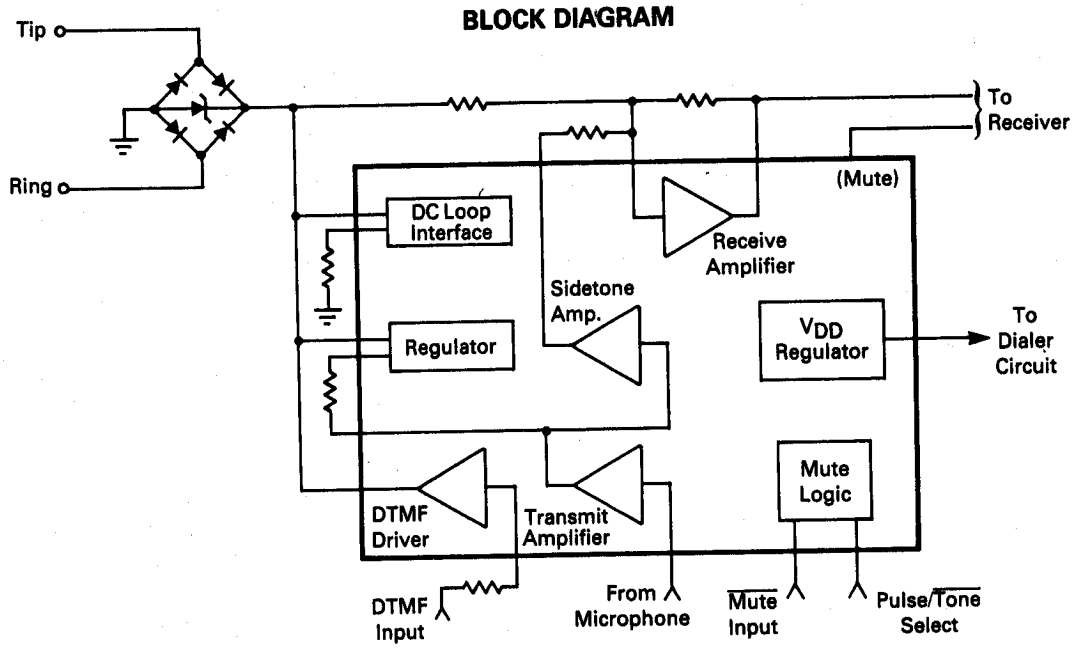


P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
SO-20L



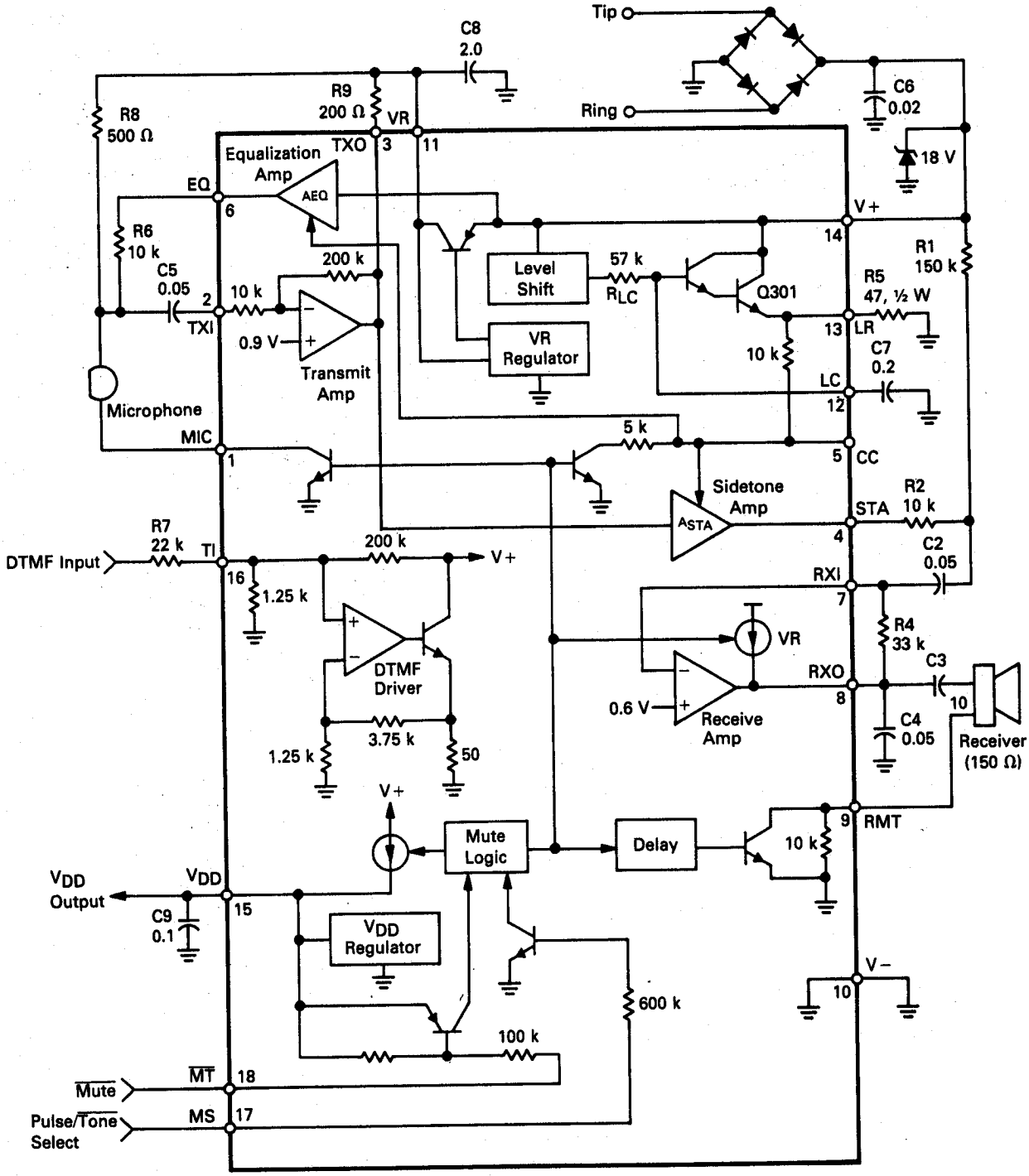
BLOCK DIAGRAM



PIN DESCRIPTION (See Figure 1)

Pin # SOIC	Pin # DIP	Name	Description
1	1	MIC	Microphone negative supply. Bias current from the electret microphone is returned to V− through this pin, through an open collector NPN transistor whose base is controlled by an internal mute signal. During dialing, the transistor is off, disabling the microphone.
2	2	TXI	Transmit amplifier input. Input impedance is 10 kΩ. Signals from the microphone are input through capacitor C5 to TXI.
3	3	TXO	Transmit amplifier output. The ac signal current from this output flows through the V_R series pass transistor via R9 to drive the line at V+. Increasing R9 will decrease the signal at V+. The output is biased at ≈0.65 V to allow for maximum swing of ac signals. The closed loop gain from TXI to TXO is internally set at 26 dB.
4	4	STA	Sidetone amplifier output. Input to this amplifier is TXO. The signal at STA cancels the sidetone signals in the receive amplifier. The signal level at STA increases with loop length.
5	5	CC	Compensation Capacitor. A capacitor from CC to ground will compensate the loop length equalization circuit when additional stability is required. In most applications, CC remains open.
7	6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feedback around the transmit amplifier. The feedback decreases with increasing loop length, causing the ac impedance of the circuit to increase.
8	7	RXI	Receive amplifier input. Input impedance is >100 kΩ. Signals from the line and sidetone amplifier are summed at RXI.
9	8	RXO	Receive Amplifier output. RXO is biased by a 2.5 mA current source. Feedback maintains the dc bias voltage at ≈0.65 V. Increasing R4 (between RXO and RXI) will increase the receive gain. C4 stabilizes the amplifier. C3 couples the signals to the receiver. The 2.5 mA current source is reduced to 0.4 mA when dialing.
10	9	RMT	Receiver Mute. The ac receiver current is returned to V− through an open collector NPN transistor and a parallel 10 kΩ resistor. The base of the NPN is controlled by an internal mute signal. During dialing the transistor is off, leaving the 10 kΩ resistor in series with the receiver.
11	10	V−	Negative supply. The most negative input connected to Tip and Ring through the polarity guard diode bridge.
12	11	VR	Regulated voltage output. The VR voltage is regulated at 1.2 V and biases the microphone and the speech circuits. An internal series pass PNP transistor allows for regulation with a line voltage as low as 1.5 V. Capacitor C8 stabilizes the regulator.
13	12	LC	DC load capacitor. An external capacitor C7 and an internal resistor form a low pass filter between V+ and LR to prevent ac signals from being loaded by the dc load resistor R5. Forcing LC to V− will turn off the dc load current and increase the V+ voltage.
14	13	LR	DC load resistor. Resistor R5 from LR to V− determines the dc resistance of the telephone, and removes power dissipation from the chip. The LR pin is biased 2.8 volts below the V+ voltage (4.5 volts in the tone dialing mode).
15	14	V+	Positive supply. V+ is the positive line voltage (from Tip & Ring) through the polarity guard bridge. All sections of the MC34014 are powered by V+.
17	15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nominal voltage of 3.3 V. The nominal output current is increased from 550 μA to 2 mA when dialing. Capacitor C9 stabilizes the regulator and sustains the V_{DD} voltage during pulse dialing.
18	16	TI	Tone input. The DTMF signal from a dialer circuit is input at TI through an external resistor R7. The current at TI is amplified to drive the line at V+. Increasing R7 will reduce the DTMF output levels. The input impedance at TI is nominally 1.25 kΩ.
19	17	MS	Mode select. This pin is connected through an internal 600 kΩ resistor to the base of an NPN transistor. A Logic "1" (>2.0 V) selects the pulse dialing mode. A Logic "0" (<0.3 V) selects the tone dialing mode.
20	8	$\overline{MT}$	Mute input. $\overline{MT}$ is connected through an internal 100 kΩ resistor to the base of a PNP transistor, with the emitter at V_{DD}. A Logic "0" (<1.0 V) will mute the network for either pulse or tone dialing. A Logic "1" (>V_{DD} − 0.3 V) puts the MC34014 into the speech mode.

FIGURE 1 — TEST CIRCUIT



NOTE: Pin numbers are for 18 pin DIP.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V−, T_A = 25°C) (See Note 1.)

Parameter	Value	Units
V+ Voltage	−1.0, +18	Vdc
V_{DD} (externally applied, V+ = 0)	−1.0, +6	Vdc
V_{LR}	−1.0, V+ − 3.0	Vdc
$\overline{MT}$, MS Inputs	−1.0, V_{DD} +1.0	Vdc
Storage Temperature	−65, +150	°C

NOTE 1: Devices should not be operated at these values. The "Recommended Operating Conditions" provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Voltage (Speech Mode) (Tone Dialing Mode)	+1.5 to +15 +3.3 to +15	Vdc Vdc
I_{TXO} (Instantaneous)	0 to 10	mA
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1) (T_A = 25°C)

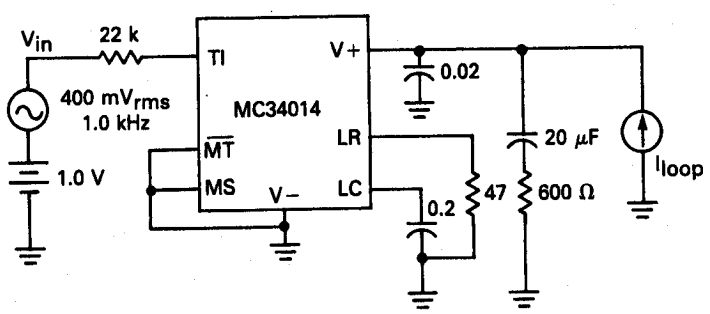
Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V+ Voltage	V+				Vdc
I_{loop} = 20 mA (Speech/Pulse Mode)		2.6	3.2	3.8	
I_{loop} = 30 mA (Speech/Pulse Mode)		3.0	3.7	4.4	
I_{loop} = 120 mA (Speech/Pulse Mode)		7.0	8.2	9.5	
I_{loop} = 20 mA (Tone Mode)		4.1	4.9	5.7	
I_{loop} = 30 mA (Tone Mode)		4.6	5.4	6.2	
V+ Current (Pin 12 Grounded)	I+				mA
V+ = 1.7 V (Speech Mode)		4.0	6.6	8.5	
V+ = 12 V (Speech/Pulse Modes)		5.5	8.4	12.5	
V+ = 12 V (Tone Mode)		6.0	8.8	14.0	
LR Level Shift (V+ − V_{LR})	ΔV_{LR}				Vdc
(Speech/Pulse Mode)		—	2.7	—	
(Tone Mode)		—	4.3	—	
LC Terminal Resistance	R_{LC}	36	57	94	kΩ
VOLTAGE REGULATORS					
VR Voltage (V+ = 1.7 V)	V_R	1.1	1.2	1.3	Vdc
Load Regulation (0 mA < I_R < 6.0 mA)	ΔV_{RLD}	—	20	—	mV
Line Regulation (2.0 V < V+ < 6.5 V)	ΔV_{RLN}	—	25	—	mV
V_{DD} Voltage (V+ = 4.5 V)	V_{DD}	3.0	3.3	3.8	Vdc
Load Regulation (0 < I_{DD} < 1.6 mA) (Dialing Mode)	ΔV_{DDLD}	—	0.25	—	Vdc
Line Regulation (All Modes) (4.0 V < V+ < 9.0 V)	ΔV_{DDLN}	—	50	—	mV
Max. Output Current (Speech Mode)	I_{DDSP}	375	550	1000	μA
Max. Output Current (Dialing Mode)	I_{DDDL}	1.6	2.0	3.6	mA
V_{DD} Leakage Current (V+ = 0, V_{DD} = 3.0 V)	I_{DDLK}	—	—	1.5	μA
SPEECH AMPLIFIERS					
Transmit Amplifier					
Gain (TXI to TXO)	A_{TXO}	—	20	—	V/V
TXO Bias Voltage (Speech/Pulse Mode)	V_{TXOSP}	0.45	0.52	0.60	x V_R
TXO Bias Voltage (Tone Mode Mode)	V_{TXODL}	VR−25	VR−5.0	—	mV
TXO High Voltage (Speech/Pulse Mode)	V_{TXOH}	VR−25	VR−5.0	—	mV
TXO Low Voltage (Speech/Pulse Mode)	V_{TXOL}	—	125	250	mV
TXI Input Resistance	R_{TXI}	—	10	—	kΩ
Receive Amplifier					
RXO Bias Voltage (All Modes)	V_{RXO}	0.45	0.52	0.60	x VR
RXO Source Current (Speech Mode)	I_{RXOSP}	1.5	2.0	—	mA
RXO Source Current (Pulse/Tone Mode)	I_{RXODL}	200	400	—	μA
RXO High Voltage (All Modes)	V_{RXOH}	VR−100	VR−50	—	mV
RXO Low Voltage (All Modes)	V_{RXOL}	—	50	150	mV

ELECTRICAL CHARACTERISTICS — (continued) (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE, RECEIVER CONTROLS					
MIC Saturation Voltage (Speech Mode, I = 500 μA)	$V_{OL_{MIC}}$	—	50	125	mV
MIC Leakage Current (Dialing Mode, Pin 1 = 3.0 V)	$I_{MIC_{LK}}$	—	0	5.0	μA
RMT Resistance (Speech Mode) (Dialing Mode)	$R_{RMT_{SP}}$ $R_{RMT_{DL}}$	— 5.0	8.0 10	15 18	Ω kΩ
RMT Delay (Dialing to Speech)	t_{RMT}	2.0	4.0	20	ms
DIALING INTERFACE					
$\overline{MT}$ Input Resistance	R_{MT}	58	100	—	kΩ
$\overline{MT}$ Input High Voltage	V_{IHMT}	V_{DD} − 0.3	—	—	Vdc
$\overline{MT}$ Input Low Voltage	V_{ILMT}	—	—	1.0	Vdc
MS Input Resistance	R_{MS}	280	600	—	kΩ
MS Input High Voltage	V_{IHMS}	2.0	—	—	Vdc
MS Input Low Voltage	V_{ILMS}	—	—	0.3	Vdc
TI Input Resistance	R_{TI}	—	1.25	—	kΩ
DTMF Gain (See Figure 2) ($V+/V_{in}$)	A_{DTMF}	3.2	4.8	6.2	dB
SIDETONE AMPLIFIER					
Gain (TXO to STA) (Speech Mode) @ V_{LR} = 0.5 V (Speech Mode) @ V_{LR} = 2.5 V (Pulse Mode) @ V_{LR} = 0.2 V (Pulse Mode) @ V_{LR} = 1.0 V	A_{STA}	 — — — —	 −15 −21 −15 −21	 — — — —	dB
STA Bias Voltage (All Modes)	V_{STA}	0.65	0.8	0.9	x V_R
EQUALIZATION AMPLIFIER					
Gain (V+ to EQ) (Speech Mode) @ V_{LR} = 0.5 V (Speech Mode) @ V_{LR} = 2.5 V (Pulse Mode) @ V_{LR} = 0.2 V (Pulse Mode) @ V_{LR} = 1.0 V	A_{EQ}	 — — — —	 −12 −2.5 −12 −2.5	 — — — —	dB
EQ Bias Voltage (Speech Mode) @ V_{LR} = 0.5 V (Pulse Mode) @ V_{LR} = 0.5 V (Speech, Pulse) @ V_{LR} = 2.5 V	V_{EQ}	 — — —	 0.66 1.3 3.3	 — — —	Vdc

NOTE: Typical values are not tested or guaranteed.

FIGURE 2 — DTMF DRIVER TEST



SYSTEM SPECIFICATIONS (T_A = 25°C) (See Figures 1–4)

Parameter		Min	Typ	Max	Unit
Tip-Ring Voltage (including polarity guard bridge drop of 1.4 V)					Vdc
(Speech Mode)	I_{loop} = 5.0 mA	—	2.4	—	
	I_{loop} = 10 mA	—	3.9	—	
	I_{loop} = 20 mA	—	4.6	—	
	I_{loop} = 40 mA	—	5.6	—	
	I_{loop} = 60 mA	—	6.6	—	
Transmit					
Gain from V_S to V+ (Figure 3) (I_{loop} = 20 mA)		28	30	31	dB
Gain change as I_{loop} is increased to 60 mA		−6.0	−4.5	−3.6	dB
Distortion		—	2.0	—	%
Output noise		—	11	—	dBrnc
Receive					
V_{RXO}/V_S (f = 1.0 kHz, I_{loop} = 20 mA) (See Figure 4)		−16	−15	−13	dB
Receive gain change as I_{loop} is increased to 60 mA		−5.0	−3.0	−2.0	dB
Distortion		—	2.0	—	%
Sidetone Level					dB
$V_{RXO}/V+$ (Figure 3)					
	I_{loop} = 20 mA	—	−36	—	
	I_{loop} = 60 mA	—	−21	—	
Sidetone Cancellation $\left[\frac{V_{RXO}}{V+}\text{ (Figure 4)}\right]$ dB − $\left[\frac{V_{RXO}}{V+}\text{ (Figure 3)}\right]$ dB I_{loop} = 20 mA		20	26	—	dB
DTMF Driver		3.2	4.8	6.2	dB
$V+/V_{in}$ (Figure 2)	I_{loop} = 20 mA				
AC Impedance					Ω
Speech mode (incl. C_6, See Figure 4)	I_{loop} = 20 mA	—	750	—	
$Z_{ac} = (600)V+/(V_S - V+)$	I_{loop} = 60 mA	—	300	—	
Tone mode (including C_6)	20 mA < I_{loop} < 60 mA	—	1650	—	

NOTE: Typicals are not tested or guaranteed.

FIGURE 3 — TRANSMIT AND SIDETONE LEVEL TEST

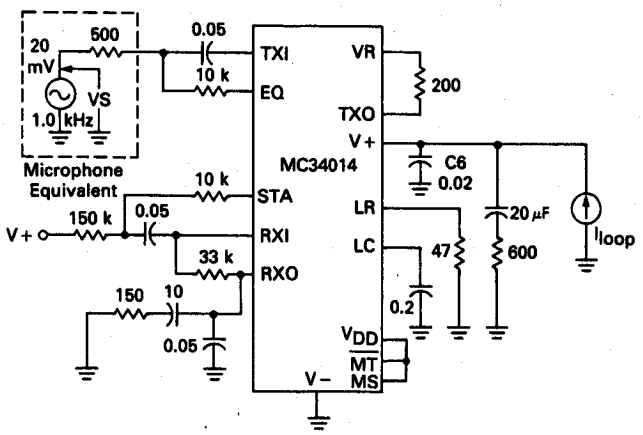
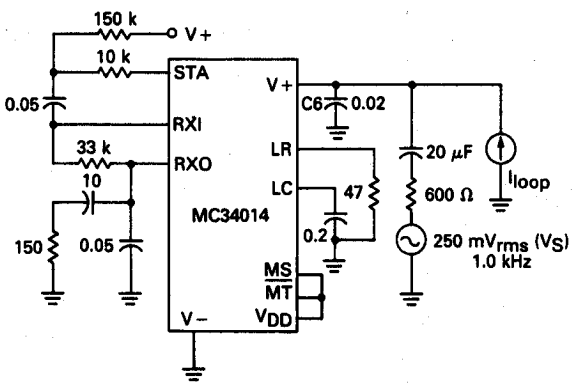


FIGURE 4 — AC IMPEDANCE, RECEIVE AND SIDETONE CANCELLATION TEST



DESIGN GUIDELINES (Refer to Figure 1)

INTRODUCTION

The MC34014 is a speech network meant for connection to the Tip & Ring lines through a polarity guard bridge. The circuit incorporates four amplifiers: transmit, receive, sidetone, and equalization. Some parameters of each amplifier are set by external components, and in addition, the gains of the sidetone and equalization amplifiers vary with loop current.

The line interface portion determines the dc voltage versus loop current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing, and tone (DTMF) dialing. When switching to either dialing mode some parameters of the various sections are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

TABLE 1 — OPERATING PARAMETERS AS A FUNCTION OF OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift ($V+ - V_{LR}$)	2.7 V	2.7 V	4.3 V
V_{DD} Source Current	550 μA	2.0 mA	2.0 mA
Transmit Amplifier	Functional	Functional	Inoperative
MIC Switch (Pin 1)	On	Off	Off
Equalization Amplifier	See Transfer Curves — Figure 8		
Sidetone Amplifier	See Transfer Curves — Figure 6		
Receive Amplifier Output Current	2.5 mA	400 μA	400 μA
RMT (Pin 9) Impedance	8.0 Ω	10 kΩ	10 kΩ
DTMF Amplifier	Inoperative	Inoperative	Functional
CC Voltage	$V_{LR}/3$	V_{LR}	V_{LR}

DC LINE INTERFACE (Figure 5)

The dc line interface circuit (Pins 10, 12–14) sets the dc voltage characteristics with respect to the loop current. The loop current enters at Pin 14 where the internal circuitry of the MC34014 draws 5–6 mA. Pin 3 sinks (typically) 3 mA through R_9. The remainder of the loop current is passed through Q_{301} and R_5. The resulting voltage across the entire circuit is therefore equal to the voltage across R_5, plus the level shift voltage from Pin 13 (LR) to Pin 14 (V+), nominally 2.7 volts in the speech and pulse modes. In the tone mode, the level shift increases to 4.3 volts, the internal current changes slightly (Figure 6), and the current required at Pin 3 decreases to near zero. These changes increase the equivalent dc resistance of the circuit, raising the voltage at V+ to ensure adequate voltage at V_{DD} for the external tone dialer. See Figure 7 for typical voltage versus loop current characteristics.

Capacitor C_7 at Pin 12 provides high frequency rolloff (above 10 Hz) so that R_5 does not load down the speech and DTMF signals.

The voltage at V_R is an internally regulated 1.2 volt supply which provides the bias currents for the microphone and the transmit amplifier output (Pin 3), as well as internal bias for the various amplifiers. Capacitor C_8 stabilizes the regulator. The use of an (internal) PNP transistor allows V_R to be regulated with a V+ voltage as low as 1.5 volts.

FIGURE 5 — DC LINE INTERFACE

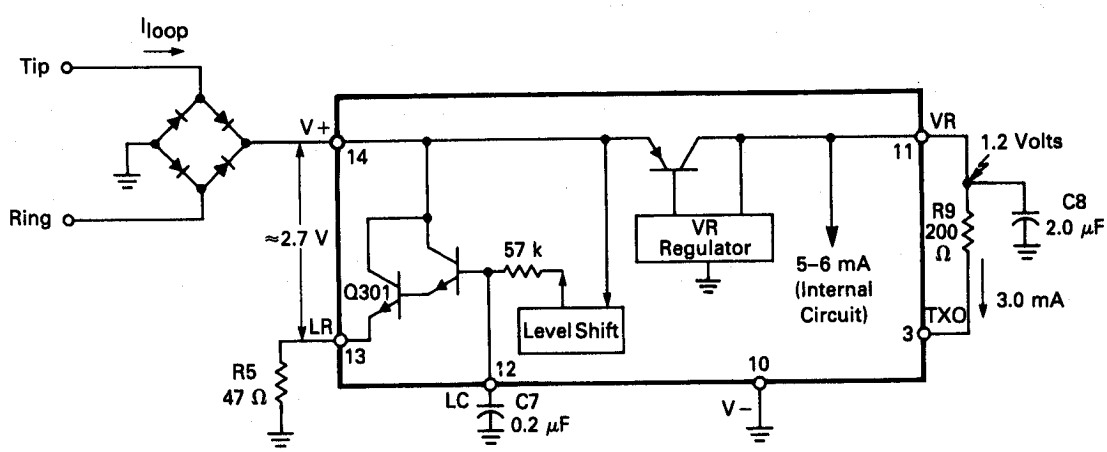


FIGURE 6 — INTERNAL CURRENT versus VOLTAGE

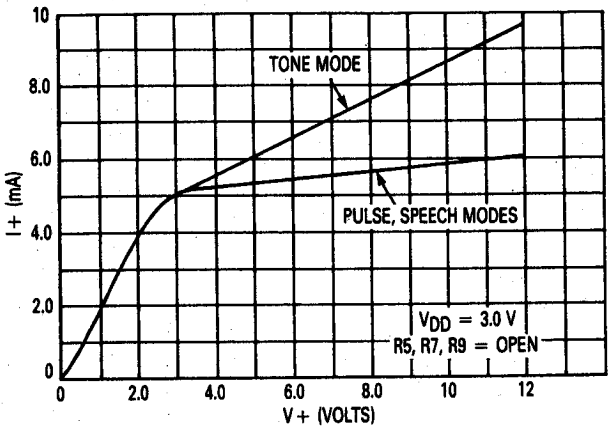
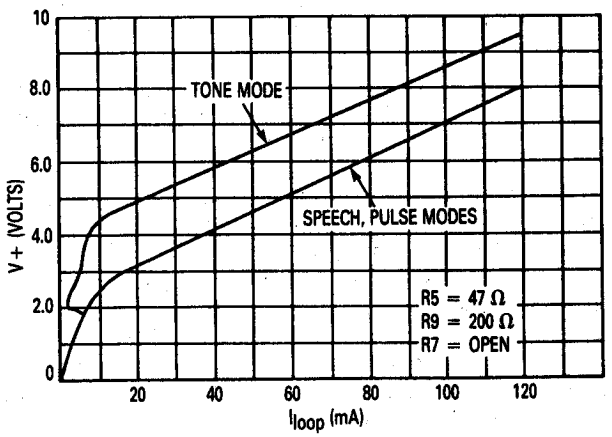


FIGURE 7 — CIRCUIT VOLTAGE versus LOOP CURRENT



TRANSMIT AMPLIFIER

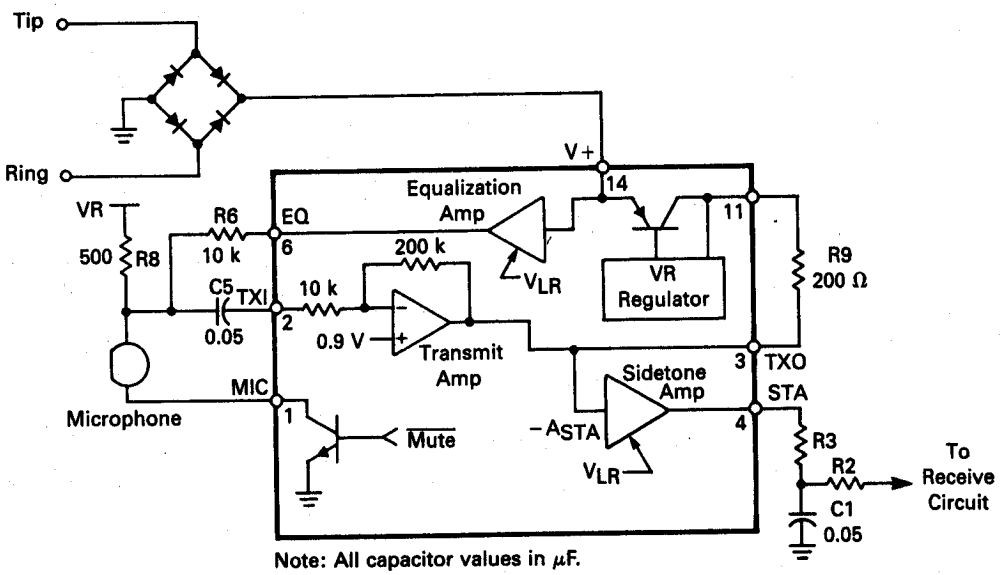
The transmit amplifier (from TXI to TXO) is inverting, with a fixed internal gain of 20 V/V (26 dB), and a typical input impedance of 10 kΩ (Figure 8). The input bias currents are internally supplied, allowing capacitive coupling of the microphone signals to the amplifier.

In the speech and pulse modes, the dc bias level at TXO is typically 0.52 x VR (≈0.63 V), which permits the output to swing 0.55 volts in both positive and negative directions without clipping. The ac voltage signal at TXO (the amplified speech signal) is converted to an ac current by Rg. The ac current passes through the VR series pass transistor to V+, modulating the loop current. The voltage signal at V+ is out of phase with the signal at TXI.

In the tone dialing mode, the TXO dc bias level is clamped at approximately VR-10 mV, rendering the amplifier inoperative. This action also reduces the TXO bias current from 3.0 mA to less than 125 μA.

MIC (Pin 1) is connected to an open-collector NPN transistor, and provides the ground path for the microphone bias current. In either dialing mode, the transistor is off, disabling the microphone.

FIGURE 8 — TRANSMIT SECTION



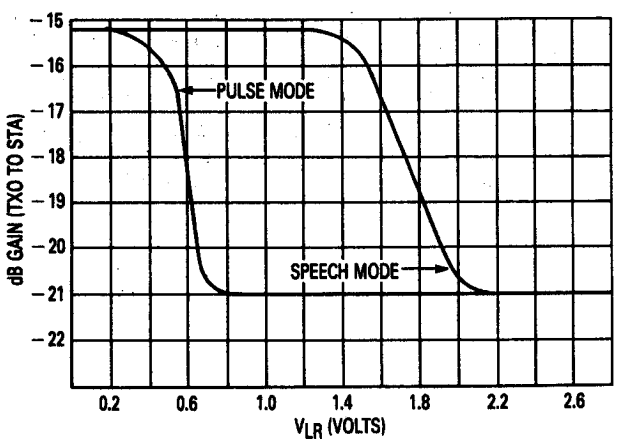
Note: All capacitor values in μF.

SIDETONE AMPLIFIER

The sidetone amplifier provides inversion of the TXO signal for the reduction of the sidetone signal at the receive amplifier (Figure 8). Resistors R_2 and R_3 determine the amount of sidetone cancellation. Capacitor C_1 provides phase shift to compensate for the phase shift created by the complex impedance of the Tip & Ring lines.

The gain of the sidetone amplifier varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −15 dB (0.17 V/V) at low loop currents, and the minimum gain is −21 dB (0.09 V/V) at high loop current (see Figure 9 for transfer curves). For example, using 47 Ω for R_5, the gain would begin to decrease at ≈30 mA, and would stop decreasing at ≈57 mA (speech mode). The dc bias voltage at STA (Pin 4) changes slightly (≈50 mV) with variations in loop current. The output is inverted from TXO, which is the input to this amplifier. Since the transmit amplifier is inoperative in the tone dialing mode, the sidetone amplifier is also inoperative in that mode.

FIGURE 9 — SIDETONE AMPLIFIER GAIN



RECEIVE AMPLIFIER

The gain of the receive amplifier (from V+ to RXO) is determined according to the following equation (refer to Figure 10):

$$\frac{V_{RXO}}{V+} = \frac{R_4}{R_1} + \frac{(X_C//R_2)\,(A_{EQ})\,(A_{TXO})\,(A_{STA}) \times R_A \times R_4}{((X_C//R_2)+R_3)\,(R_A+R_6) \times R_2}$$

Where $R_A = R_8//10\ k\Omega$ (10 kΩ = R_{in} of T_X Amp)
A_{EQ} = Gain of Equalization Amp
A_{TXO} = Gain of Transmit Amp (20 V/V)
A_{STA} = Gain of sidetone Amp
X_C = Impedance of C_1 at frequency of interest

The waveform at STA (Pin 4) is in phase with that at V+ (for receive signals), hence the plus sign between the terms. Due to the variations of A_{EQ} and A_{STA} with loop current, the receive gain will vary by ≈1.5 dB. If capacitor C_1 is not used, the above equation is simplified by deleting the terms containing X_C.

The output at RXO is inverted from V+ in the receive mode. In the transmit mode, the V+-to-RXO phase relationship depends on the amount of sidetone cancellation (determined by R_2 and R_3 and C_1), and can vary from 0° to 180°.

In the speech mode, the output current capability (at RXO) is typically 2.0 mA. In either dialing mode, the current capability is reduced to 400 μA in order to reduce internal current consumption. This feature is beneficial when this device is used in conjunction with a line-powered speakerphone circuit, such as the MC34018, where the majority of the loop current is needed for the speakerphone.

RMT (Pin 9) is the return path for the receiver's ac current. This pin is internally connected to an open collector NPN transistor, paralleled by a 10 kΩ resistor. In the speech mode, the transistor is on, providing a low impedance from RMT to ground. In either dialing mode, the transistor is off, muting the receive signal. This prevents loud "clicks" or loud DTMF tones from being heard in the receiver during dialing. When switching from either dialing mode to the speech mode ($\overline{MT}$ switches from low to high), the RMT pin switches back to a low impedance after a delay of 2–20 ms. The delay reduces clicks in the receiver associated with switching from the dialing to speech mode.

EQUILIZATION AMPLIFIER

The equalization amplifier gain varies with loop current, and is configured in the circuit so as to cause a variation of the network ac impedance (when looking in from the Tip & Ring lines). The gain varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −2.5 dB (0.75 V/V) at high loop current, and the minimum gain is −12 dB (0.25 V/V) and low loop current (see Figure 11 for transfer curve). For example, using 47 Ω for R_5, the gain would begin to increase at ≈30 mA, and would stop increasing at ≈57 mA (speech mode). The output signal is in phase with the signal at V+, which is the input to this amplifier.

The dc bias level at EQ (Pin 6) varies with the voltage at LR (Pin 13) according to the curve of Figure 12. In most applications, this level shift is of little consequence, and may be ignored. If a particular circuit configuration should be sensitive to the shift, however, the output signal at EQ may be ac coupled to the rest of the circuit.

The equalization amplifier remains functional in all three modes, although in the tone mode, its function has no consequence when the circuit is configured as shown in Figure 1.

V_{DD} REGULATOR

The V_{DD} regulator is a shunt type regulator which supplies a nominal 3.3 volts for external dialers, and/or

other circuitry. In the speech mode, the output current capability at Pin 15 is typically 550 μA. In either dialing mode, the current capacity is increased to 2.0 mA.

V_{DD} will be regulated whenever V+ is >300 mV above the regulated value. As V+ is lowered, and the internal pass transistor becomes saturated, the circuit steers current away from the external load through an internal current source, in order that the V_{DD} capacitor (C9) does not load down speech and DTMF signals at V+. As V+ is lowered below 1 volt, Pin 15 switches to a high impedance state to prevent discharging of any storage capacitors, or batteries used for memory retention.

The V_{DD} voltage is unaffected by the choice of operating mode.

DIALER INTERFACE

The dialer interface consists of the mode control pins, $\overline{MT}$ and MS (Pins 18 and 17), and the DTMF current amplifier.

The $\overline{MT}$ pin, when at a Logic "1" (> V_{DD} − 0.3 V), sets the circuit into the speech mode, independent of the state of the MS pin. When the $\overline{MT}$ pin is at a Logic "0" (< 1.0 V), the dialing mode is determined by the MS pin. When MS is at a Logic "1" (> 2.0 V), the circuit is in the pulse dialing mode, and when at a Logic "0" (< 0.3 V) the tone (DTMF) mode is in effect.

The input impedance of the $\overline{MT}$ pin is typically 100 kΩ, with the input current flowing out of the pin (from V_{DD}). The input impedance of the MS pin is typically 600 kΩ, and the input current flows into the pin (Figure 1).

The DTMF amplifier (Figure 13) is a current amplifier which transmits DTMF signals to the V+ pin, and consequently onto the Tip & Ring lines. Waveforms from a DTMF dialer are input at TI (Pin 16) through a current limiting resistor (R_7). Negative feedback around the amplifier reduces the overall gain so that return loss specifications may be met. The voltage gain is calculated using the following equation:

$$\frac{V+}{V_i} = \frac{80\ R_E}{(1\ +\ 0.795R_7\ +\ 0.4R_ER_7)}$$

(R_E, R_7 in kΩ)
where $R_E = R_L//2$ kΩ (2 kΩ = internal dynamic impedance)

Using 22 kΩ for R_7, and 600 Ω for R_L, the voltage gain is a nominal 4.3 dB. The minimum loop current at which the circuit of Figure 1 will operate without distortion is 12 mA.

The DTMF amplifier is functional only in the tone dialing mode, and the waveform at V+ is inverted from that at TI. The TI pin requires a dc bias current (into the pin) of 20–50 μA, which may be supplied by the Tone dialer circuit, or by using the biasing scheme of Figure 14.

CC (PIN 5)

The CC pin (Compensation Capacitor) has two functions: 1) to provide equalization loop stability where the normal stabilizing components are ineffective; and 2) to allow optional control of the equalization functions.

In most applications, the capacitor at LC (Pin 12) provides the required stability, and no further compensation is required. In applications where changes are forced at Pin 12 and/or 13 (e.g., see Figure 23), the LC capacitor's effectiveness may be lost. The addition of a 10 μF capacitor to Pin 5 will provide the required additional compensation.

The CC pin may be used to force the loop length compensation circuits to specific modes. Grounding CC will set the sidetone and equalization amplifiers at the low loop current values. Connecting CC to V_R will set the amplifiers at the high loop current values.

Variations in the curves of Figures 9 and 11 may be obtained by using external resistors from LR to CC, and from CC to V−.

FIGURE 10 — RECEIVE CIRCUIT

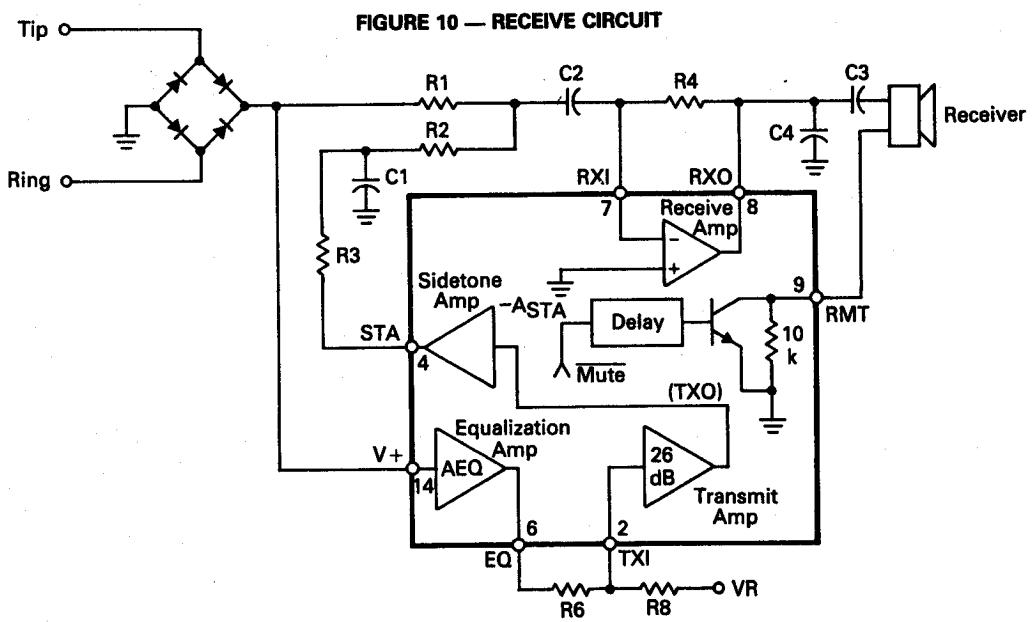


FIGURE 11 — EQUALIZATION AMPLIFIER GAIN

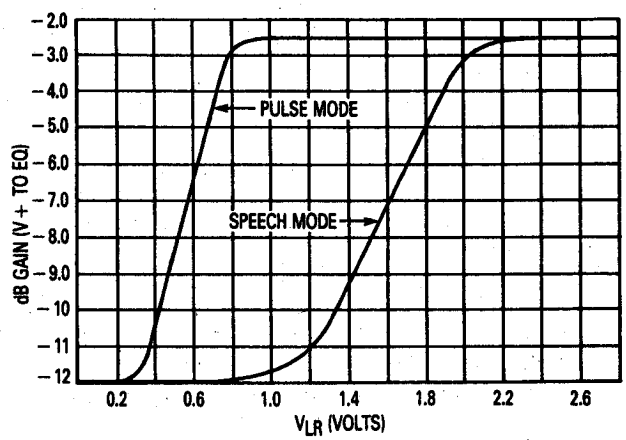


FIGURE 12 — EQ (PIN 6) DC VOLTAGE

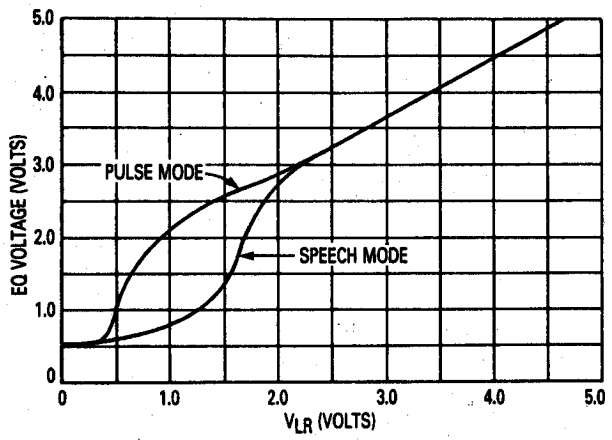


FIGURE 13 — DTMF TONE DIALER

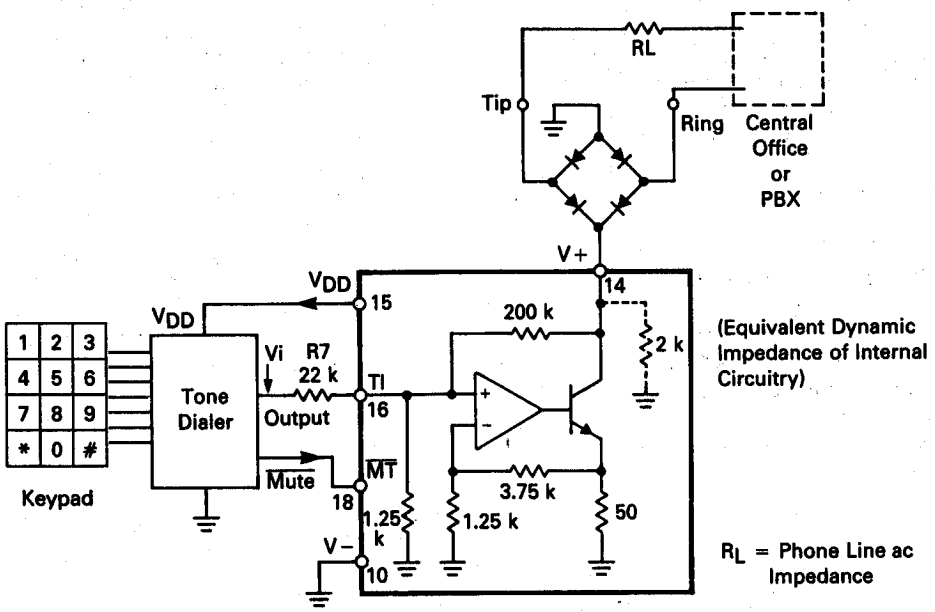
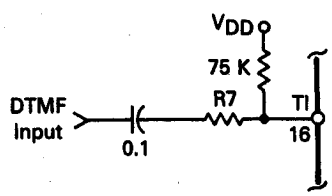


FIGURE 14 — INPUT BIASING



APPLICATIONS INFORMATION

AC IMPEDANCE

One of the basic problems with early telephones is that the performance varied with different line lengths (distance from the Central Office to the telephone). If a particular phone were optimized for short loops and then connected to a long loop, both the transmitted and receive signals would be difficult to hear. On the other hand, phones optimized for long loops would then be annoyingly loud on short loops. The process of equalization is one whereby the performance is forced to vary with loop length inversly to the expected variations. Monitoring of loop length is accomplished by monitoring the loop current at the telephone. In the MC34014, loop length equalization is provided by varying the ac impedance of the telephone circuit. In this manner the MC34014 mimics a passive network, with varistors providing the equalization.

Figure 15 depicts the situation in the receive mode. The receive signal coming from the Central Office is V_S and is independent of the loop length. Z_R is the ac impedance of the Central Office, nominally 900 Ω. Z_L is the characteristic impedance of the phone line, and is a nominal 600 Ω. The signal applied to the line (V_1) is therefore a portion of V_S. That signal is attenuated by the distributive impedance of the phone line, with a resulting signal V_2 at the telephone. The amplitude of V_2 depends on the amount of attenuation, the impedance of the phone line at the telephone and the ac impedance of the telephone (Z_{ac}), according to:

$$V_2 = \frac{V_1' \times Z_{ac}}{Z_{ac} + Z_L}$$

where V_1' is the equivalent signal source at the receive end of the phone line, providing the signal V_2 through the impedance equal to the characteristic impedance of the line (Z_L). The value of V_1' depends on how much V_1 has been attenuated by the length of phone line. By increasing Z_{ac} on long loops, V_2 is a greater portion of V_1', resulting in a stronger receive signal at the telephone.

FIGURE 15 — RECEIVE MODE

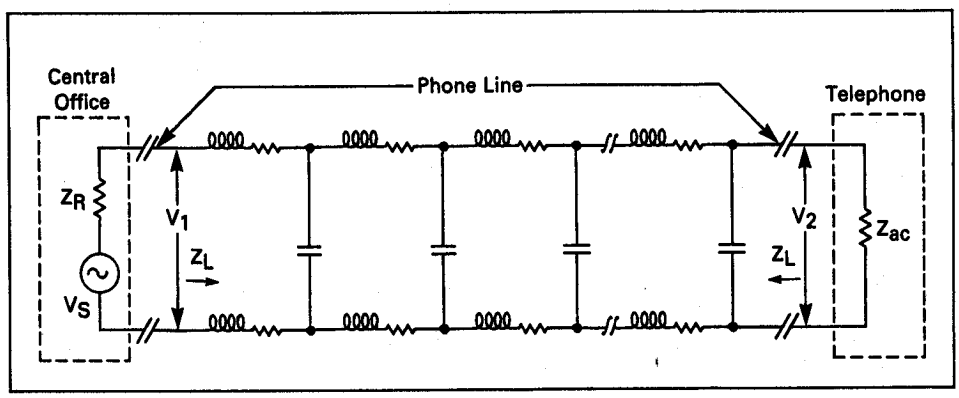
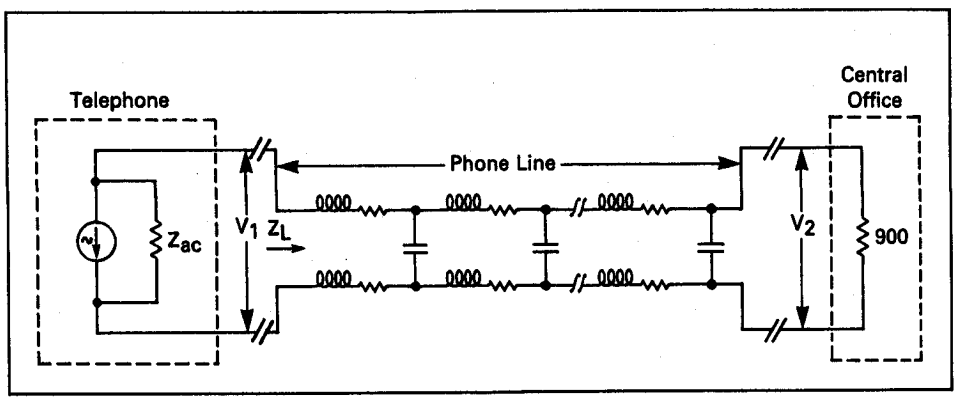


Figure 16 depicts the situation in the transmit mode. In this mode, the MC34014 is an ac current source, with a finite output impedance, modulating the loop current. The voltage signal V_1 is therefore equal to the ac signal current acting on Z_{ac} in parallel with the characteristic impedance of the phone line (Z_L). The signal is attenuated by the distributive impedance of the phone line, and so only a portion of that signal (V_2) appears at the Central Office. By increasing Z_{ac} on long loops, V_1 is increased, resulting in a higher signal level at V_2.

FIGURE 16 — TRANSMIT MODE



The ac impedance of the telephone circuit is determined by the transmit amplifier, equalization amplifier, and external resistors R_6, R_8, and R_9. In Figure 17, a portion of the receive signal at V+ appears at EQ. That signal is reduced at TXI by the R_8-R_6 divider (the electret microphone is a high impedance). The signal at TXI is then amplified by 20, and that signal (at TXO) is converted to an ac current by R9. The ac impedance of the circuit is therefore $V+/I_{TXO}$, and is defined by the following equation:

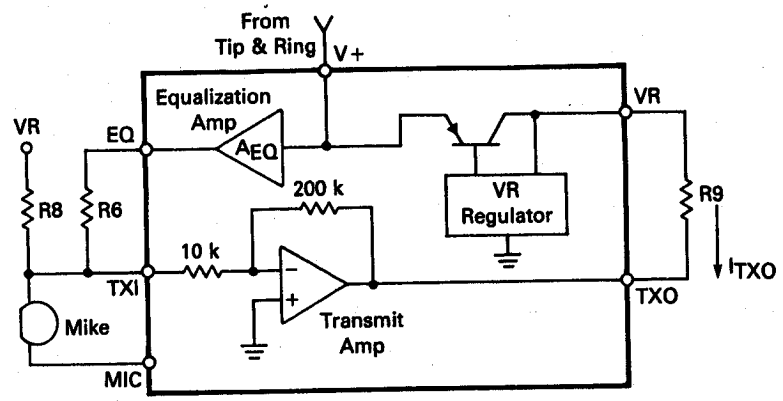
$$Z_{ac} = \frac{(1 + R_8/R_6)(R_9)}{20 \times A \times (R_8/R_6)}$$

where A = the gain of the equalization amplifier (0.25 to 0.75)

Since the gain of the equalization amplifier varies by a factor of 3, the ac impedance will vary the same amount. Using the resistor values indicated in Figure 1, the ac impedance will vary from 280 Ω (short loop) to 840 Ω (long loop).

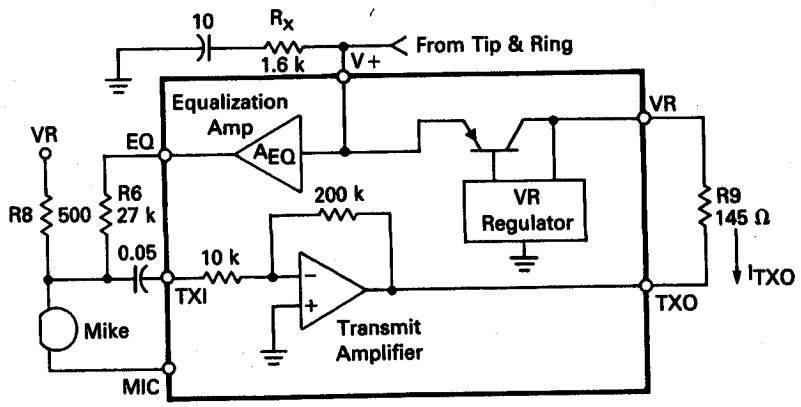
When calculating or measuring the ac impedance, capacitor C_6 (≈8.0 kΩ at 1.0 kHz) and the dynamic impedance of the MC34014 (≈10 kΩ) must be taken into account. If the microphone has an impedance lower than that of a typical electret, then its dynamic impedance must be accounted for in the above equation.

FIGURE 17 — DETERMINING AC IMPEDANCE



If a variation in Z_{ac} of less than 3:1 is desired, the circuit configuration of Figure 18 may be used. The ac impedance is the parallel combination of R_X and the impedance presented by the remainder of the circuit. With the values shown in Figure 18, the ac impedance varies from 400 Ω to 800 Ω.

FIGURE 18 — REDUCED AC IMPEDANCE VARIATION



TRANSMIT DESIGN PROCEDURE

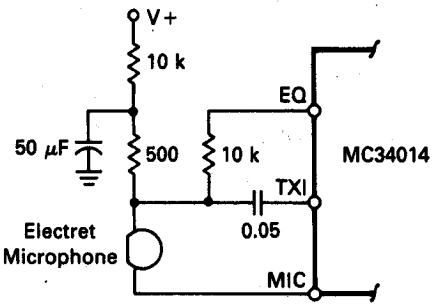
Referring to Figure 17, first select R_9 for the desired maximum output level at Tip & Ring, assuming a signal level at TXO of 1.0 V p-p. The maximum signal level at Tip & Ring will be approximately:

$$\frac{(V_{TXO})\ (Z_L)}{R_9}$$

where Z_L is the characteristic ac impedance of the phone line. Capacitor C_6 and the ≈10 kΩ dynamic impedance of the MC34014 must also be considered in the above computation, since they are in parallel with Z_L.

The next step is to select the R_6/R_8 ratio, according to the required Z_{ac}, using the equation on the previous page. Then R_8 is selected to set the microphone sensitivity. R_8 is typically in the range of 0.5 k to 1.5 kΩ, and is dependent on the characteristics of the microphone. R_6 is then calculated from the above mentioned ratio.

FIGURE 19 — ALTERNATE MICROPHONE BIAS



The overall gain from the microphone to V+ will vary with loop current due to the influence of the equalization amplifier on TXI. The signal at EQ is out of phase with that at TXI, therefore the signal at V+ decreases as loop current (and the EQ signal) increases. Variations are typically 2.0 to 5.0 dB and depend largely on the impedance characteristics of the microphone.

ALTERNATE MICROPHONE BIASING

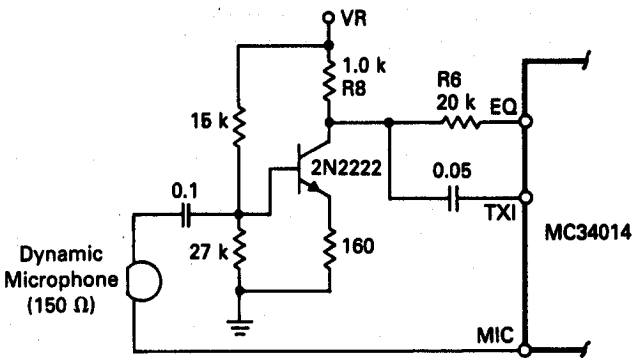
In the event that the microphone cannot be properly biased from the 1.2 volt VR supply, a higher voltage can be obtained by biasing from the V+ supply. The configuration shown in Figure 19, provides a higher voltage to the microphone, and also filters the speech signals at V+ from reaching it, preventing an oscillatory loop from forming. The maximum voltage limit of the microphone must be considered when biasing this way.

If a dynamic microphone is to be used in place of an electret unit, the circuit in Figure 20 will buffer its low impedance from the MC34014 circuit, maintaining the high impedance required at the junction of R_8 and R_6. The circuit shown provides a gain of ≈2.6 for the microphone signals, and can be adjusted by varying the 160 Ω resistor.

HANDSET/HANDS-FREE TELEPHONE

Figure 23 indicates a circuit using the MC34014 speech network, MC34018 speakerphone circuit, and the MC34017 tone ringer to provide a complete telephone/speakerphone. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, and placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the MC34014 to the pulse dialing mode to mute the handset microphone and receiver when using the speakerphone. To compensate for the different equalization response of the MC34014 when in the pulse dialing mode (Figures 9 and 11), the 47 Ω resistor normally found at Pin 13 of the MC34014 is instead divided into two resistors (33 Ω and 15 Ω). This arrangement provides similar equalization response in both the handset and in the speakerphone modes. Since the LC capacitor (Pin 12) is ineffective in the speakerphone mode, a capacitor is added at Pin 5 (CC) to provide compensation for the equalization loop when the speakerphone mode is in effect.

FIGURE 20 — INTERFACING A DYNAMIC MICROPHONE



SWITCHABLE TONE/PULSE TELEPHONE

Figure 21 indicates a switchable tone/pulse telephone circuit using the MC145412 tone/pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer is programmable, and can store up to 10 phone numbers. As can be seen, the interface to the MC34014 is straightforward.

PULSE ONLY TELEPHONE

Figure 22 indicates a pulse only telephone circuit using the MC145409 pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer has last number redial, and provides a pacifier tone to the receiver during dialing.

FIGURE 21 — COMPLETE TELEPHONE WITH PULSE/TONE DIALING

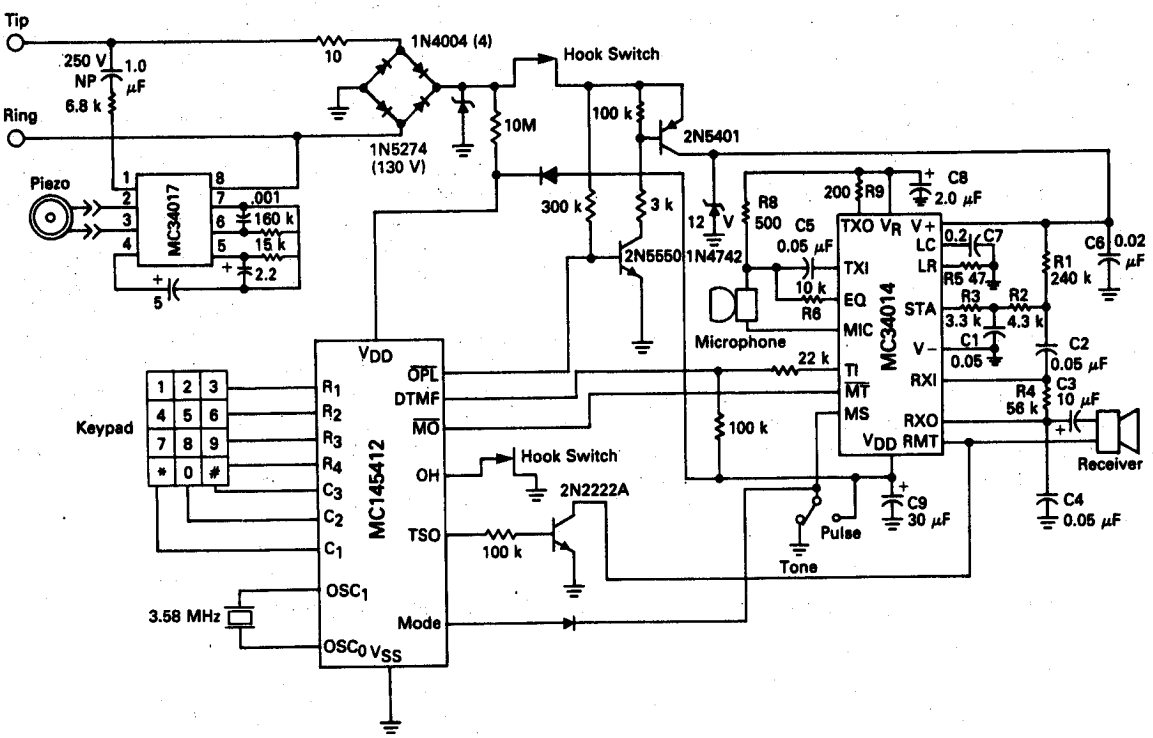
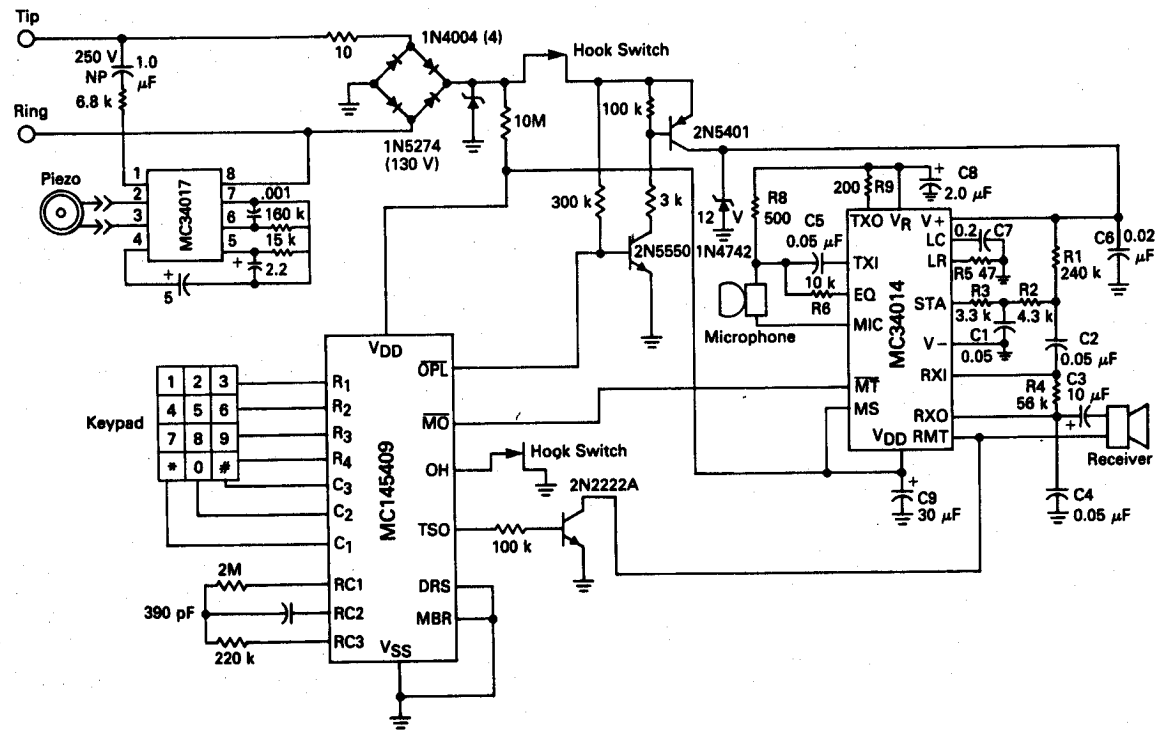


FIGURE 22 — COMPLETE TELEPHONE WITH PULSE DIALING



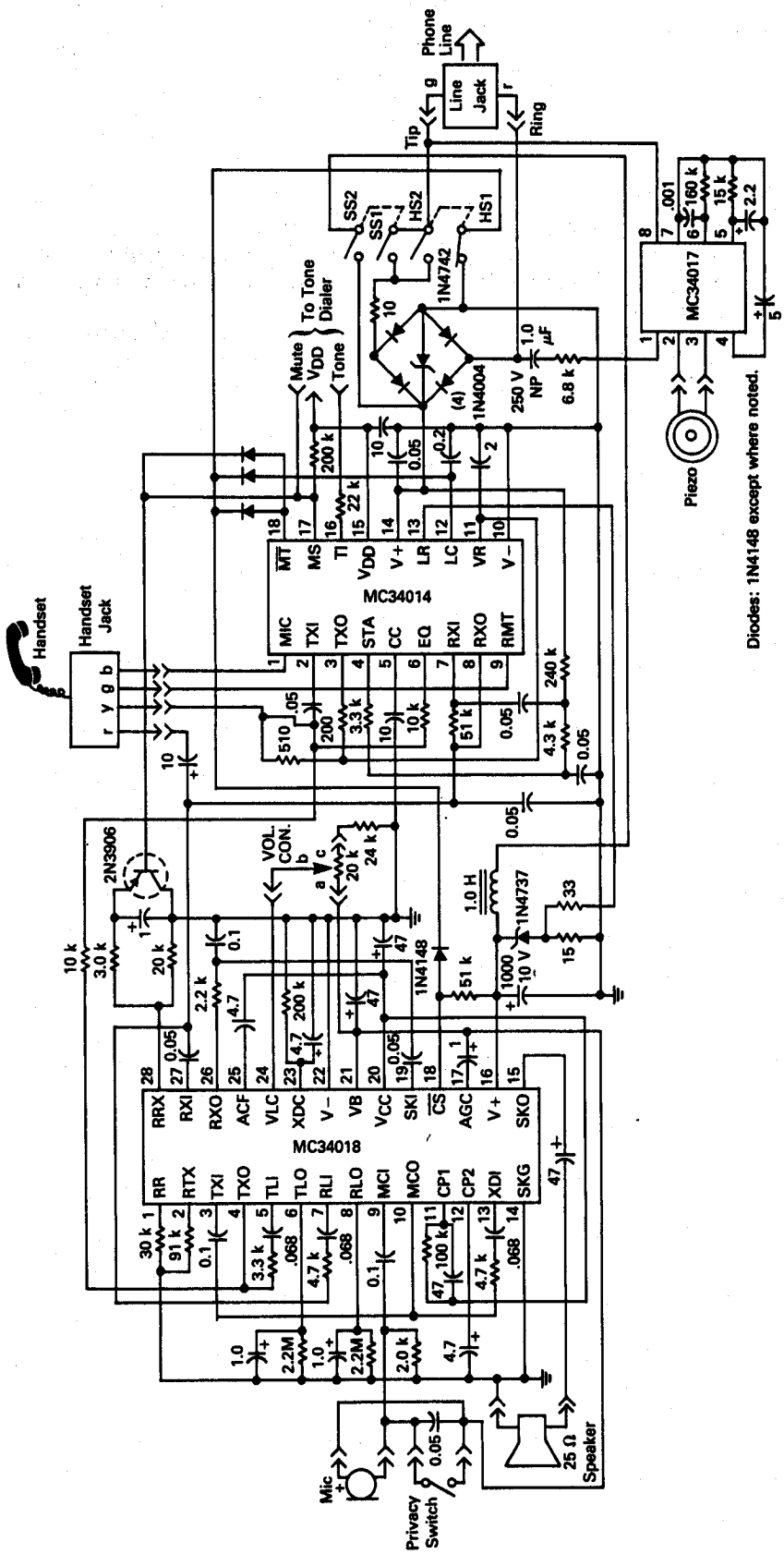


FIGURE 23 — SWITCHABLE HANDSET/HANDSFREE SYSTEM

Recommended External Components

Piezo Sounder
Models KSN 1113-1116
Motorola, Inc.
Albuquerque, N.M.
505-822-8801

Microphone/Receiver
Microphone model EM-95
Receiver model DH-34
Primo Microphone, Inc.
Elk Grove Village, Ill.
312-595-1022

Microphone Model KUC2123
Hosiden Electronics
Chicago, Ill.
312-956-7707

TRANSIENT PROTECTION & RFI SUPPRESSION

Protection from voltage transients is necessary in most telephone circuits, and may take the form of zener diodes, RC or LC filters, transient suppressors, or a combination of the above.

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the telephone. RFI may enter the circuitry through the Tip & Ring lines, through the microphone and/or receiver leads in the handset cord, or through any of the wiring or PC board traces. Ceramic decoupling capacitors, ferrite beads, and other RFI suppression techniques may be needed. Good PC board design techniques, such as the avoidance of loops, should be used. Long tracks on high impedance nodes should be avoided.