National Semiconductor

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LM1290
Autosync Horizontal Deflection Processor

General Description

The LM1290 is a high-performance, low-cost deflection solution for autosync monitors.

The LM1290 provides full autosync capability, DC controls and complete freedom from manufacturing trims. Its continuous capture range is from 22 kHz to 110 kHz (1:5). Mode change frequency ramping, for protection of the horizontal deflection output transistor, is programmable by using an external capacitor.

Together with the National Semiconductor LM1296 Raster Geometry Correction System for Multi-Frequency Displays, excellent performance is offered. The two-chip solution provides the advantage of good jitter performance, simplified board layout, and lower system cost.

The LM1290 is packaged in a 14-pin plastic DIP package.

Features

- Full autosync — 22 kHz to 110 kHz with no component switching or external adjustments
- No manufacturing trims needed — internal VCO capacitor trimmed on chip
- Sample-and-hold circuit for fast top-of-screen phase recovery, even when using composite sync
- DC-controlled H phase and duty cycle
- Resistor-programmable minimum VCO frequency
- Excellent jitter performance
- X-ray input disables H drive until V_{CC} powered down
- Low V_{CC} disables H drive (V_{CC} < 8.5V)
- H output transistor protected against accidental turn on during flyback
- Capacitor-programmable frequency ramping, df_{VCO}/dt, protects H output transistor during scanning mode changes

Connection Diagram

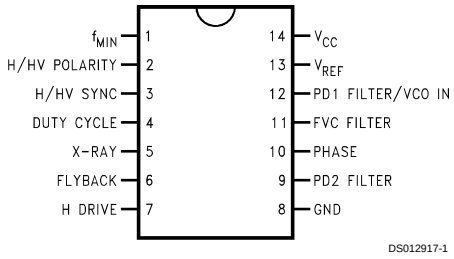

FIGURE 1.
Order Number LM1290N
See NS Package Number N14A

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Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	15V
Input Voltage (V_{DC})	
Pin 1	8V
Pins 3, 4, 5, 6	V_{CC}
Pin 10	$1.0V < V_{DC} < 7.5V$
Pin 12	10V
Output Sink Current, Pin 7	130 mA
Power Dissipation (P_D) (Above 25˚C, derate based on θ_{JA} and T_J)	1.65W
Thermal Resistance (θ_{JA})	75˚C/W
Junction Temperature (T_J)	150˚C
ESD Susceptibility (Note 5)	3.5 kV
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering 10 seconds)	265˚C

Operating Ratings (Note 2)

Operating Temperature Range	−20˚C to +80˚C
Supply Voltage	$10.8V \le V_{CC} \le 13.2V$

Electrical Characteristics

See Test Circuit (*Figure 2*) ; T_A = 25˚C; V_{CC} = 12V; V_5 = 0V unless otherwise stated.

Parameter	Condition	Typical (Note 6)	Limit (Note 7)	Units
Supply Current (Pin 14)	Pin 3 and Pin 7 Open Circuit, Pin 1 = −100 µA	30	40	mA (max)
Minimum Capture Frequency	H Sync Duty Cycle = 10%;	10	22	kHz (max)
Maximum Capture Frequency	Pin 1 (f_{MIN}) Open	115	110	kHz (min)
H/HV SYNC Input (Pin 3)	High Level		2.2	V (min)
Threshold Voltage	Low Level		0.8	V (max)
H/HV SYNC Input (Pin 3) Maximum Sync Tip Duty Cycle		26	24	%
H/HV SYNC Input (Pin 3) Minimum Sync Tip Duty Cycle	f_H = 22 kHz	5		%
H/HV POLARITY (Pin 2) Low Level Output Voltage, V_{OL}	C_{POL} = 0.1 µF; I_{OL} = +1 µA	0.05	0.4	V (max)
H/HV POLARITY (Pin 2) High Level Output Voltage, V_{OH}	C_{POL} = 0.1 µF; I_{OL} = −1 µA	4.5	4	V (min)
FVC Gain	22 kHz ≤ f_H ≤ 110 kHz	0.055		V/kHz
VCO Gain	22 kHz ≤ f_{VCO} ≤ 110 kHz	18.2		kHz/V
Phase Detector 1 Gain	H Sync Duty Cycle = 10%:			µA/radian
	f_H = 110 kHz	120		
	f_H = 60 kHz	80		
	f_H = 22 kHz	30		
Phase Detector 1 Output Impedance (Pin 12)		20		kΩ
Phase Detector 1 Leakage Current + VCO Bias Current (Pin 12)	H/HV SYNC Input Grounded	0.3	2	µA
Jitter	f_H = 110 kHz (Note 8)	0.9		ns p-p
	f_H = 90 kHz	1.1		
	f_H = 60 kHz	1.6		
	f_H = 31 kHz	3.6		
	f_H = 22 kHz	5.8		
Free Run Frequency Variation	I_1 = −225 µA	32	34	kHz (max)
		26	25	kHz (min)
H Drive Phase Control Gain	V_{10} = 2V to 6V (Note 11)	8.89 (32)		% T_H/V (˚/V)

Electrical Characteristics (Continued)

See Test Circuit (*Figure 2*) ; T_A = 25˚C; V_{CC} = 12V; V_5 = 0V unless otherwise stated.

Parameter	Condition	Typical (Note 6)	Limit (Note 7)	Units
H Drive Phase Control Range	V_{10} = 3.6V to 7V (Notes 9, 11) (See Application Hint #3)	±14		$\%T_H$
H Drive Duty Cycle Control Gain	V_4 = 0V to 4V (Note 10)	10.8		%/V
H Drive Duty Cycle Maximum (Pin 7)	V_4 = 0V (Note 10)	68	63	% (min)
H Drive Duty Cycle Minimum (Pin 7)	V_4 = 4V (Note 10)	25	35	% (max)
H Drive Low Level Output Voltage (Pin 7)	I_{OL} = 100 mA	0.7		V
Flyback Input Threshold Voltage (Pin 6)	Positive-Going Flyback Pulse	2.2		V
Maximum Allowable Storage Delay of Horizontal Deflection Output Transistor Plus Half of Flyback Pulse Width	From H Drive Rising Edge to Center of Flyback Pulse	30		$\%T_H$
V_{CC} Lockout Threshold Voltage (Pin 14)	V_{CC} Below Threshold: H Drive Output Disabled		8.5	V (max)
	V_{CC} Above Threshold: H Drive Output Enabled		10.5	V (min)
X-Ray Shutdown Threshold Voltage (Pin 5)	Above Threshold: H Drive Output Disabled	1.85	2	V (min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any elevated temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 150˚C. The typical thermal resistance (θ_{JA}) of the LM1290N is 75˚C/W.

Note 5: Human Body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 6: Typical specifications are at T_A = 25˚C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The standard deviation, σ, of the flyback pulse period is measured with a HP 53310A Modulation Domain Analyzer. Peak-to-peak jitter of the flyback pulse is defined by 6σ.

Note 9: A positive phase value represents a phase lead of the flyback pulse peak with reference to the center of H sync.

Note 10: The duty cycle is measured under the conditions of free run with I_1 = −100 µA, T_{FBP} = 3 µs and T_d = 3.5 µs where T_{FBP} and T_d are the flyback pulse width and the turn off delay of the H deflection output transistor respectively.

Note 11: T_H is defined as the total time of one horizontal line.

Test Circuit

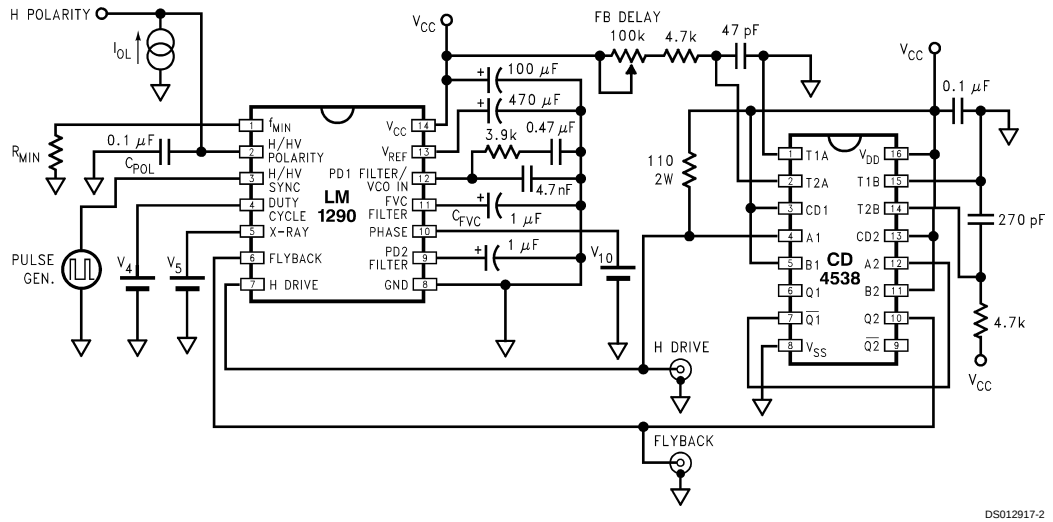

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FIGURE 2.

System Block Diagram

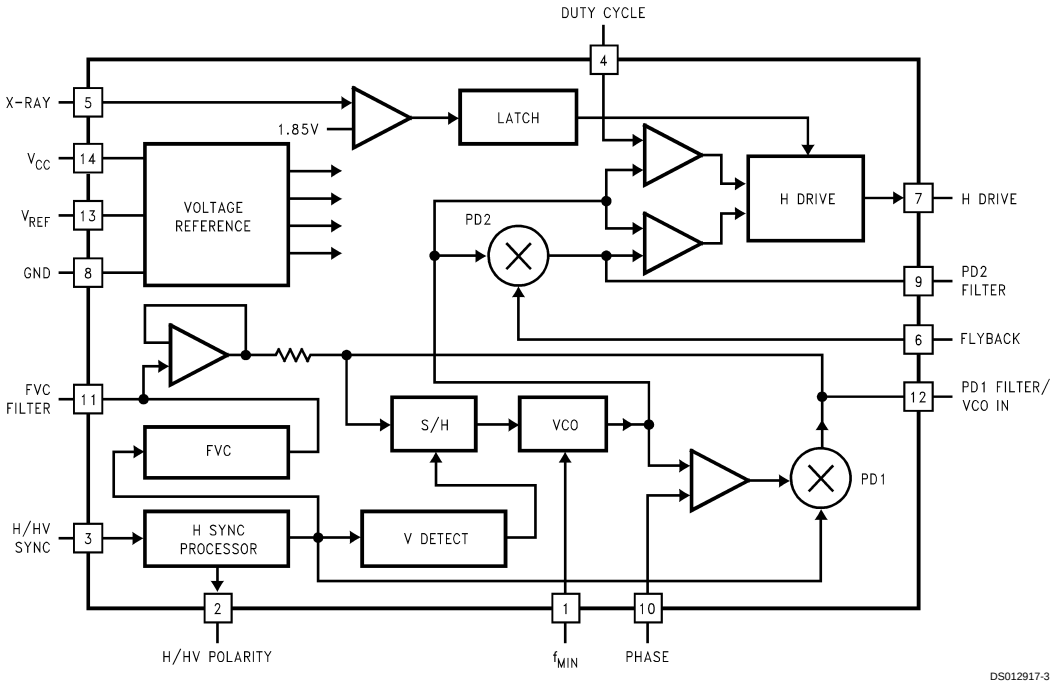

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FIGURE 3.

Pin Descriptions

See *Figure 4* through *Figure 10* for input and output schematics.

Pin 1 — f_{MIN}: A resistor from this pin to ground sets the free run frequency of the LM1290. The free run frequency should be set typically as:

$$f_{MIN} = 0.85(f_{MINLOCK}) - 2\ kHz$$

where $f_{MINLOCK}$ is the minimum lock frequency required for the application. The resistance required to set this frequency is approximately:

$$R_{MIN} \approx \frac{5.475 \times 10^8}{f_{MIN}} - 500\Omega$$

For example, to find R_{MIN} for VGA which has $f_{MINLOCK}$ = 31.469 kHz,

$$f_{MIN} = 0.85(31.469\ kHz) - 2\ kHz = 24749$$

$$R_{MIN} \approx \frac{5.475 \times 10^8}{24749} - 500 = 21622\Omega$$

Rounding to the closest standard 1% resistor gives R_{MIN} = 21.5 kΩ.

Pin 2 — H/HV POLARITY: A 0.1 µF capacitor is connected from this pin to ground for detecting the polarity of H/HV sync at pin 3. A low logic level at pin 2 indicates active-high H/HV sync to pin 3, a high level indicates active-low. See *Figure 4* for the output schematic.

Pin 3 — H/HV SYNC: This input pin accepts DC-coupled H or composite sync of either polarity. For best noise immunity, a resistor of 2 kΩ or less should be connected from this pin to pin 8 (GND) via a short path. See *Figure 5* for the input schematic.

Pin 4 — DUTY CYCLE: A DC voltage applied to this pin sets the duty cycle of the H DRIVE output (pin 7), with a range of approximately 30% to 70%. 2V sets the duty cycle to approximately 50%. See *Figure 6* for the input schematic.

Pin 5 — X-RAY: This pin is for monitoring CRT anode voltage. If the input voltage exceeds an internal threshold, H DRIVE output (pin 7) is latched high. V_{CC} has to be reduced to below approximately 2V to clear the latched condition, i.e., power must be turned off. See *Figure 7* for the input schematic.

Pin 6 — FLYBACK: Input pin for phase detector 2. For best operation, the flyback peak should be at least 5V but not greater than V_{CC}. Any pulse width greater than 1.5 µs is acceptable. See *Figure 8* for the input schematic.

Pin 7 — H DRIVE: This is an open-collector output which provides the drive pulse for the high power deflection circuit. The pulse duty cycle is controlled by pin 4. Polarity convention: Horizontal deflection output transistor is on when H DRIVE OUT is low. See *Figure 9* for the output schematic.

Pin 8 — GND: System ground. For best jitter performance, all bypass capacitors should be connected to this pin via short paths.

Pin 9 — PD2 FILTER: The low-pass filter cap of between 0.01 µF to 1 µF for the output of phase detector 2 is connected from this pin to pin 8 (GND) via a short path. A smaller value increases the response.

Pin 10 — PHASE: A DC control voltage applied to this pin sets the phase of the flyback pulse with respect to the center of H sync. See *Figure 10* for the input schematic.

Pin 11 — FVC FILTER: A 1 µF capacitor is connected from this pin to pin 8 (GND) via a short path.

Pin 12 — PD1 OUT/VCO IN: Phase detector 1 has a gated charge pump output which requires an external low-pass filter. For best jitter performance, the filter should be grounded to pin 8 (GND) via a short path. If a voltage source is applied to this pin, the phase detector is disabled and the VCO can be controlled directly.

Pin 13 — V_{REF}: This is the decoupling pin for the internal 8.2V reference. It should be decoupled to pin 8 (GND) via a short path with a cap of at least 470 µF. Do not load this pin.

Pin 14 — V_{CC}: 12V nominal power supply pin. This pin should be decoupled to pin 8 (GND) via a short path with a cap of at least 47 µF.

Input/Output Schematics

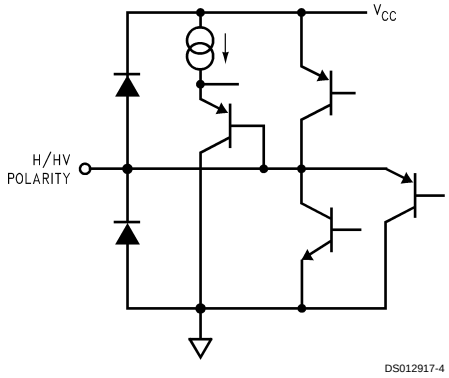


FIGURE 4.

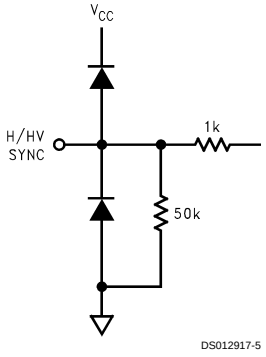


FIGURE 5.

Input/Output Schematics (Continued)

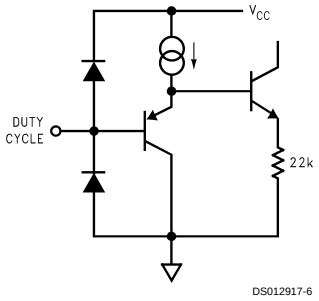


FIGURE 6.

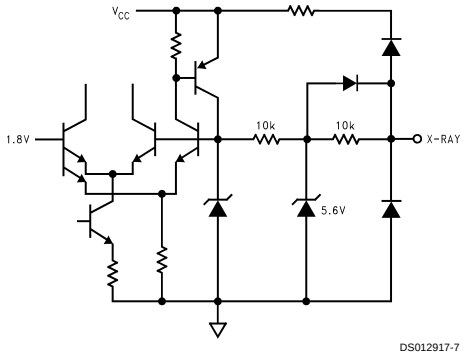


FIGURE 7.

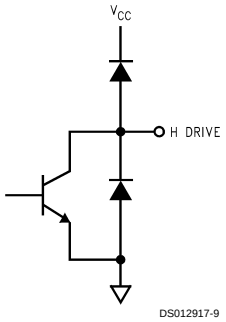


FIGURE 9.

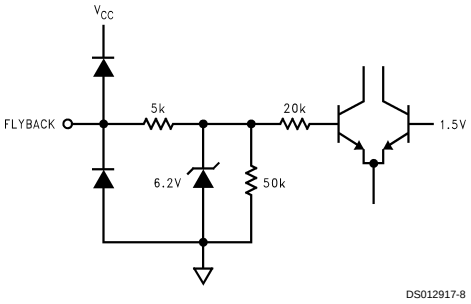


FIGURE 8.

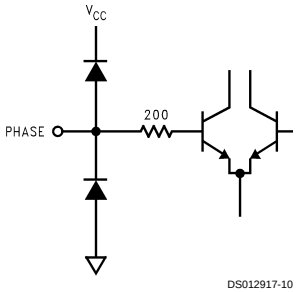


FIGURE 10.

Application Hints

1. **Phase Control for Geometry Correction:** Pin 10 (PHASE) is designed to control static phase (picture horizontal position) as well as dynamic phase for geometry correction. Complete control of static and dynamic phase can be achieved by superposing a correction waveform (Sawtooth and/or parabola) on the DC control voltage at pin 10 (see *Figure 12*).
2. **Programmable Frequency Ramping:** H frequency transitions from high to low present a special problem for deflection output stages without current limiting. If, during such a transition, the output transistor on-time increases excessively before the B+ voltage has decreased to its final level, then the deflection inductor current ramps too high and the induced flyback pulse can exceed the breakdown voltage, BV_{CEX}, of the output transistor. To prevent this, the rate of change of the VCO frequency must be limited.

   Consider a scanning mode transition at t = 0 from f_1 to f_2. The VCO frequency as a function of time, $f_{VCO}(t)$, is described by the equation,

   $f_{VCO}(t) \cong f_1 + (f_2 - f_1)\,(1 - \exp(-t/\tau))$,

   where $\tau = 40 \times 10^3 \times C_{FVC}$.

   The above equation can be used to predict VCO behavior during frequency transitions, but in practice the value of C_{FVC} is most easily determined empirically. In general, large values minimize the chance of exceeding BV_{CEX}, but generate long PLL capture times.
3. **Phase Voltage Range vs Delay Time:** The recommended phase voltage range to use on pin 10 (PHASE) depends on the delay time of the deflection output stage. Delay time is defined as the time from the rising edge of H Drive to the center of flyback. For best performance the phase voltage range should be in the unshaded area of *Figure 11*.

Recommended Phase Voltage for 640 x 480 @ 60 Hz

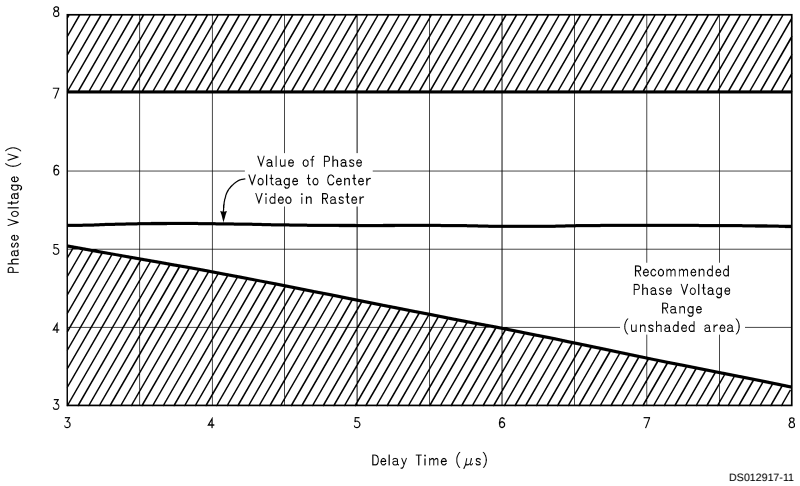
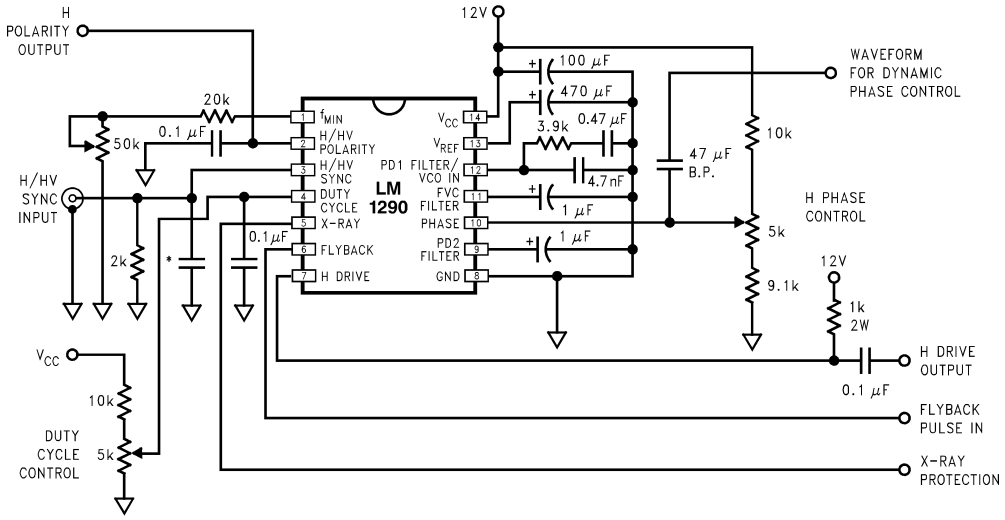


FIGURE 11.

Typical Application



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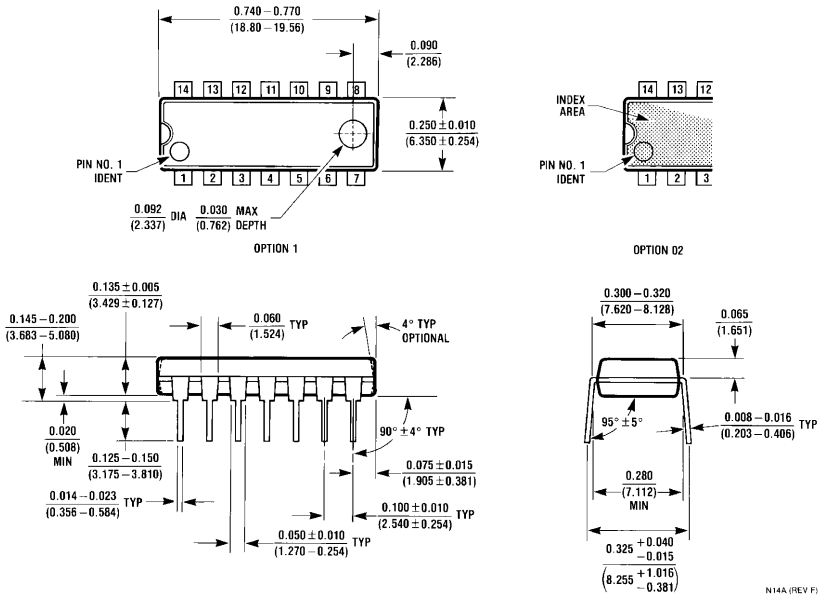
*Actual value depends on the application and the ambient noise level inside the monitor.

FIGURE 12.

Physical Dimensions inches (millimeters) unless otherwise noted



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NS Package Number N14A

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