Ordering number: EN1616H

CMOS LSI

SANYO No.1616H

LC7565, 7565A, 7565B

FLT Driver for Display of Graphic Equalizer

Use

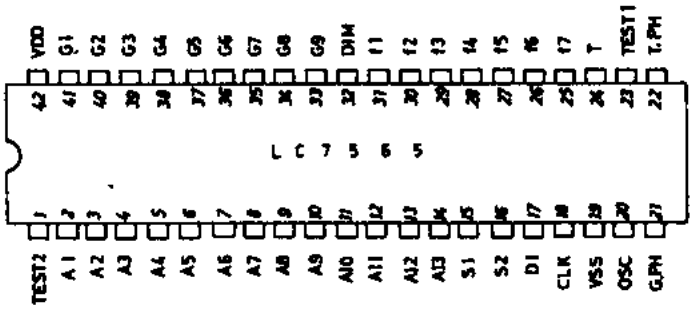
FLT driver for spectrum analyzer display and driver for setting point of graphic equalizers LC7520, LC7522.

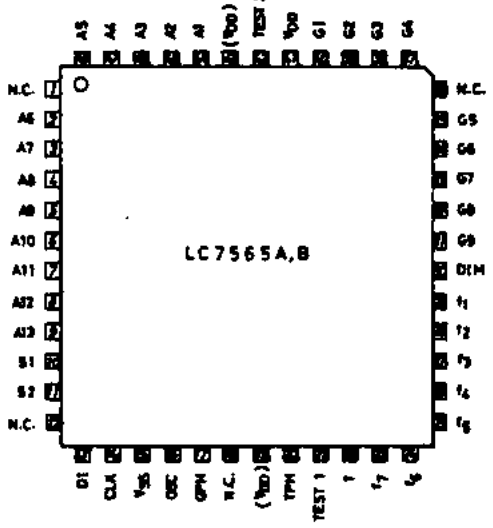
Features

(1) Single 5V supply (FLT driver section : 40V breakdown voltage)
(2) 7-band display + accessory display + total display : 13 segments × 9 grids
- Display of band-pass signal strength → Spectrum analyzing display : 7 bands 2dB/step, 13-dot display + total display
- Display of setting state in each band → Dot display : Flashable at the setting mode, R/L selectable.
- Accessory display : 13 kinds of L, R, and Mn of memory.

(3) In 1-chip applications, the signal strength display input is the L/R mixing input. (The mixing circuit is connected externally.)
(4) Display unit : Dynamic drive of FLT. Duty cycle 1/11.4 (Total display 2/11.4)
(5) Band-pass filter for display : External equivalent filter
(6) System control : External microcomputer-controlled. Only 2 control buses
(7) Spectrum analyzing display with peak hold function.
(8) Dimmer function
(9) LED display available with external transistor driver.
(10) Flashing of a setting point in each band for graphic equalizer display is possible using setting point flash data.

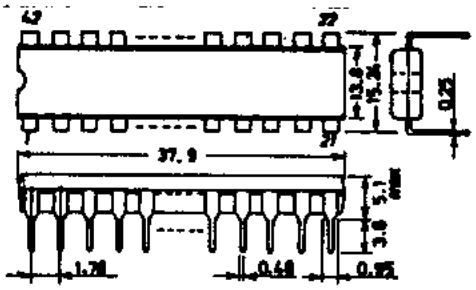
Pin Assignment





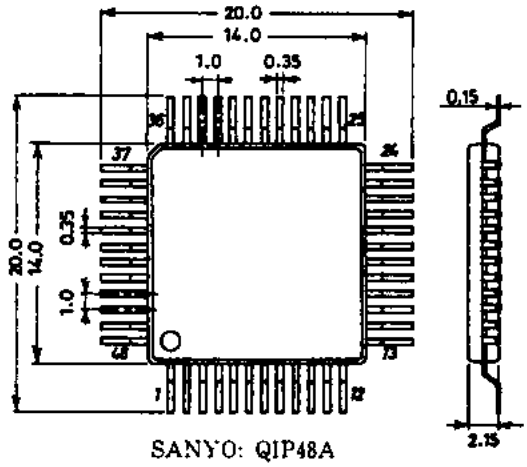
SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10,1 Ueno, Taito-ku, TOKYO, 110 JAPAN

Package Dimensions 3025B
(unit : mm) [LC7565]



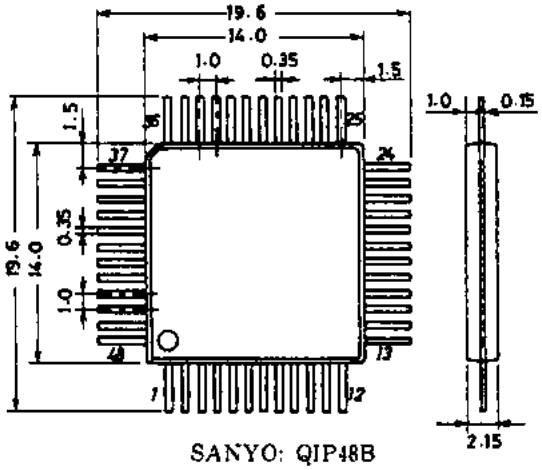
SANYO: DIP42S

Package Dimensions 3052A
(unit : mm) [LC7565A]



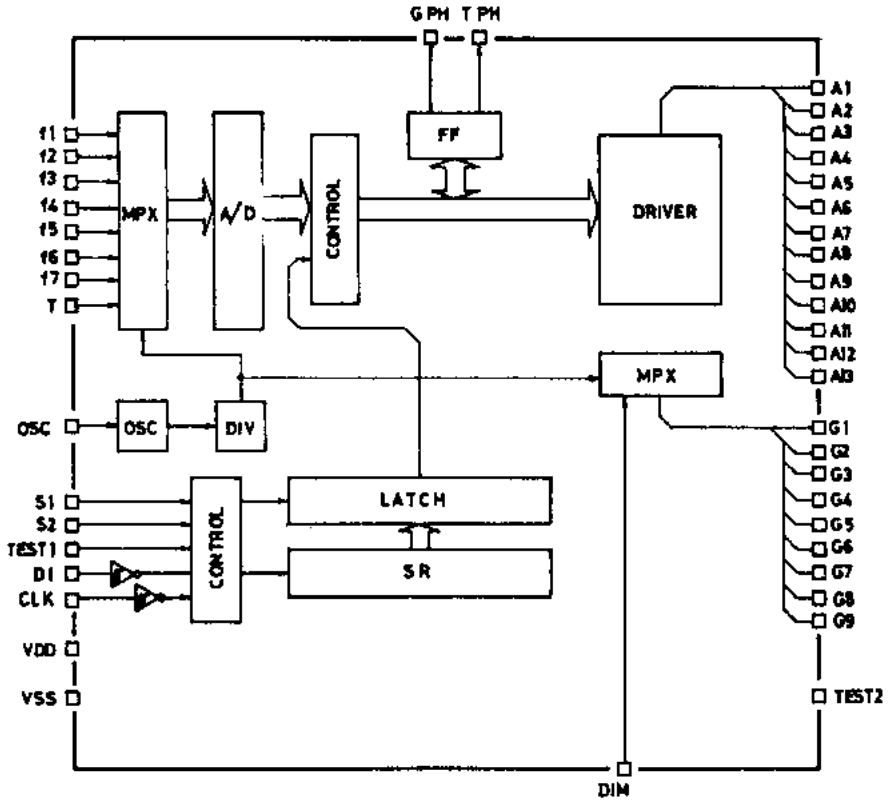
SANYO: QIP48A

Package Dimensions 3118
(unit : mm) [LC7565B]



SANYO: QIP48B

Equivalent Circuit Block Diagram



Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

				unit
Maximum Supply Voltage	V_{DD} max		V_{SS} to V_{SS} + 7.0	V
Maximum Input Voltage	V_I max	CLK,DI,f1 to f7,T,TEST1, S1,S2,T-PH,G-PH,DIM	V_{SS} − 0.3 to V_{DD} + 0.3	V
Maximum Output Voltage	V_O max	A1 to A13,G1 to G9	V_{DD} − 40 to V_{DD} + 0.3	V
Output Current	I_{O1}	A1 to A13	down to −5.0	mA
	I_{O2}	G1 to G9	down to −15.0	mA
Allowable Power Dissipation	Pd max		300	mW
Operating Temperature	Topg		−40 to +85	°C
Storage Temperature	Tstg		−40 to +125	°C

Allowable Operating Conditions at Ta = 25°C, V_{SS} = 0V

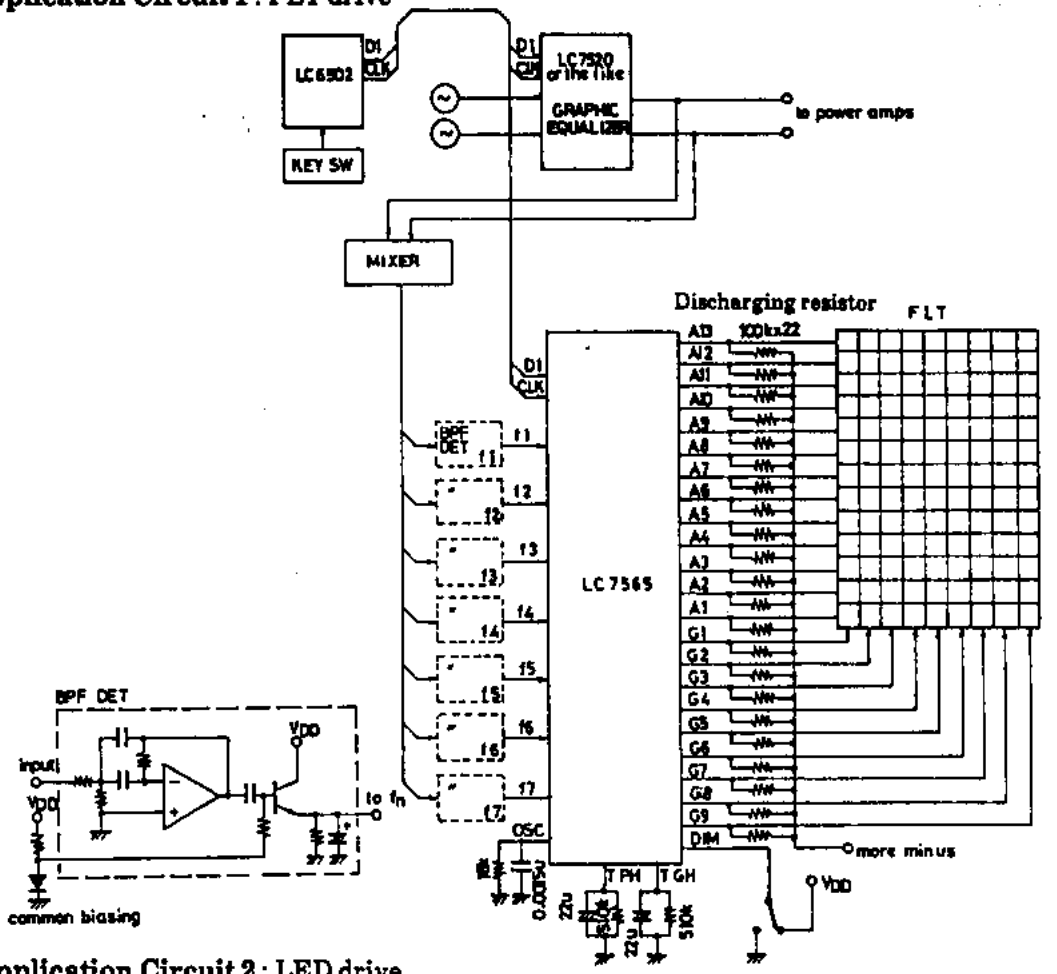
			min	typ	max	unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Input "H"-Level Voltage	$V_{IH}1$	CLK,DI,S1,S2,DIM	0.8V_{DD}		V_{DD}	V
	$V_{IH}2$	T-PH,G-PH	0.9V_{DD}		V_{DD}	V
Input "L"-Level Voltage	$V_{IL}1$	CLK,DI,S1,S2,DIM	V_{SS}		0.2V_{DD}	V
	$V_{IL}2$	T-PH,G-PH	V_{SS}		0.1V_{DD}	V
Input Pulse Width	$t_{\phi w}$	CLK	1			μs
Setup Time	t_{stup}	CLK,DI	1			μs
Hold Time	t_{hold}	DI	1			μs
Operating Frequency	f_{opg}	CLK			330	kHz
Output Voltage (Open drain)	v_o	A1 to A13, G1 to G9	V_{DD} − 38		V_{DD}	V

Electrical Characteristics at Ta = 25°C, V_{DD} = 5V

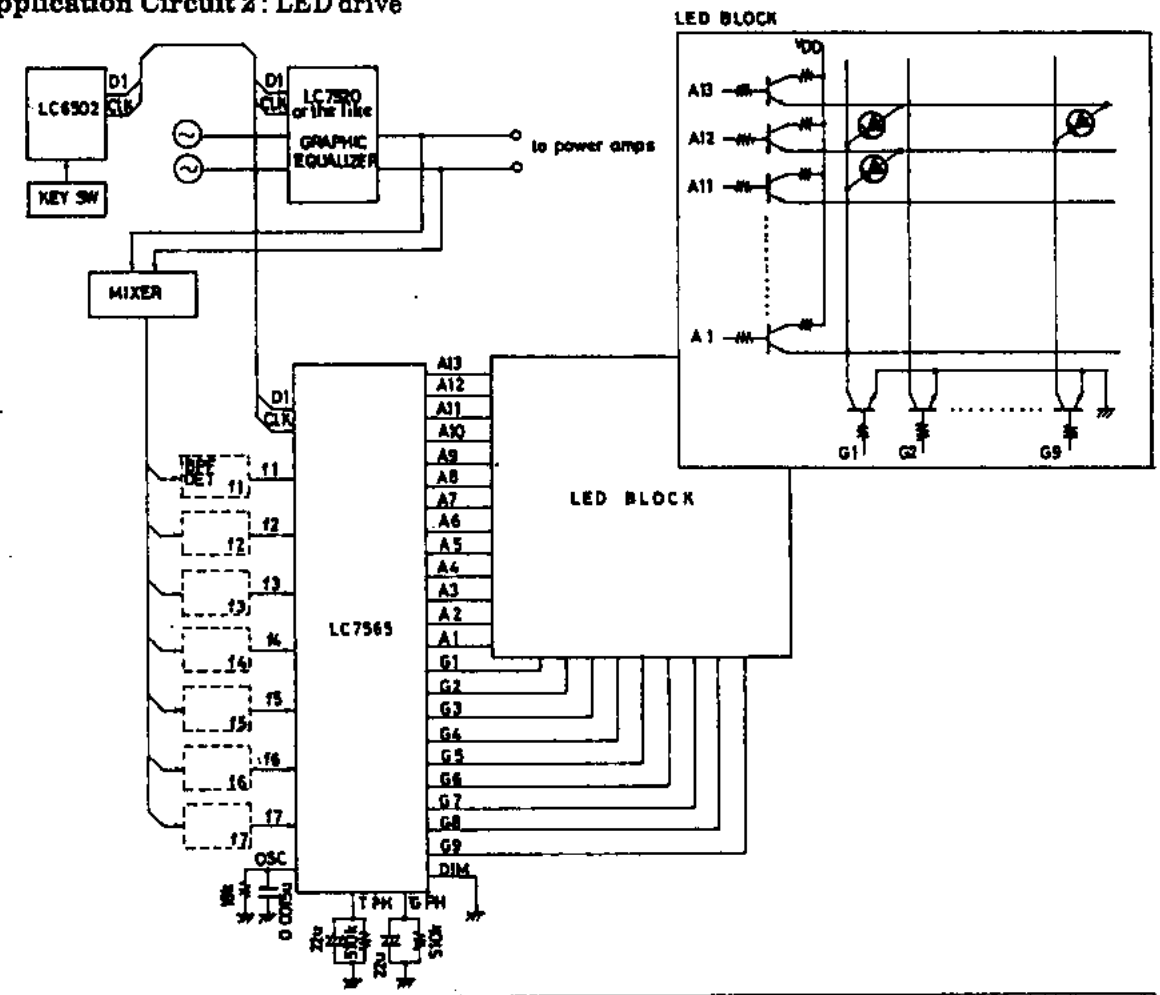
				min	typ	max	unit
Input "H"-Level Current	I_{IH}	CLK,DI,S1,S2,TEST1,V_I = 5V		0		10	μA
Input "L"-Level Current	I_{IL}	CLK,DI,S1,S2,TEST1,V_I = 0V		−10		0	μA
Output "H"-Level Voltage	$V_{OH}1$	A1 to A13,I_O = −2.5mA		V_{DD} − 2.5			V
	$V_{OH}2$	G1 to G9,I_O = −14mA		V_{DD} − 6.0			V
Output Leakage Current	I_{off}	G1 to G9,A1 to A13, V_O = V_{DD} − 38				10	μA
Input Sensitivity	v_i	f1 to f7,V_{DD} = 5V, 0dB = 267mV	+12 lighted	23	24	25	dB
			+10 lighted	21	22	23	dB
			+8 lighted	19	20	21	dB
			+6 lighted	17	18	19	dB
			+4 lighted	15	16	17	dB
			+2 lighted	13	14	15	dB
			0 lighted	11	12	13	dB
			−2 lighted	9	10	11	dB
			−4 lighted	7	8	9	dB
			−6 lighted	5	6	7	dB
			−8 lighted	3	4	5	dB
			−10 lihgted	1	2	3	dB
			−12 lighted	−1	0	1	dB
Current Dissipation	I_{DD}	Output open				2	mA
Duty Cycle	D.S	G1 to G7,G9			1/11.4		
		G8			2/11.4		

Note 1 : When mounting the QIP package on the board, do not dip the entire package in solder.

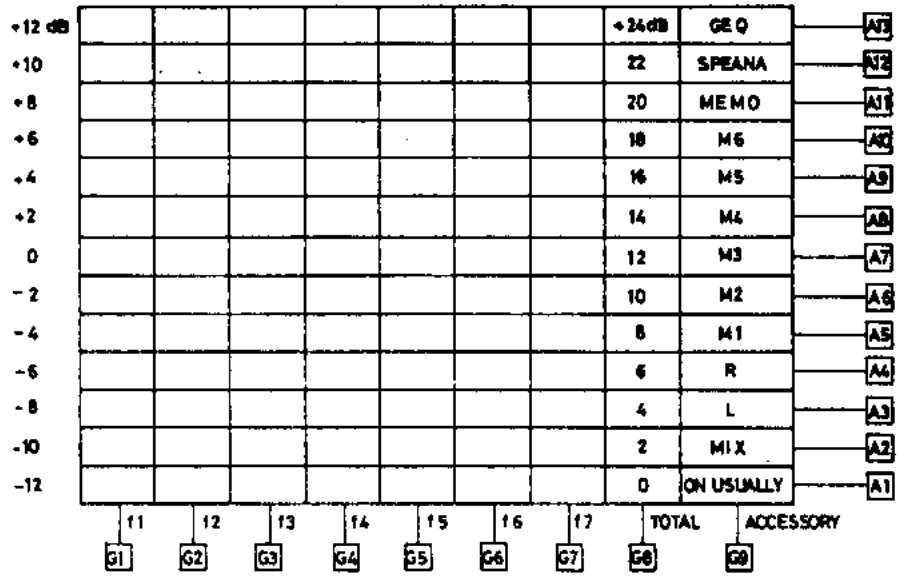
Sample Application Circuit 1 : FLT drive



Sample Application Circuit 2 : LED drive



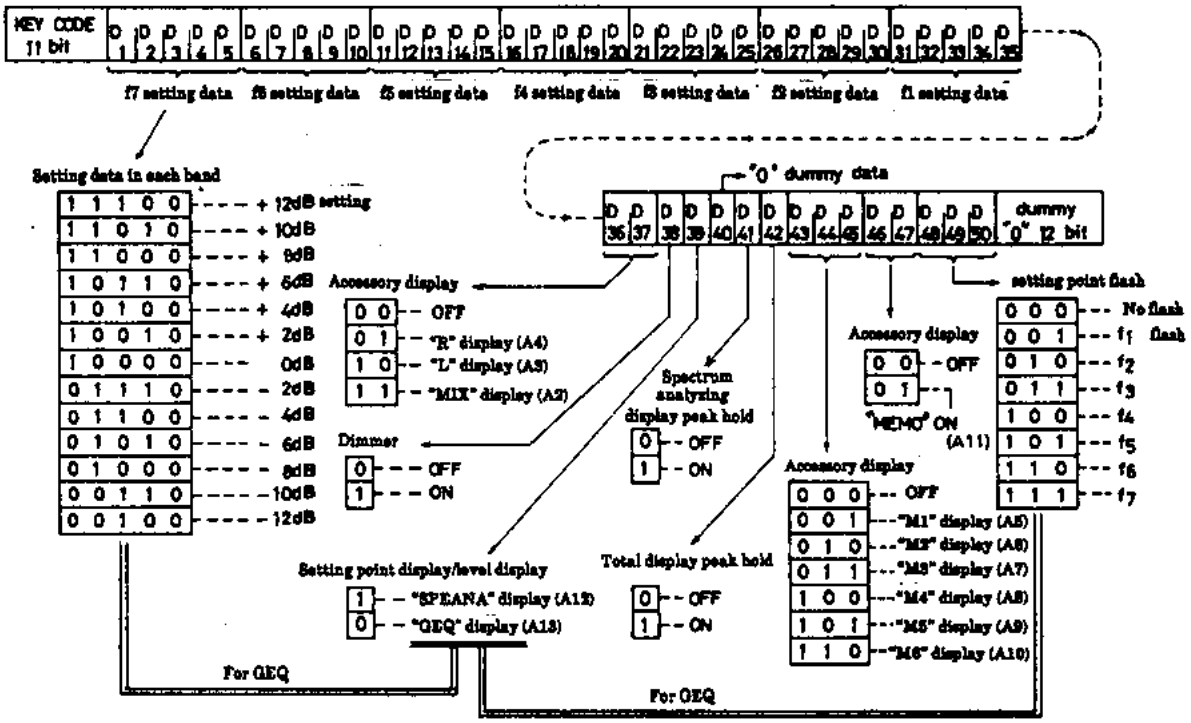
Segment Assignment



The following restrictions are imposed on accessory display.

(1) Either GEQ (A13) or SPEANA (A12) is lighted. Lighting of GEQ/SPEANA is synchronized with the setting dot mode/spectrum analyzing mode respectively.
(2) MEMO (A11) can be turned ON/OFF independently.
(3) All of M1 (A5) to M6 (A10) are unlighted or one of them is lighted.
(4) All of R (A4), L (A3), MIX (A2) are unlighted or one of them is lighted.
(5) (A1) remains turned ON.

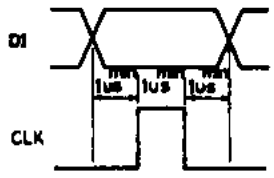
Data Code



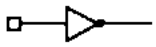
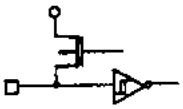
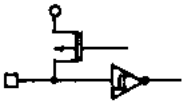
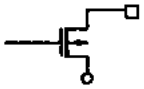
Note 1 When power is applied, data "0" must be first transferred for 61 clocks (initial clock) or more. If data transfer is stopped halfway, the transfer of the remaining data must be completed or data transfer must be started after the initial clocks have been transferred.

Note 2 When the DI, CLK pins are shared with the LC7520, etc., the maximum initial clocks for such device must be transferred.

Data Timing



Pin Description ( ) : LC7565A, 7565B

Pin Name	Pin No.	Pin Configuration	Function
V_{DD}	42 (41)		· Power supply pin. +5V typ.
V_{SS}	19 (15)		· Power supply pin. Gnd.
DI	17 (13)		· Pin for inputting data from CPU · Schmitt inverter type
CLK	18 (14)		· Pin for inputting CLK from CPU · Schmitt inverter type
S1	15 (10)		· Select pin when a plurality of chips (max. 3 pcs.) are used. · S2 S1 Key code Last bit 1 0 1 1 1 1 1 0 0 1 0 1 0 0 1 1 1 1 1 1 0 0 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0
S2	16 (11)		
G.PH	21 (17)		· Pin for connecting C, R which determine the peak hold reset time of spectrum analyzing display of graphic equalizer. When no peak hold is used, pull down with a resistor of several kΩ.
T.PH	22 (20)		· Pin for connecting C, R which determine the peak hold reset time of total display. When no peak hold is used, pull down with a resistor of several kΩ.
DIM	32 (30)		· Pin used to direct drive the IC (when not CPU-controlled) and to control the dimmer. · "1" : Dimmer ON, "0" : Dimmer OFF
f1 to f7, T	31 to 25 (23 to 29) 24 (22)		· Pin for inputting the rectified voltage of audio signal.
OSC	20 (16)		· Output buffer of open drain type · Pin for connecting C, R for OSC
A1 to A13	2 to 14 (44 to 48) (2 to 9)		· Open drain driver · Anode drive
G1 to G9	41 to 33 (31 to 35) (37 to 40)		· Open drain drive Grid drive
TEST 1	23 (21)		· IC test pin (input) Normally connected to V_{SS}
TEST 2	1 (42)		· IC test pin (output) Normally open
NC	(1, 12) (18, 36)	QIP-48 only	· No connection pin. Nothing must be connected to this pin.
(V_{DD})	(43, 19)	QIP-48 only	· V_{DD} sub-pin. Open or connected to V_{DD}.