Ordering number : EN4677

CMOS LSI

LC66354B, 66356B, 66358B

Four-bit Single-Chip Microcontrollers On-Chip 4 K/6 K/8 K-byte ROM

Overview

The LC66354B, LC66356B and LC66358B are 42-pin package four-bit CMOS microcontrollers that integrate on a single chip all functions required in a control microcontroller, including ROM, RAM, I/O ports, serial interfaces, comparator inputs, three-value inputs, timers and an interrupt system. These products differ from the earlier LC66358A series in their power supply voltage range and operating speed specifications.

Features and Functions

- ROM (with 4 K-, 6 K- and 8 K-byte capacities) and RAM (512 4-bit digits) on chip
- LC66000 series compatible instruction set (128 instructions)
- A total of 36 I/O port pins
- Two eight-bit serial interfaces that can be connected in cascade to form a 16-bit interface
- Instruction cycle time: 0.92 to 10 µs (3 to 5.5 V)
  The earlier LC66358A series had instruction cycle times of from 1.96 to 10 µs (at 3 to 5.5 V) and from 3.92 to 10 µs (at 2.2 to 5.5 V).
- Powerful timer and prescaler functions
  Time limit timer, event counter, pulse width measurement and square wave output using a 12-bit timer.
  Time limit timer, event counter, PWM output and square wave output using an 8-bit timer.
  Time base function using a 12-bit prescaler.
- Powerful interrupt system with eight interrupts and eight vector locations
  External interrupts: three interrupts and three vector locations
  Internal interrupts: five interrupts and five vector locations
- Flexible I/O functions
  Comparator inputs, three-value inputs, 20 mA drive outputs, 15 V withstand voltage, pull-up or open-drain option switching
- Runaway detection function (watchdog timer) option
- Eight-bit I/O function
- Power reduction functions using halt and hold modes
- Packages: DIP42S, QIP48E (QFP48E)
- Evaluation LSI: used together
  — LC66599 (evaluation chip) + EVA850/800-TB6630X
  — LC66E308 (on-chip EPROM microcontroller)

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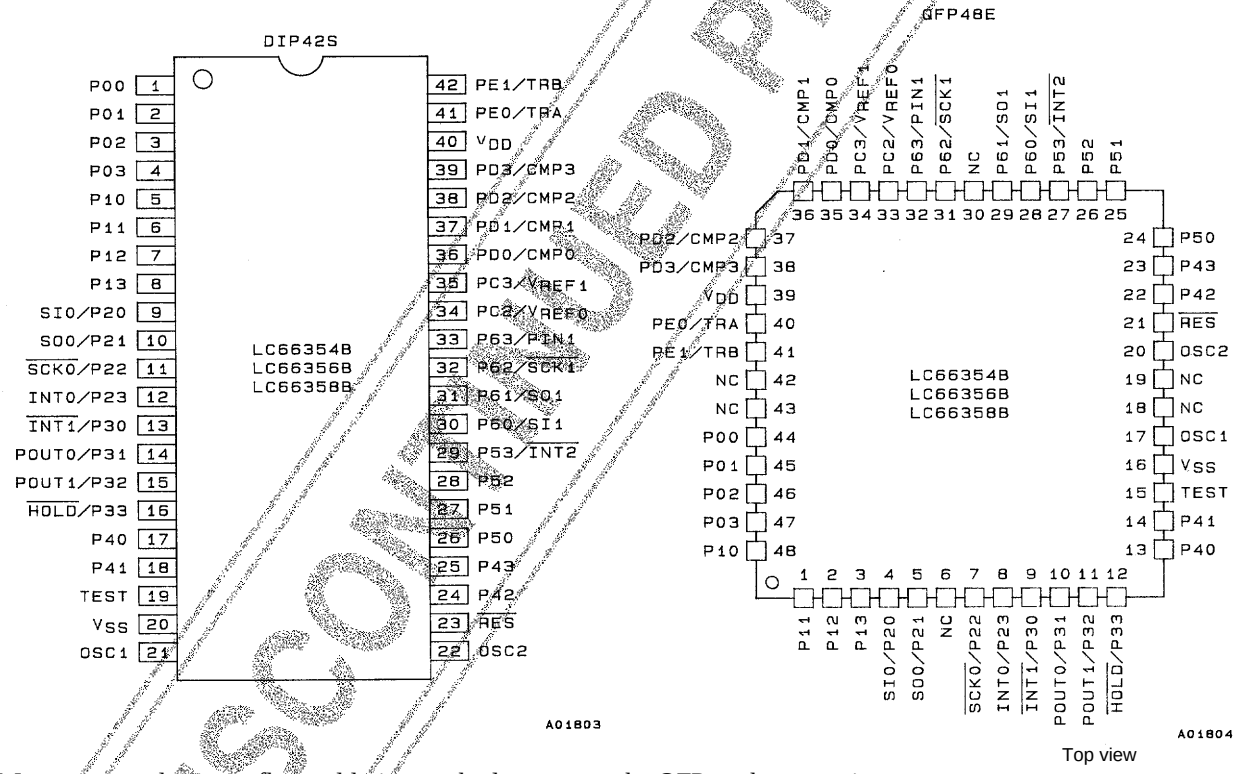
93098HA (OT) / 83194TH (OT) B8-0696 No. 4677-1/23

Series Structure

Product name	Pins	ROM capacity	RAM capacity	Package		Features
LC66304A/306A/308A	42, 48	4 K/6 K/8 K bytes	512 W	DIP42S	QFP48E	Normal version 4.0 to 6.0 V/0.92 µs
LC66404A/406A/408A	42, 48	4 K/6 K/8 K bytes	512 W	DIP42S	QFP48E	
LC66506B/508B/512B/516B	64	6 K/8 K/12 K/16 K bytes	512 W	DIP64S	QFP64A	
LC66354A/356A/358A	42, 48	4 K/6 K/8 K bytes	512 W	DIP42S	QFP48E	Low-voltage version 2.2 to 5.5 V/3.92 µs
LC66354S/356S/358S*	44	4 K/6 K/8 K bytes	512 W		QFP44M	
LC66556A/558A/562A/566A	64	6 K/8 K/12 K/16 K bytes	512 W	DIP64S	QFP64E	
LC66354B/356B/358B	42, 48	4 K/6 K/8 K bytes	512 W	DIP42S	QFP48E	Low-voltage, high-speed version 3.0 to 5.5 V/0.92 µs
LC66556B/558B*	64	6 K/8 K bytes	512 W	DIP64S	QFP64E	
LC66562B/566B	64	12 K/16 K bytes	512 W	DIP64S	QFP64E	
LC66E308	42, 48	EPROM, 8 K bytes	512 W	DIC42S (window)	QFC48 (window)	Evaluation window and OTP versions 4.5 to 5.5 V/0.92 µs
LC66P308	42, 48	OTPROM, 8 K bytes	512 W	DIP42S	QFP48E	
LC66E408	42, 48	EPROM, 8 K bytes	512 W	DIC42S (window)	QFC48 (window)	
LC66P408	42, 48	OTPROM, 8 K bytes	512 W	DIP42S	QFP48E	
LC66E516	64	EPROM 16 K bytes	512 W	DIC64S (window)	QFC64 (window)	
LC66P516	64	OTPROM 16 K bytes	512 W	DIP64S	QFP64E	

Note: * Under development

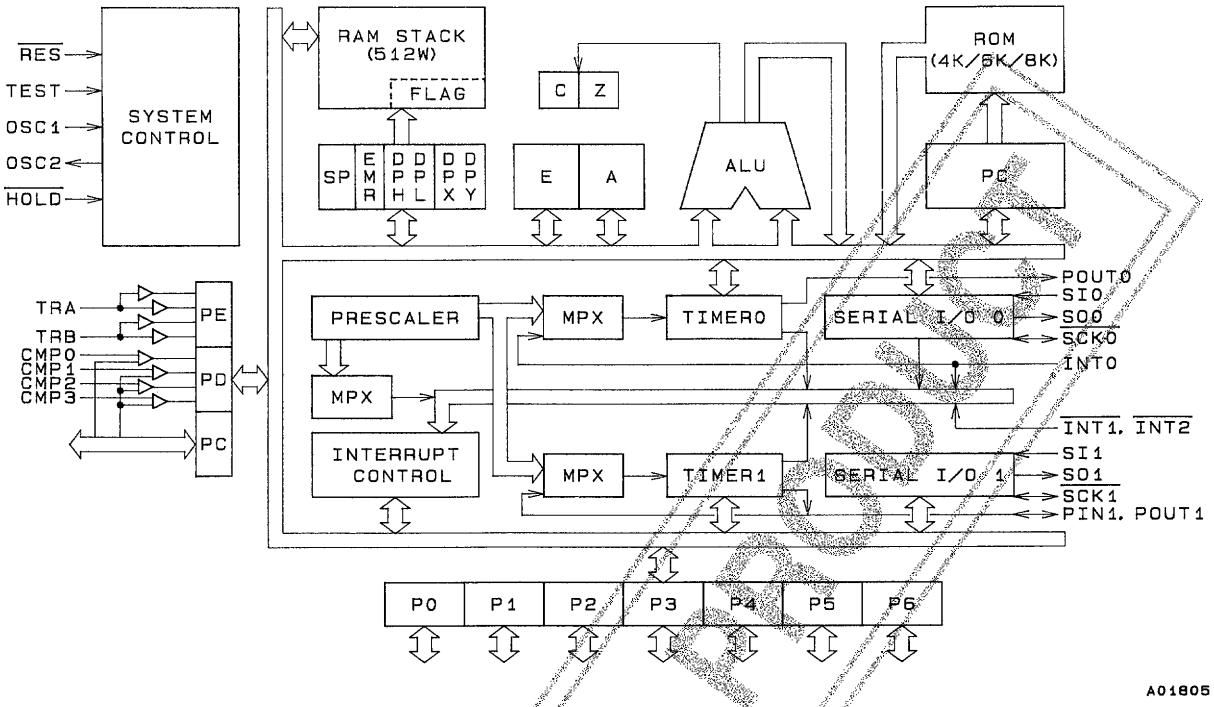
Pin Assignments



Top view

We recommend using reflow soldering methods to mount the QFP package version.
Contact your Sanyo sales representative to discuss process conditions if techniques in which the whole package is immersed in a solder bath (solder dip or spray techniques) are used.

System Block Diagram



Differences between the LC66354B, LC66356B and LC66358B and the LC6630X Series

Parameter	LC6630X series (including the LC66599 evaluation chip)	LC6635XB series
System Differences • Hardware wait time (number of cycles) when HOLD mode is cleared	65536 cycles At 4 MHz (Tcyc = 1 µs): About 64 ms	16384 cycles At 4 MHz (Tcyc = 1 µs): About 16 ms
• Value of timer 0 on reset (including the value after HOLD mode is cleared)	The value FFO is loaded.	The value FFC is loaded.
Main differences in product characteristics • Operating power supply voltage/operating speed (cycle time)	LC66304A, 66306A, 66308A 4.0 to 6.0 V/0.92 to 10 µs LC66E308, 66P308 4.5 to 5.5 V/0.92 to 10 µs	3.0 to 5.5 V/0.92 to 10 µs LC6635XA, 2.2 to 5.5 V/3.92 to 10 µs, 3.0 to 5.5 V/1.96 to 10 µs

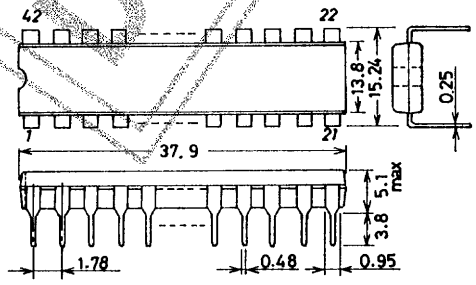
Note: 1. An RC oscillator cannot be used with the LC66354B, LC66356B and LC66358B.
2. In addition, there are differences in the output currents, comparator input voltages and other aspects. For details, refer to the individual catalogs for the LC66308A, LC66E308 and the LC66P308.
3. These points require care when using the LC66E308 or LC66P308 for evaluation purposes.

Package Dimensions

unit: mm

3025B-DIP42S

[LC66354B, 66356B, 66358B]

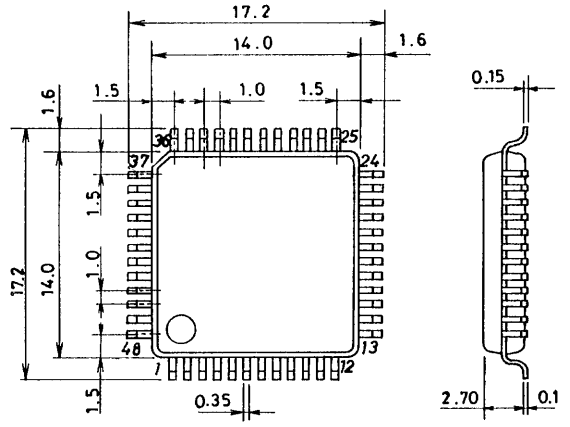


SANYO: DIP42S

unit: mm

3156-QFP48E

[LC66354B, 66356B, 66358B]



SANYO: QFP48E

Pin Function Overview

Pin	I/O	Overview	Output drive type	Option	Value on reset
P00 P01 P02 P03	I/O	I/O ports P00 to P03 • Input or output in 4-bit or 1-bit units • P00 to P03 have control functions in HALT mode.	• P-channel: pull-up MOS type • N-channel: intermediate sink current type	• Either with pull-up MOS or n-channel OD output • Reset output level	High or low level (option)
P10 P11 P12 P13	I/O	I/O ports P10 to P13 • Input or output in 4-bit or 1-bit units	• P-channel: pull-up MOS type • N-channel: intermediate sink current type	• Either with pull-up MOS or n-channel OD output • Reset output level	High or low level (option)
P20/SI0 P21/SO0 P22/$\overline{SCK0}$ P23/INT0	I/O	I/O ports P20 to P23 • Input or output in 4-bit or 1-bit units • P20 is also used as the serial input SI0 pin. • P21 is also used as the serial output SO0 pin. • P22 is also used as the serial clock $\overline{SCK0}$ pin. • P23 is also used as the INT0 interrupt request, the timer 0 event counter and pulse width measurement input.	• P-channel: CMOS type • N-channel: intermediate sink current type (+15 V withstand voltage in OD)	• Either CMOS or n-channel OD output	H
P30/$\overline{INT1}$ P31/POUT0 P32/POUT1	I/O	I/O ports P30 to P32 • Input or output in 3-bit or 1-bit units • P30 is also used as the $\overline{INT1}$ interrupt request. • P31 is also used for square wave output from timer 0. • P32 is also used for square wave output from timer 1 and PWM output.	• P-channel: CMOS type • N-channel: intermediate sink current type (+15 V withstand voltage in OD)	• Either CMOS or n-channel OD output	H
P33/$\overline{HOLD}$	I	Hold mode control input • Hold mode is entered if a HOLD instruction is executed when $\overline{HOLD}$ is low. • When in hold mode, the CPU is reactivated by setting $\overline{HOLD}$ to the high level. • P33 can also be used as an input port along with P30 to P32. • When P33/$\overline{HOLD}$ is low, the CPU will not be reset by a low level on $\overline{RES}$. Therefore, $\overline{RES}$ cannot be used in applications that set P33/$\overline{HOLD}$ low when power is first applied.			
P40 P41 P42 P43	I/O	I/O ports P40 to P43 • Input or output in 3-bit or 1-bit units • I/O in 8-bit units when used in conjunction with P50 to P53 • Output of 8-bit ROM data when used in conjunction with P50 to P53	• P-channel: pull-up MOS type • N-channel: intermediate sink current type (+15 V withstand voltage in OD)	• Either with pull-up MOS or n-channel OD output	H

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Pin	I/O	Overview	Output drive type	Option	Value on reset
P50 P51 P52 P53/$\overline{INT2}$	I/O	I/O ports P50 to P53 • Input or output in 4-bit or 1-bit units • I/O in 8-bit units when used in conjunction with P40 to P43 • Output of 8-bit ROM data when used in conjunction with P40 to P43 • P53 is also used for the INT2 interrupt request.	• P-channel: pull-up MOS type • N-channel: intermediate sink current type (+15 V withstand voltage in OD)	• Either with pull-up MOS or n-channel OD output	H
P60/SI1 P61/$\overline{SO1}$ P62/$\overline{SCK1}$ P63/PIN1	I/O	I/O ports P60 to P63 • Input or output in 4-bit or 1-bit units • P60 is also used as the serial input SI1 pin. • P61 is also used as the serial output $\overline{SO1}$ pin. • P62 is also used as the serial clock $\overline{SCK1}$ pin. • P63 is also used as the timer 1 event counter input.	• P-channel: CMOS type • N-channel: intermediate sink current type (+15 V withstand voltage in OD)	• Either CMOS or n-channel OD output	H
PC2/VREF0 PC3/VREF1	I/O	I/O ports PC2 and PC3 • Output in 4-bit or 1-bit units • PC2 is also used as the VREF0 comparator comparison voltage pin. • PC3 is also used as the VREF1 comparator comparison voltage pin.	• P-channel: CMOS type • N-channel: intermediate sink current type	• Either CMOS or n-channel OD output	H
PD0/CMP0 PD1/CMP1 PD2/CMP2 PD3/CMP3	I	Dedicated input ports PD0 to PD3 • Can be switched to use as comparator inputs under program control. The PD0 comparison voltage is VREF0. The PD1 to PD3 comparison voltage is VREF1. Comparisons can be specified in units of PD0, PD2, and PD2 and PD3 together.			Normal input
PE0/TRA PE1/TRB	I	Dedicated input ports • Can be switched to function as three-value inputs under program control.			Normal input
OSC1 OSC2	I O	System clock oscillator external connection When an external clock is used, leave OSC2 open and input the clock signal to OSC1.		• Selection of either ceramic oscillator or external clock input.	
$\overline{RES}$	I	System reset input The CPU is initialized if a low level is input to $\overline{RES}$ when the P33/$\overline{HOLD}$ pin is high.			
TEST	I	CPU test pin This pin must be connected to V_{SS} during normal operation.			
V_{DD} V_{SS}		Power supply connections			

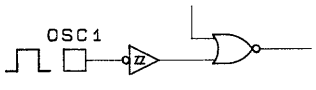
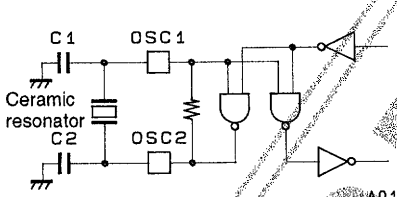
Note: Pull-up MOS output:.....A pull-up MOS transistor is connected to the output circuit.
CMOS output: .....Complementary output
OD output:.....Open drain output

User Option Types

1. Port 0 and 1 reset time output level option
   The output levels of ports 0 and 1 can be selected from the following two options in 4-bit units.

Option	Conditions and notes
High level output at reset time	Ports 0 and/or 1 in 4-bit sets
Low level output at reset time	Ports 0 and/or 1 in 4-bit sets

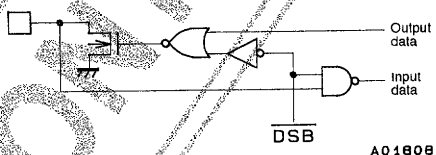
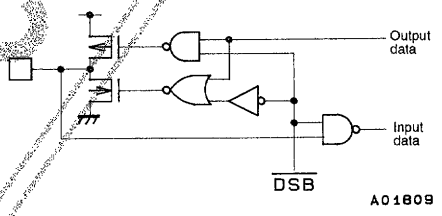
2. Oscillator circuit option

Option	Circuit	Conditions and notes
External clock		This input is a Schmitt specification input.
Ceramic oscillator		

Note: There is no RC oscillator option.

3. Watchdog timer option
   The presence or absence of a watchdog timer can be selected as an option.

4. Port output type option
   • One of the following two output circuit options can be selected for each bit in ports P0, P1, P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P4, P5. P6 and PC.

Option	Circuit	Conditions and notes
Open drain output		P2, P3, P5 and P6 are Schmitt inputs.
Built-in pull-up resistor output		P2, P3, P5 and P6 are Schmitt inputs. CMOS outputs (P2, P3, P6 and PC) and pull-up MOS outputs (P0, P1, P4 and P5) are differentiated according to the drive capacity of the p-channel transistor.

   • The PD comparator inputs and the PE three-value inputs are selected in software.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Applicable pins, notes	Conditions	Ratings	Unit	Note
Maximum supply voltage	V_{DD} max	V_{DD}		–0.3 to +7.0	V	
Input voltage	V_{IN} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P5, P6		–0.3 to +15.0	V	1
	V_{IN} (2)	Other inputs		–0.3 to V_{DD} + 0.3	V	2
Output voltage	V_{OUT} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P5, P6		–0.3 to +15.0	V	1
	V_{OUT} (2)	Other outputs		–0.3 to V_{DD} + 0.3	V	2
Output current per pin	I_{ON}	P0, P1, P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P5, P6, PC		20	mA	3
	$-I_{OP}$ (1)	P0, P1, P4, P5		2	mA	4
	$-I_{OP}$ (2)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6, PC		4	mA	4
Total pin current	ΣI_{ON} (1)	P0, P1, P2, P3, (except for the P33/$\overline{HOLD}$ pin), P40, P41		75	mA	3
	ΣI_{ON} (2)	P5, P6, P42, P43, PC		75	mA	3
	ΣI_{OP} (1)	P0, P1, P2, P3 (except for the P33/$\overline{HOLD}$ pin), P40, P41		25	mA	4
	ΣI_{OP} (2)	P5, P6, P42, P43, PC		25	mA	4
Allowable power dissipation	Pd max	Ta = –30 to +70°C	DIP42S	600	mW	
			QFP48E	430	mW	5
Operating temperature	Topr			–30 to +70	°C	
Storage temperature	Tstg			–55 to +125	°C	

Note: 1. Applies to open drain output specification pins. The rating from the "other pin" entry applies for specifications other than the open drain output specification.
2. Levels up to the free-running oscillation level are allowed for the oscillator input and output pins.
3. Inflow current
4. Outflow current (Applies to the pull-up output specification and CMOS output specification pins.)
5. We recommend using reflow soldering methods to mount the QFP package version.
Contact your Sanyo sales representative to discuss process conditions if techniques in which the whole package is immersed in a solder bath (solder dip or spray techniques) are used.

Allowable Operating Ranges at Ta = –30 to + 70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V unless otherwise specified

Parameter	Symbol	Applicable pins	Conditions	Ratings			Unit	Note
				min	typ	max		
Operating supply voltage	V_{DD}	V_{DD}	0.92 ≤ Tcyc ≤ 10 µs	3.0		5.5	V	
Memory hold supply voltage	V_{DD} (H)	V_{DD}	In HOLD mode	1.8		5.5	V	
Input high level Voltage	V_{IH} (1)	P2, P3 (except for the P33/HOLD pin), P4, P5, P6	With the output n-channel transistor off	0.8 V_{DD}		13.5	V	1
	V_{IH} (2)	P33/$\overline{HOLD}$, $\overline{RES}$, OSC1	With the output n-channel transistor off	0.8 V_{DD}		V_{DD}	V	2
	V_{IH} (3)	P0, P1, PC, PD, PE	With the output n-channel transistor off	0.75 V_{DD}		V_{DD}	V	3
	V_{IH} (4)	PE	Using three-value input	0.8 V_{DD}		V_{DD}	V	
Middle level input voltage	V_{IM}	PE	Using three-value input	0.4 V_{DD}		0.6 V_{DD}	V	
Common mode input voltage range	V_{CMM} (1)	PD0, PC2	Using comparator input	1.5		V_{DD}	V	
	V_{CMM} (2)	PD1, PD2, PD3, PC3		V_{SS}		V_{DD} – 1.5	V	
Input low level voltage	V_{IL} (1)	P2, P3 (except for the P33/HOLD pin), P5, P6, $\overline{RES}$, OSC1	With the output n-channel transistor off			0.2 V_{DD}	V	1
	V_{IL} (2)	P33/$\overline{HOLD}$	V_{DD} = 1.8 to 5.5 V			0.2 V_{DD}	V	
	V_{IL} (3)	P0, P1, P4, PC, PD, PE, TEST	With the output n-channel transistor off	V_{SS}		0.25 V_{DD}	V	3
	V_{IL} (4)	PE	Using comparator input	V_{SS}		0.2 V_{DD}	V	
Operating frequency (instruction cycle time)	f_{OP} (T_{CYC})			0.4 (10)		4.35 (0.92)	MHz (µs)	

Note: 1. Applies to open drain specification pins. However, the rating for V_{IH} (2) applies to the P33/$\overline{HOLD}$ pin. Ports P2, P3 and P6 cannot be used as input pins when CMOS output specifications are used.
2. Applies to open drain specification pins.
3. When PE is used as a three-value input, V_{IH} (4), V_{IM} and V_{IL} (4) apply. Port P3 cannot be used as input pins when CMOS output specifications are used.

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Parameter		Symbol	Applicable pins	Conditions	Ratings			Unit	Note
					min	typ	max		
External clock input conditions	Frequency	f_{ext}	OSC1	See Figure 1. With the signal input to OSC1 and with OSC2 open (with external clock input selected for the oscillator circuit option)	0.4		4.35	MHz	
	Pulse width	$t_{ext}H$ $t_{ext}L$		See Figure 1. With the signal input to OSC1 and with OSC2 open (with external clock input selected for the oscillator circuit option)	100			ns	
	Rise/fall times	$t_{ext}R$ $t_{ext}F$		See Figure 1. With the signal input to OSC1 and with OSC2 open (with external clock input selected for the oscillator circuit option)			30	ns	

Electrical Characteristics at Ta = –30 to + 70°C, V_{SS} = 0 V, V_{DD} = 3.5 to 5.5 V unless otherwise specified

Parameter		Symbol	Applicable pins	Conditions	Ratings			Unit	Note
					min	typ	max		
Input high level current		I_{IH} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P5, P6	V_{IN} = 13.5, With the output n-channel transistor off			5.0	µA	1
		I_{IH} (2)	P0, P1, PC, OSC1, $\overline{RES}$, P33/$\overline{HOLD}$	V_{IN} = V_{DD}, With the output n-channel transistor off			1.0	µA	1
		I_{IH} (3)	PD, PE, PC2, PC3	V_{IN} = V_{DD}, With the output n-channel transistor off			1.0	µA	1
Input low level current		I_{IL} (1)	Inputs other than PD, PE, PC2 and PC3	V_{IN} = V_{SS}, With the output n-channel transistor off	–1.0			µA	2
		I_{IL} (2)	PC2, PC3, PD, PE	V_{IN} = V_{SS}, With the output n-channel transistor off	–1.0			µA	2
Output high level voltage		V_{OH} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6, PC	I_{OH} = –1 mA	V_{DD} – 1.0			V	3
				I_{OH} = –0.1 mA	V_{DD} – 0.5				
		V_{OH} (2)	P0, P1, P4, P5	I_{OH} = –50 µA	V_{DD} – 1.0			V	4
				I_{OH} = –30 µA	V_{DD} – 0.5				
Output pull-up current		I_{PO}	P0, P1, P4, P5	V_{IN} = V_{SS}, V_{DD} = 5.5 V	–1.6			mA	4
Output low level voltage		V_{OL} (1)	P0, P1, P2, P3, P4, P5, P6, PC (except for the P33/$\overline{HOLD}$ pin)	I_{OL} = 1.6 mA			0.4	V	5
		V_{OL} (2)	P0, P1, P2, P3, P4, P5, P6, PC (except for the P33/$\overline{HOLD}$ pin)	I_{OL} = 8 mA			1.5	V	
Output off leakage current		I_{OFF} (1)	P2, P3, P4, P5, P6	V_{IN} = 13.5 V			5.0	µA	5
		I_{OFF} (2)	P0, P1, PC	V_{IN} = V_{DD}			1.0	µA	5
Comparator offset voltage		V_{OFF} (1)	PD1, PD2, PD3	V_{IN} = V_{SS} to V_{DD} – 1.5 V		±50	±300	mV	
		V_{OFF} (2)	PD0	V_{IN} = 1.5 to V_{DD}		±50	±300	mV	
Schmitt characteristics	Hysteresis voltage	V_{HIS}	P2, P3, P5, P6, OSC1 (EXT), $\overline{RES}$			0.1 V_{DD}		V	
	High level thresHOLD voltage	VtH			0.5 V_{DD}		0.8 V_{DD}	V	
	Low level thresHOLD voltage	VtL			0.2 V_{DD}		0.5 V_{DD}	V	

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Parameter			Symbol	Applicable pins		Conditions	Ratings min	Ratings typ	Ratings max	Unit	Note
Ceramic oscillator	Oscillator frequency		f_{CF}	OSC1, OSC2		Figure 2, 4 MHz		4.0		MHz	
	Oscillator stabilization time		f_{CFS}			Figure 3, 4 MHz			10	ms	
Serial clock	Cycle time	Input	t_{CKCY}	$\overline{SCK0}$, $\overline{SCK1}$		The timing from Figure 4 and the test load from Figure 5	0.9			µs	
		Output					2.0			Tcyc	
	Low level/ high level pulse widths	Input	t_{CKL}				0.4			µs	
		Output	t_{CKH}				1.0			Tcyc	
	Rise/ fall times	Output	t_{CKR} t_{CKF}						0.1	µs	
Serial input	Data setup time		t_{ICK}	SI0, SI1		Stipulated with respect to the rising edge timing for $\overline{SCK0}$ and $\overline{SCK1}$ from Figure 4	0.3			µs	
	Data hold time		t_{CKI}				0.3			µs	
Serial output	Output delay time		t_{CKO}	SO0, SO1		Stipulated with respect to the rising edge timing for $\overline{SCK0}$ and $\overline{SCK1}$ from Figure 4 and the test load shown in Figure 5			0.3	µs	
Pulse conditions	INT0 high/low level pulse widths		t_{IOH} t_{IOL}	INT0	Figure 6	• Conditions such that the INT0 interrupt is accepted • Conditions such that timer 0 event counter and pulse width measurement inputs are accepted.	2			Tcyc	
	High/low level pulse widths for interrupt inputs other than INT0		t_{IIH} t_{IIL}	$\overline{INT1}$, $\overline{INT2}$		• Conditions such that all interrupts are accepted	2			Tcyc	
	PIN1 high/low level pulse widths		t_{PINH} t_{PINL}	PIN1		• Conditions such that timer 1 event counter inputs are accepted.	2			Tcyc	
	$\overline{RES}$ high/low level pulse widths		t_{RSH} t_{RSL}	$\overline{RES}$		• Conditions such that reset occurs	3			Tcyc	
Comparator response speed			T_{RS}	PD	Figure 7				20	ms	
Operating mode current drain			$I_{DD\,OP}$	V_{DD}		Using a 4 MHz ceramic oscillator		3.0	5.0	mA	8
						Using a 4 MHz external clock		3.0	5.0	mA	
HALT mode current drain			I_{DDHALT}	V_{DD}		Using a 4 MHz ceramic oscillator		1.0	2.0	mA	
						Using a 4 MHz external clock		1.0	2.0	mA	
Hold-mode current drain			I_{DDHOLD}	V_{DD}		V_{DD} = 1.8 to 5.5 V		0.01	10	µA	

Note: 1. Common input and output ports with open-drain output specifications are specified for the state with the output n-channel transistor turned off. These pins cannot be used for input when the CMOS output specification option is selected.
2. Common input and output ports with open-drain output specifications are specified for the state with the output n-channel transistor turned off. Ratings for pull-up output specification pins are stipulated for the output pull-up current I_{PO}. These pins cannot be used for input when the CMOS output specification option is selected.
3. Stipulated for CMOS output specifications with the output n-channel transistor in the off state.
4. Stipulated for pull-up output specifications with the output n-channel transistor in the off state.
5. Stipulated for open-drain output specifications with the output n-channel transistor in the off state.
6. In the reset state

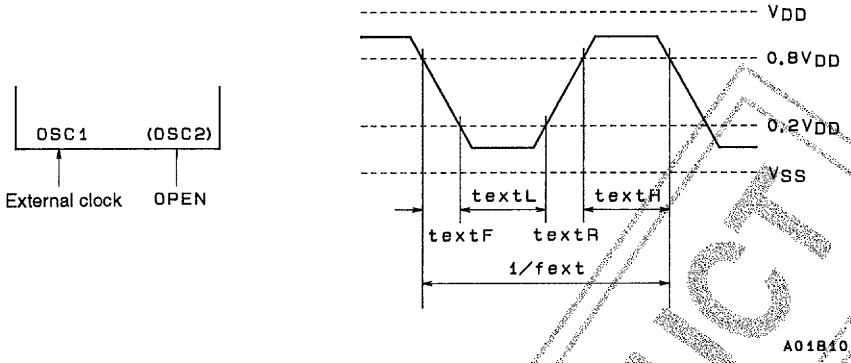


Figure 1 External Clock Input Waveform

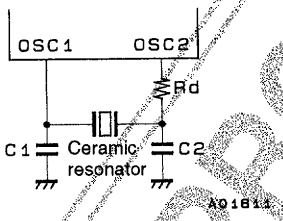


Figure 2 Ceramic Oscillator Circuit

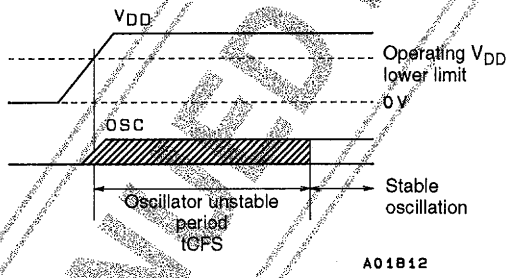


Figure 3 Oscillator Stabilization Time

Table 1 Ceramic Oscillator Guaranteed Constants

External capacitance type	2 MHz (Murata) CSA2.00MG	C1 = 33 pF ± 10%	2 MHz (Kyocera) KBR2.0MS	C1 = 47 pF ± 10%
		C2 = 33 pF ± 10%		C2 = 47 pF ± 10%
		Rd = 0 Ω		Rd = 0 Ω
	4 MHz (Murata) CSA4.00MG	C1 = 33 pF ± 10%	4 MHz (Kyocera) KBR4.0MS	C1 = 33 pF ± 10%
		C2 = 33 pF ± 10%		C2 = 33 pF ± 10%
		Rd = 0 Ω		Rd = 0Ω

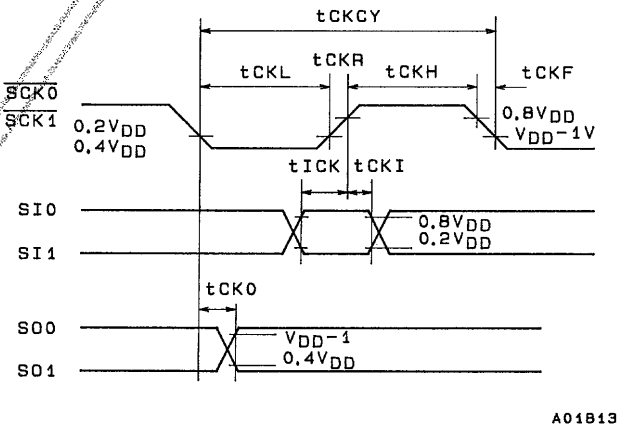


Figure 4 Serial I/O Timing

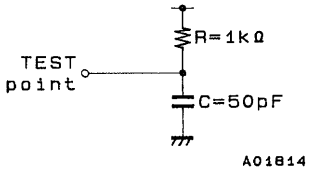


Figure 5 Timing Load

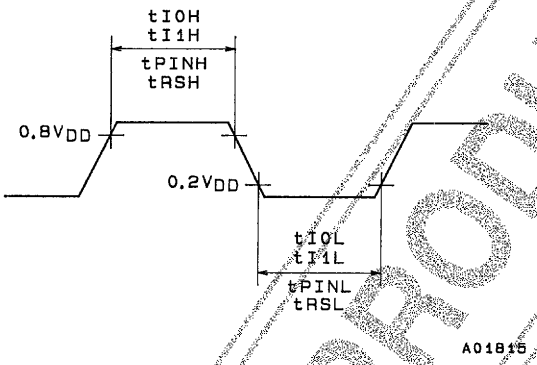


Figure 6 Input Timing for INT0, INT1, INT2, PIN1 and $\overline{RES}$

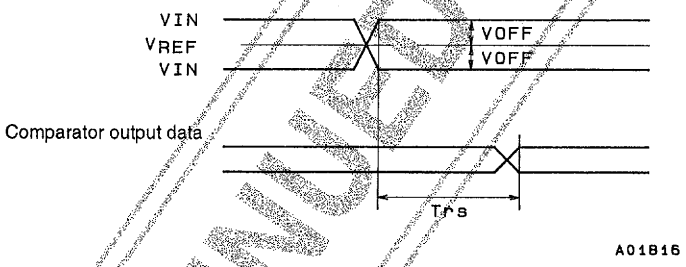
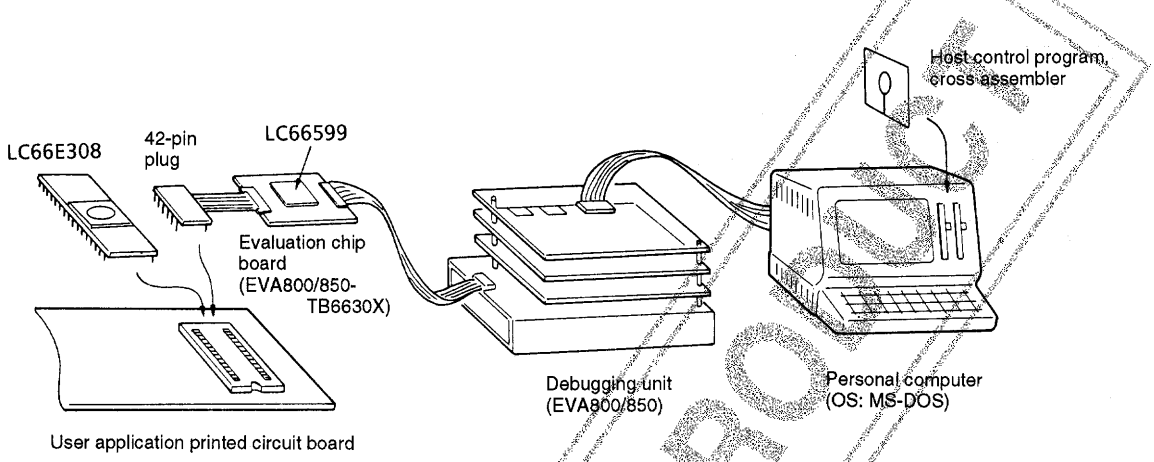


Figure 7 Comparator Response Speed Trs Timing

Application Development Tools

Programs for the LC66354B, LC66356B and LC66358B microcontrollers are developed on an IBM-PC compatible personal computer running the MS-DOS operating system. A cross assembler and other tools are available. To make application development more convenient, Sanyo also provides a program debugging unit (EVA800/850), an evaluation board (EVA800/850-TB6630X), an evaluation chip (LC66599) and an on-chip EPROM microprocessor (LC66E308).



Structure of the Application Development Tools

1. Program debugging unit (EVA800/850)
   This is an emulator that provides functions for EPROM writing and serial data communications with external equipment (such as a host computer). It supports application development in machine language and program modification. Its main debugging functions include breaking, stepping and tracing. (The MPM6630X is used for the EVA800/850 monitor ROM.)

2. Evaluation chip board (EVA800/850-TB6630X)
   The evaluation chip signals and ports are output to the 42-pin connector and when the output cable is connected, the evaluation chip board converts these signals to the same pin assignments as those on the mass production chip. The evaluation chip board includes jumpers for setting options and other states, and these jumper settings allow the evaluation chip to implement the same I/O circuit types and functions as the mass production chip. However, there are differences in the HOLD mode clear timing and the electrical characteristics.

   Jumper

Type	OSC		Reset method		Power supply to the user application board	
Jumper	Jumper 1 (J1)		Jumper 2 (J2: RES)		Jumper 3 (J3: V_{DD})	
Jumper setting and mode	EXT	External oscillator (external clock)	INT (a)	Reset by a RUN instruction from the host computer.	ON (a)	V_{DD} is supplied to the user application printed circuit board through the evaluation chip board.
	RC	RC oscillator				
	CF	CF oscillator	EXT (b)	Reset by the reset circuit on the user application printed circuit board.	OFF (b)	Separate power supplies on the user application printed circuit board and the evaluation chip board.

   Switches (SW9, SW10 and SW11)

Type	Port 0 and 1 output levels on reset				Watchdog timer presence or absence setting	
Switch	SW11: P0HL		SW10: P1HL		SW9: WDC	
Switch setting and mode	ON	Port 0 high	ON	Port 1 highPort 1 low	ON	Watchdog timer present
	OFF	Port 0 low	OFF		OFF	Watchdog timer absent

   Switches SW1 to SW8: Pull-up resistor option settings
   - Set the corresponding switch to the on position for built-in pull-up resistors, and set the switch to the off position for open drain output.
   - These settings can be specified for individual pins.

3. Cross Assembler

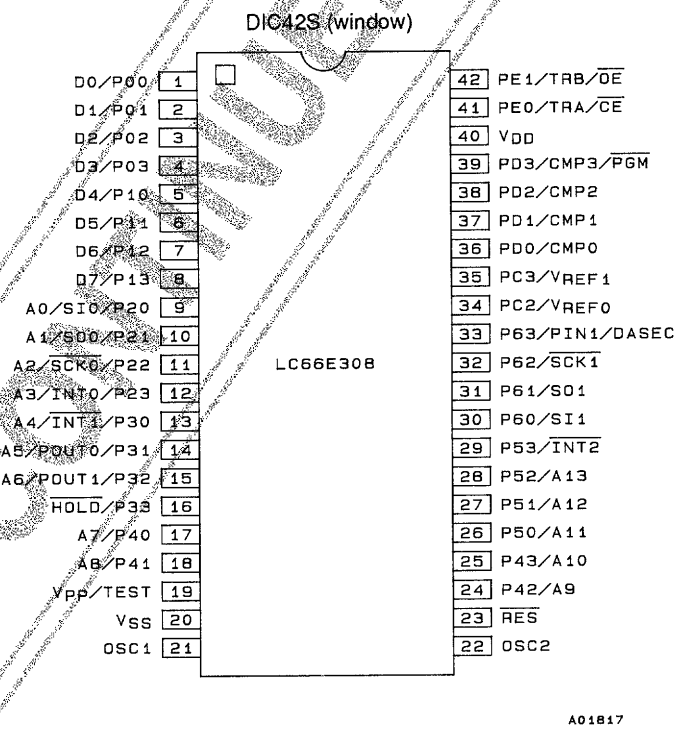
Cross assembler (file name)	Object microprocessors	Limitations on program creation
LC66S. EXE	LC66354B, 66356B, 66358B (LC66E308, 66P308) (LC66599)	SB instruction limitations • LC66354B : Only SB0 can be used. • LC66356B, 66358B : Only SB0 and SB1 can be used. (LC66E308, 66P308) • LC66599 : SB0, SB1, SB2 and SB3 can be used.

4. Simulation chip (See the LC66E308 individual product catalog for more details.)
The LC66E308 simulation chip is an on-chip EPROM microprocessor. Mounted configuration operation can be confirmed in the application product by using a dedicated conversion board (the W66EP308D/408D for DIP products and the W66EP308Q/408Q for QFP products) and writing programs with a commercial PROM writer.

- Form
The LC66E308 has a pin arrangement and functions identical to those of the LC66354B, LC66356B and LC66358B. However, there are differences in the HOLD mode clear timing and the electrical characteristics. The figure below shows the pin assignment.

- Options
The options (the port 0 and 1 level at reset, the watchdog timer and the port output circuit types) for the microprocessor to be evaluated can be specified by EPROM data. (The next item describes the option data area and definitions.) This allows evaluation with the same peripheral circuits as those that will be used in the mass production product.

Pin Assignment



Option Data Area and Definitions

ROM area	Bit	Option item		Relation between option and data
2000H	7 6 5	Unused		Must be set to zeros.
	4	Oscillator option		1 = ceramic oscillator 0 = external clock
	3	Unused		Must be set to zero.
	2	P1	Level of reset	1 = high level 0 = low level
	1	P0		
	0	Watchdog timer option		1 = present, 0 = absent
2001H	7	P13	Output circuit type	1 = PU, 0 = OD
	6	P12		
	5	P11		
	4	P10		
	3	P03		
	2	P02		
	1	P01		
	0	P00		
2002H	7	Unused		Must be set to zero.
	6	P32	Output circuit type	1 = PU, 0 = OD
	5	P31		
	4	P30		
	3	P23		
	2	P22		
	1	P21		
	0	P20		
2003H	7	P53	Output circuit type	1 = PU, 0 = OD
	6	P52		
	5	P51		
	4	P50		
	3	P43		
	2	P42		
	1	P41		
	0	P40		
2004H	7 to 4	Unused		
	3	P63	Output circuit type	1 = PU, 0 = OD
	2	P62		
	1	P61		
	0	P60		
2005H	7 to 0	Unused		Must be set to zero.
2006H	7 to 0	Unused		Must be set to zero.
2007H	7 to 4	Unused		Must be set to zero.
	3	PC3	Output circuit type	1 = PU, 0 = OD
	2	PC2		
	1 0	Unused		Must be set to zero.

LC663XX Series Instruction Table (by function)

Abbreviations:

AC: Accumulator
E: E register
CF: Carry flag
ZF: Zero flag
HL: Data pointer DPH, DPL
XY: Data pointer DPX, DPY
M: Data memory
M (HL): Data memory pointed to by the DPH, DPL data pointer
M (XY): Data memory pointed to by the DPX, DPY data pointer
M2 (HL): Two words of data memory (starting on an even address) pointed to by the DPH, DPL data pointer
SP: Stack pointer
M2 (SP): Two words of data memory pointed to by the stack pointer
M4 (SP): Four words of data memory pointed to by the stack pointer
in: n bits of immediate data
t2: Bit specification

t2	11	10	01	00
Bit	2^3	2^2	2^1	2^0

PCh: Bits 8 to 11 in the PC
PCm: Bits 4 to 7 in the PC
PCl: Bits 0 to 3 in the PC
Fn: User flag, n = 0 to 15
TIMER0: Timer 0
TIMER1: Timer 1
SIO: Serial register
P: Port
P (i4): Port indicated by 4 bits of immediate data
INT: Interrupt enable flag
( ), [ ]: Indicates the contents of a location
←: Transfer direction, result
∀: Exclusive or
∀: Logical and
∧: Logical or
+: Addition
–: Subtraction
—: Taking the one's complement

Instructions

Instruction group	Mnemonic		Instruction code								Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0						
Accumulator manipulation instructions	CLA	Clear AC	1	0	0	0	0	0	0	0	1	1	AC ← 0 (Equivalent to LAI0.)	Clear AC.	ZF	1
	DAA	Decimal adjust AC in addition	1 0	1 0	0 1	0 0	1 0	1 1	1 1	1 0	2	2	AC ← (AC) + 6 (Equivalent to ADI6.)	Add six to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 0	1 0	0 1	0 0	1 1	1 0	1 1	1 0	2	2	AC ← (AC) + 10 (Equivalent to ADIOAH.)	Add 10 to AC.	ZF	
	CLC	Clear CF	0	0	0	1	1	1	1	0	1	1	CF ← 0	Clear CF to 0.	CF	
	STC	Set CF	0	0	0	1	1	1	1	1	1	1	CF ← 1	Set CF to 1.	CF	
	CMA	Complement AC	0	0	0	1	1	0	0	0	1	1	AC ← $\overline{(AC)}$	Take the one's complement of AC.	ZF	
	IA	Increment AC	0	0	0	1	0	1	0	0	1	1	AC ← (AC) + 1	Increment AC.	ZF, CF	
	DA	Decrement AC	0	0	1	0	0	1	0	0	1	1	AC ← (AC) – 1	Decrement AC.	ZF, CF	
	RAR	Rotate AC right through CF	0	0	0	1	0	0	0	0	1	1	AC_3 ← (CF), ACn ← (ACn + 1), CF ← (AC_0)	Shift AC (including CF) right.	CF	
	RAL	Rotate AC left through CF	0	0	0	0	0	0	0	1	1	1	AC_0 ← (CF), ACn + 1 ← (ACn), CF ← (AC_3)	Shift AC (including CF) left.	CF, ZF	
	TAE	Transfer AC to E	0	1	0	0	0	1	0	1	1	1	E ← (AC)	Move the contents of AC to E.		
	TEA	Transfer E to AC	0	1	0	0	0	1	1	0	1	1	AC ← (E)	Move the contents of E to AC.	ZF	
	XAE	Exchange AC with E	0	1	0	0	0	1	0	0	1	1	(AC) ↔ (E)	Exchange the contents of AC and E.		
Memory manipulation instruction	IM	Increment M	0	0	0	1	0	0	1	0	1	1	M (HL) ← [M (HL)] + 1	Increment M (HL).	ZF, CF	
	DM	Decrement M	0	0	1	0	0	0	1	0	1	1	M (HL) ← [M (HL)] – 1	Decrement M (HL).	ZF, CF	
	IMDR i8	Increment M direct	1 I_7	1 I_6	0 I_5	0 I_4	0 I_3	1 I_2	1 I_1	1 I_0	2	2	M (i8) ← [M (i8)] + 1	Increment M (i8).	ZF, CF	
	DMDR i8	Decrement M direct	1 I_7	1 I_6	0 I_5	0 I_4	0 I_3	0 I_2	1 I_1	1 I_0	2	2	M (i8) ← [M (i8)] – 1	Decrement M (i8).	ZF, CF	
	SMB t2	Set M data bit	0	0	0	0	1	1	t_1	t_0	1	1	[M (HL), t2] ← 1	Set the bit in M (HL) specified by t0 and t1 to 1.		
	RMB t2	Reset M data bit	0	0	1	0	1	1	t_1	t_0	1	1	[M (HL), t2] ← 0	Clear the bit in M (HL) specified by t0 and t1 to 0.	ZF	
Arithmetic, logic and comparison instructions	AD	Add M to AC	0	0	0	0	0	1	1	0	1	1	AC ← (AC) + [M (HL)]	Add the contents of AC and M (HL) as two's complement values and store the result in AC.	ZF, CF	
	ADDR i8	Add M direct to AC	1 I_7	1 I_6	0 I_5	0 I_4	1 I_3	0 I_2	0 I_1	1 I_0	2	2	AC ← (AC) + [M (i8)]	Add the contents of AC and M (i8) as two's complement values and store the result in AC.	ZF, CF	
	ADC	Add M to AC with CF	0	0	0	0	0	0	1	0	1	1	AC ← (AC) + [M (HL)] + (CF)	Add the contents of AC, M (HL) and C as two's complement values and store the result in AC.	ZF, CF	
	ADI i4	Add immediate data to AC	1 0	1 0	0 1	0 0	1 I_3	1 I_2	1 I_1	1 I_0	2	2	AC ← (AC) + I_3, I_2, I_1, I_0	Add the contents of AC and the immediate data as two's complement values and store the result in AC.	ZF	
	SUBC	Subtract AC from M with CF	0	0	0	1	0	1	1	1	1	1	AC ← [M (HL)] – (AC) – $(\overline{CF})$	Subtract the contents of AC and $\overline{CF}$ from M (HL) as two's complement values and store the result in AC.	ZF, CF	2
	ANDA	And M with AC then store AC	0	0	0	0	0	1	1	1	1	1	AC ← (AC) ∀ [M (HL)]	Take the logical and of AC and M (HL) and store the result in AC.	ZF	

Note: 1. Has a vertical skip function.
2. CF will be zero if there was a borrow and one otherwise.

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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
			D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
Arithmetic, logic and comparison instructions	ORA	Or M with AC then store AC	0 0 0 0	0 1 0 1	1	1	AC ← (AC) ∨ [M (HL)]	Take the logical or of AC and M (HL) and store the result in AC.	ZF	
	EXL	Exclusive or M with AC then store AC	0 0 0 1	0 1 0 1	1	1	AC ← (AC) ∀ [M (HL)]	Take the logical exclusive or of AC and M (HL) and store the result in AC.	ZF	
	ANDM	And M with AC then store M	0 0 0 0	0 0 1 1	1	1	M (HL) ← (AC) ∧ [M (HL)]	Take the logical and of AC and M (HL) and store the result in M (HL).	ZF	
	ORM	Or M with AC then store M	0 0 0 0	0 1 0 0	1	1	M (HL) ← (AC) ∨ [M (HL)]	Take the logical or of AC and M (HL) and store the result in M (HL).	ZF	
	CM	Compare AC with M	0 0 0 1	0 1 1 0	1	1	$\overline{[M\ (HL)]}$ + (AC) + 1	Compare the contents of AC and M (HL) and set or clear CF and ZF according to the result. Magnitude comparison / CF / ZF [M (HL)] > (AC) 0 0 [M (HL)] = (AC) 1 1 [M (HL)] < (AC) 1 0	ZF, CF	
	CI i4	Compare AC wiht immediate data	1 1 0 0 1 0 1 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	$\overline{I_3\ I_2\ I_1\ I_0}$ + (AC) +1	Compare the contents of AC and the immediate data I_3 I_2 I_1 I_0 and set or clear CF and ZF according to the result. Magnitude comparison / CF / ZF I_3 I_2 I_1 I_0 > AC 0 0 I_3 I_2 I_1 I_0 = AC 1 1 I_3 I_2 I_1 I_0 < AC 1 0	ZF, CF	
	CLI i4	Compare DP_L with immediate data	1 1 0 0 1 0 1 1	1 1 1 1 I_3 I_2 I_1 I_0	2	2	ZF ← 1 if (DP_L) = I_3 I_2 I_1 I_0 ZF ← 0 if (DP_L) = I_3 I_2 I_1 I_0	Compare the contents of DP_L with the immediate data. Set ZF if identical and clear ZF if not.	ZF	
	CMB t2	Compare AC bit with M data bit	1 1 0 0 1 1 0 1	1 1 1 1 0 0 t_1 t_0	2	2	ZF ← 1 if (AC, t2) = [M (HL), t2] ZF ← 0 if (AC, t2) = [M (HL), t2]	Compare the corresponding bits specified by t_0 and t_1 in AC and M(HL). Set ZF if identical and clear ZF if not.	ZF	
Load and store instructions	LAE	Load AC and E from M2 (HL)	0 1 0 1	1 1 0 0	1	1	AC ← M (HL) E ← M (HL +1)	Load the contents of M2 (HL) into AC, E.		
	LAI i4	Load AC with immediate data	1 0 0 0	I_3 I_2 I_1 I_0	1	1	AC ← I_3 I_2 I_1 I_0	Load the immediate data into AC.	ZF	3
	LADR i8	Load AC from M direct	1 1 0 0 I_7 I_6 I_5 I_4	0 0 0 1 I_3 I_2 I_1 I_0	2	2	AC ← [M (i8)]	Load the contents of M (i8) into AC.	ZF	
	S	Store AC to M	0 1 0 0	0 1 1 1	1	1	M (HL) ← (AC)	Store the contents of AC into M (HL).		
	SAE	Store AC and E to M2 (HL)	0 1 0 1	1 1 1 0	1	1	M (HL) ← (AC) M (HL + 1) ← (E)	Store the contents of AC, E into M2(HL).		
	LA reg	Load AC from M (reg)	0 1 0 0	1 0 t_0 0	1	1	AC ← [M (reg)]	Load the contents of M (reg) into AC. The reg is either HL or XY depending on t0. reg / t_0 HL 0 XY 1	ZF	

Note: 3. Has a vertical skip function.

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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
			D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
Load and store instructions	LA reg, I	Load AC from M (reg) then increment reg	0 1 0 0	1 0 t_0 1	1	2	AC ← [M (reg)] DP_L ← (DP_L) + 1 or DP_Y ← (DP_Y) + 1	Load the contents of M (reg) into AC. (The reg is either HL or XY.) Then increment the contents of either DP_L or DP_Y. The relationship between t0 and reg is the same as that for the LA reg instruction.	ZF	4
	LA reg, D	Load AC from M (reg) then decrement reg	0 1 0 1	1 0 t_0 1	1	2	AC ← [M (reg)] DP_L ← (DP_L) – 1 or DP_Y ← (DP_Y) – 1	Load the contents of M (reg) into AC. (The reg is either HL or XY.) Then decrement the contents of either DP_L or DP_Y. The relationship between t_0 and reg is the same as that for the LA reg instruction.	ZF	5
	XA reg	Exchange AC with M (reg)	0 1 0 0	1 1 t_0 0	1	1	(AC) ↔ [M (reg)]	Exchange the contents of M (reg) and AC. The reg is either HL or XY depending on t_0. reg: HL, XY; t_0: 0, 1		
	XA reg, I	Exchange AC with M (reg) then increment reg	0 1 0 0	1 1 t_0 1	1	2	(AC) ↔ [M (reg)] DP_L ← (DP_L) + 1 or DP_Y ← (DP_Y) + 1	Exchange the contents of M (reg) and AC. (The reg is either HL or XY.) Then increment the contents of either DP_L or DP_Y. The relationship between t0 and reg is the as that for the XA reg instruction.	ZF	6
	XA reg, D	Exchange AC with M (reg) then decrement reg	0 1 0 1	1 1 t_0 1	1	2	(AC) ↔ [M (reg)] DP_L ← (DP_L) – 1 or DP_Y ← (DP_Y) – 1	Exchange the contents of M (reg) and AC. (The reg is either HL or XY.) Then decrement the contents of either DP_L or DP_Y. The relationship between t0 and reg is the as that for the XA reg instruction.	ZF	7
	XADR i8	Exchange AC with M direct	1 1 0 0 I_7 I_6 I_5 I_4	1 0 0 0 I_3 I_2 I_1 I_0	2	2	(AC) ↔ [M (i8)]	Exchange the contents of AC with M (i8).		
	LEAI i8	Load E & AC with immediate data	1 1 0 0 I_7 I_6 I_5 I_4	0 1 1 0 I_3 I_2 I_1 I_0	2	2	E ← I_7 I_6 I_5 I_4 AC ← I_3 I_2 I_1 I_0	Load the immediate data i8 into E, AC.		
	RTBL	Read table data from program ROM	0 1 0 1	1 0 1 0	1	2	E, AC ← [ROM (PCh, E, AC)]	Load into E, AC the ROM data at the location determined by replacing the lower 8 bits of the PC with E, AC.		
	RTBLP	Read table data from program ROM then output to P4, 5	0 1 0 1	1 0 0 0	1	2	Port 4, 5 ← [ROM (PCh, E, AC)]	Output from ports 4 and 5 the ROM data at the location determined by replacing the lower 8 bits of the PC with E, AC.		

Note: 4. ZF is set according to the result of incrementing DP_L or DP_Y.
5. ZF is set according to the result of decrementing DP_L or DP_Y.
6. ZF is set according to the result of incrementing DP_L or DP_Y.
7. ZF is set according to the result of decrementing DP_L or DP_Y.

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Instruction group	Mnemonic		Instruction code								Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0						
Data pointer manipulation instructions	LDZ i4	Load DP_H with zero and DP_L with immediate data respectively	0	1	1	0	I_3	I_2	I_1	I_0	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3\ I_2\ I_1\ I_0$	Load zero into DP_H and the immediate data i4 into DP_L.		
	LHI i4	Load DP_H with immediate data	1 0	1 0	0 0	0 0	1 I_3	1 I_2	1 I_1	1 I_0	2	2	$DP_H \leftarrow I_3\ I_2\ I_1\ I_0$	Load the immediate data i4 into DP_H.		
	LLI i4	Load DP_L with immediate data	1 0	1 0	0 0	0 1	1 I_3	1 I_2	1 I_1	1 I_0	2	2	$DP_L \leftarrow I_3\ I_2\ I_1\ I_0$	Load the immediate data i4 into DP_L.		
	LHLI i8	Load DP_H, DP_L with immediate data	1 I_7	1 I_6	0 I_5	0 I_4	0 I_3	0 I_2	0 I_1	0 I_0	2	2	$DP_H \leftarrow I_7\ I_6\ I_5\ I_4$ $DP_L \leftarrow I_3\ I_2\ I_1\ I_0$	Load the immediate data into DL_H, DP_L.		
	LXYI i8	Load DP_X, DP_Y with immediate data	1 I_7	1 I_6	0 I_5	0 I_4	0 I_3	0 I_2	1 I_1	0 I_0	2	2	$DP_X \leftarrow I_7\ I_6\ I_5\ I_4$ $DP_Y \leftarrow I_3\ I_2\ I_1\ I_0$	Load the immediate data into DL_X, DP_Y.		
	IL	Increment DP_L	0	0	0	1	0	0	0	1	1	1	$DP_L \leftarrow (DP_L) + 1$	Increment the contents . of DP_L	ZF	
	DL	Decrement DP_L	0	0	1	0	0	0	0	1	1	1	$DP_L \leftarrow (DP_L) - 1$	Decrement the contents of DP_L.	ZF	
	IY	Increment DP_Y	0	0	0	1	0	0	1	1	1	1	$DP_Y \leftarrow (DP_Y) + 1$	Increment the contents of DP_Y.	ZF	
	DY	Decrement DP_Y	0	0	1	0	0	0	1	1	1	1	$DP_Y \leftarrow (DP_Y) - 1$	Decrement the contents of DP_Y.	ZF	
	TAH	Transfer AC to DP_H	1 1	1 1	0 1	0 1	1 0	1 0	1 0	1 0	2	2	$DP_H \leftarrow (AC)$	Transfer the contents of AC to DP_H.		
	THA	Transfer DP_H to AC	1 1	1 1	0 1	0 0	1 0	1 0	1 0	1 0	2	2	$AC \leftarrow (DP_H)$	Transfer the contents of DP_H . to AC	ZF	
	XAH	Exchange AC with DP_H	0	1	0	0	0	0	0	0	1	1	$(AC) \leftrightarrow (DP_H)$	Exchange the contents of AC and DP_H.		
	TAL	Transfer AC to DP_L	1 1	1 1	0 1	0 1	1 0	1 0	1 0	1 1	2	2	$DP_L \leftarrow (AC)$	Transfer the contents of AC to DP_L.		
	TLA	Transfer DP_L to AC	1 1	1 1	0 1	0 0	1 0	1 0	1 0	1 1	2	2	$AC \leftarrow (DP_L)$	Transfer the contents of DP_L to AC.	ZF	
	XAL	Exchange AC with DP_L	0	1	0	0	0	0	0	1	1	1	$(AC) \leftrightarrow (DP_L)$	Exchange the contents of AC and DP_L.		
	TAX	Transfer AC to DP_X	1 1	1 1	0 1	0 1	1 0	1 0	1 1	1 0	2	2	$DP_X \leftarrow (AC)$	Transfer the contents of AC to DP_X.		
	TXA	Transfer DP_X to AC	1 1	1 1	0 1	0 0	1 0	1 0	1 1	1 0	2	2	$AC \leftarrow (DP_X)$	Transfer the contents of DP_X to AC.	ZF	
	XAX	Exchange AC with DP_X	0	1	0	0	0	0	1	0	1	1	$(AC) \leftrightarrow (DP_X)$	Exchange the contents of AC and DP_X.		
	TAY	Transfer AC to DP_Y	1 1	1 1	0 1	0 1	1 0	1 0	1 1	1 1	2	2	$DP_Y \leftarrow (AC)$	Transfer the contents of AC to DP_Y.		
	TYA	Transfer DP_Y to AC	1 1	1 1	0 1	0 0	1 0	1 0	1 1	1 1	2	2	$AC \leftarrow (DP_Y)$	Transfer the contents of DP_Y to AC.	ZF	
	XAY	Exchange AC with DP_Y	0	1	0	0	0	0	1	1	1	1	$(AC) \leftrightarrow (DP_Y)$	Exchange the contents of AC and DP_Y		
Flag manipulation instructions	SFB n4	Set flag bit	0	1	1	1	n_3	n_2	n_1	n_0	1	1	$Fn \leftarrow 1$	Set the flag specified by n4 to 1.		
	RFB n4	Reset flag bit	0	0	1	1	n_3	n_2	n_1	n_0	1	1	$Fn \leftarrow 0$	Clear the flag specified by n4 to 0.	ZF	

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Instruction group	Mnemonic		Instruction code D_7 D_6 D_5 D_4	Instruction code D_3 D_2 D_1 D_0	Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
Jump and subroutine instructions	JMP addr	Jump in the current bank	1 1 1 0 P_7 P_6 P_5 P_4	P_{11} P_{10} P_9 P_8 P_3 P_2 P_1 P_0	2	2	PC12 ← PC12 PC11 to 0 ← P_{11} to P_0	Jump to the location in the same bank specified by the immediate data P12.		8
	JPEA	Jump to the address stored at E and AC in the current page	0 0 1 0	0 1 1 1	1	1	PC12 to PC8 ← PC12 to PC8 PC7 to 4 ← (E) PC3 to 0 ← (AC)	Jump to the location determined by replacing the lower 8 bits of the PC by E, AC.		
	CAL addr	Call subroutine	0 1 0 1 P_7 P_6 P_5 P_4	0 P_{10} P_9 P_8 P_3 P_2 P_1 P_0	2	2	PC12, 11 ← 0 PC10 to 0 ← P_{10} to P_0 M4 (SP) ← (CF, ZF, PC12 to 0) SP ← (SP) – 4	Call a subroutine.		
	CZP addr	Call subroutine in the zero page	1 0 1 0	P_3 P_2 P_1 P_0	1	2	PC12 to 6, PC1 to 0 ← 0 PC5 to 2 ← P_3 to P_0 M4 (SP) ← (CF, ZF, PC12 to 0) SP ← SP – 4	Call a subroutine on page 0 in bank 0.		
	BANK	Change bank	0 0 0 1	1 0 1 1	1	1		Change the memory bank and register bank.		
	PUSH reg	Push reg on M2 (SP)	1 1 0 0 1 1 1 1	1 1 1 1 1 i_1 i_0 0	2	2	M2 (SP) ← (reg) SP ← (SP) – 2	Store the contents of reg in M2 (SP). Subtract 2 from SP after the store. reg: HL (i_1 i_0 = 0 0), XY (0 1), AE (1 0), Illegal setting (1 1)		
	POP reg	Pop reg off M2 (SP)	1 1 0 0 1 1 1 0	1 1 1 1 1 i_1 i_0 0	2	2	SP ← (SP) + 2 reg ← [M2 (SP)]	Add 2 to SP and then load the contents of M2 (SP) into reg. The relation between i_1 i_0 and reg is the same as that for the PUSH reg instruction.		
	RT	Return from subroutine	0 0 0 1	1 1 0 0	1	2	SP ← (SP) + 4 PC ← [M4 (SP)]	Return from a subroutine or interrupt handling routine. ZF and CF are not restored.		
	RTI	Return from interrupt routine	0 0 0 1	1 1 0 1	1	2	SP ← (SP) + 4 PC ← [M4 (SP)] CF, ZF ← [M4 (SP)]	Return from a subroutine or interrupt handling routine. ZF and CF are restored.	ZF, CF	
Branch instructions	BAt2 addr	Branch on AC bit	1 1 0 1 P_7 P_6 P_5 P_4	0 0 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if (AC, t2) = 1	Branch to the location in the same page specified by P_0 to P_7 if the bit in AC specified by the immediate data t_1 t_0 is one.		
	MNAt2 addr	Branch on no AC bit	1 0 0 1 P_7 P_6 P_5 P_4	0 0 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if (AC, t2) = 0	Branch to the location in the same page specified by P_0 to P7 if the bit in AC specified by the immediate data t_1 t_0 is zero.		
	BMt2 addr	Branch on M bit	1 1 0 1 P_7 P_6 P_5 P_4	0 1 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if [M (HL), t2] = 1	Branch to the location in the same page specified by P_0 to P_7 if the bit in M (HL) specified by the immediate data t_1 t_0 is one.		
	BNMt2 addr	Branch on no M bit	1 0 0 1 P_7 P_6 P_5 P_4	0 1 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if [M (HL), t2] = 0	Branch to the location in the same page specified by P_0 to P_7 if the bit in M (HL) specified by the immediate data t_1 t_0 is zero.		

Note: 8. This becomes PC12 + (PC12) immediately following a BANK instruction.

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Instruction group	Mnemonic		Instruction code D_7 D_6 D_5 D_4	Instruction code D_3 D_2 D_1 D_0	Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
Branch instructions	BPt2 addr	Branch on port bit	1 1 0 1 P_7 P_6 P_5 P_4	1 0 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if [P (DP_L), t2] = 1	Branch to the location in the same page specified by P_0 to P_7 if the bit in port (DP_L) specified by the immediate data t_1 t_0 is one.		9
	BNPt2 addr	Branch on no port bit	1 0 0 1 P_7 P_6 P_5 P_4	1 0 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if [P (DP_L), t2] = 0	Branch to the location in the same page specified by P_0 to P_7 if the bit in port (DP_L) specified by the immediate data t_1 t_0 is zero.		9
	BC addr	Branch on CF	1 1 0 1 P_7 P_6 P_5 P_4	1 1 0 0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if (CF) = 1	Branch to the location in the same page specified by P_0 to P_7 if CF is one.		
	BNC addr	Branch on no CF	1 0 0 1 P_7 P_6 P_5 P_4	1 1 0 0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if (CF) = 0	Branch to the location in the same page specified by P_0 to P_7 if CF is zero.		
	BZ addr	Branch on ZF	1 1 0 1 P_7 P_6 P_5 P_4	1 1 0 1 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if (ZF) = 1	Branch to the location in the same page specified by P_0 to P_7 if ZF is one.		
	BNZ addr	Branch on no ZF	1 0 0 1 P_7 P_6 P_5 P_4	1 1 0 1 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if (ZF) = 0	Branch to the location in the same page specified by P_0 to P_7 if ZF is zero.		
	BFn4 addr	Branch on flag bit	1 1 1 1 P_7 P_6 P_5 P_4	n_3 n_2 n_1 n_0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if (Fn) = 1	Branch to the location in the same page specified by P_0 to P_7 if the flag (of the 16 user flags) specified by n_3 n_2 n_1 n_0 is one.		
	BNFn4 addr	Branch on no flag bit	1 0 1 1 P_7 P_6 P_5 P_4	n_3 n_2 n_1 n_0 P_3 P_2 P_1 P_0	2	2	PC7 to 0 ← P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if (Fn) = 0	Branch to the location in the same page specified by P_0 to P_7 if the flag (of the 16 user flags) specified by n_3 n_2 n_1 n_0 is zero.		
I/O instructions	IP0	Input port 0 to AC	0 0 1 0	0 0 0 0	1	1	AC ← (P0)	Input the contents of port 0 to AC.	ZF	
	IP	Input port to AC	0 0 1 0	0 1 1 0	1	1	AC ← [P (DP_L)]	Input the contents of port P (DP_L) to AC.	ZF	
	IPM	Input port to M	0 0 0 1	1 0 0 1	1	1	M (HL) ← [P (DP_L)]	Input the contents of port P (DP_L) to M (HL).		
	IPDR i4	Input port to AC direct	1 1 0 0 0 1 1 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	AC ← [P (i4)]	Input the contents of P (i4) to AC.	ZF	
	IP45	Input port 4, 5 to E, AC respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 0	2	2	E ← [P (4)] AC ← [P (5)]	Input the contents of ports P (4) and P (5) to E and AC respectively.		
	OP	Output AC to port	0 0 1 0	0 1 0 1	1	1	P (DP_L) ← (AC)	Output the contents of AC to port P (DP_L).		
	OPM	Output M to port	0 0 0 1	1 0 1 0	1	1	P (DP_L) ← [M (HL)]	Output the contents of M (HL) to port P (DP_L).		
	OPDR i4	Output AC to port direct	1 1 0 0 0 1 1 1	1 1 1 1 I_3 I_2 I_1 I_0	2	2	P (i4) ← (AC)	Output the contents of AC to P (i4).		
	OP45	Output E, AC to port 4, 5 respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 1	2	2	P (4) ← (E) P (5) ← (AC)	Output the contents of E and AC to ports P (4) and P (5) respectively.		

Note: 9. Internal control registers can also be tested by executing this instruction immediately after a BANK instruction. However, this is limited to registers that can be read out.

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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
			D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
I/O instructions	SPB t2	Set port bit	0 0 0 0	1 0 t_1 t_0	1	1	[P (DP_L), t2] ← 1	Set to one the bit in port P (DP_L) specified by the immediate data t_1 t_0.		
	RPB t2	Reset port bit	0 0 1 0	1 0 t_1 t_0	1	1	[P (DP_L), t2] ← 0	Clear to zero the bit in port P (DP_L) specified by the immediate data t_1 t_0.	ZF	
	ANDPDR i4, p4	And port with immediate data then output	1 1 0 0 I_3 I_2 I_1 I_0	0 1 0 1 P_3 P_2 P_1 P_0	2	2	P (P_3 to P_0) ← [P (P_3 to 0)] ∨ $I_{3\ to\ 0}$	Take the logical and of P (P_3 to P_0) and the immediate data I_3 I_2 I_1 I_0 and output the result to P (P_3 to P_0).	ZF	
	ORPDR i4, p4	Or port with immediate data then output	1 1 0 0 I_3 I_2 I_1 I_0	0 1 0 0 P_3 P_2 P_1 P_0	2	2	P (P_3 to P_0) ← [P (P_3 to 0)] ∨ $I_{3\ to\ 0}$	Take the logical or of P (P_3 to P_0) and the immediate data I_3 I_2 I_1 I_0 and output the result to P (P_3 to P_0).	ZF	
Timer control instructions	WTTM0	Write timer 0	1 1 0 0	1 0 1 0	1	2	TIMER0 ← [M2 (HL)], (AC)	Write the contents of M2 (HL), AC into the timer 0 reload register.		
	WTTM1	Write timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 0	2	2	TIMER1 ← (E), (AC)	Write the contents of E, AC into the timer 1 reload register A.		
	RTIM0	Read timer 0	1 1 0 0	1 0 1 1	1	2	M2 (HL), AC ← (TIMER0)	Read out the contents of the timer 0 counter into M2 (HL), AC.		
	RTIM1	Read timer1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 1	2	2	E, AC ← (TIMER1)	Read out the contents of the timer 1 counter into E, AC.		
	START0	Start timer 0	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 0	2	2	Start timer 0 counter	Start the timer 0 counter.		
	START1	Start timer 1	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 1	2	2	Start timer 1 counter	Start the timer 1 counter.		
	STOP1	Stop timer 0	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 0	2	2	Stop timer 0 counter	Stop the timer 0 counter.		
	STOP1	Stop timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 1	2	2	Stop timer 1 counter	Stop the timer 1 counter.		
Interrupt control instructions	MSET	Set interrupt master enable flag	1 1 0 0 0 1 0 1	1 1 0 1 0 0 0 0	2	2	MSE ← 1	Set the interrupt master enable flag to one.		
	MRESET	Reset interrupt master enable flag	1 1 0 0 1 0 0 1	1 1 0 1 0 0 0 0	2	2	MSE ← 0	Clear the interrupt master enable flag to zero.		
	EIH i4	Enable interrupt high	1 1 0 0 0 1 0 1	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIH ← (EDIH) ∨ i4	Set the interrupt enable flag to one.		
	EIL i4	Enable interrupt low	1 1 0 0 0 1 0 0	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIL ← (EDIL) ∨ i4	Set the interrupt enable flag to one.		
	DIH i4	Disable interrupt high	1 1 0 0 1 0 0 1	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIH ← (EDIL) ∧ $\overline{i4}$	Clear the interrupt enable flag to zero.	ZF	
	DIL i4	Disable interrupt low	1 1 0 0 1 0 0 0	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIL ← (EDIL) ∧ $\overline{i4}$	Clear the interrupt enable flag to zero.	ZF	
	WTSP	Write SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 0	2	2	SP ← (E), (AC)	Transfer the contents of E, AC to SP.		
	RSP	Read SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 1	2	2	E, AC ← (SP)	Transfer the contents of SP to E, AC.		
Standby control instructions	HALT	HALT	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 0	2	2	HALT	Enter halt mode.		
	HOLD	HOLD	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 1	2	2	HOLD	Enter HOLD mode.		

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Instruction group	Mnemonic		Instruction code								Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0						
Serial I/O control instructions	STARTS	Start serial IO	1 1	1 1	0 1	0 0	1 1	1 1	1 1	1 0	2	2	START SI O	Start SIO operation.		
	WTSIO	Write serial IO	1 1	1 1	0 1	0 0	1 1	1 1	1 1	1 1	2	2	SIO ← (E), (AC)	Write the contents of E, AC to SIO.		
	RSIO	Read serial IO	1 1	1 1	0 1	0 1	1 1	1 1	1 1	1 1	2	2	E, AC ← (SIO)	Read the contents of SIO into E, AC.		
Other instructions	NOP	No operation	0	0	0	0	0	0	0	0	1	1	No operation	Consume one machine cycle without performing any operation.		
	SB i2	Select bank	1 1	1 1	0 0	0 0	1 0	1 0	1 I_1	1 I_0	2	2	PC12 ← I_1 I_0	Specify the memory bank.		