



LB1980

3-Phase Brushless Motor Driver for VCR Capstan Motors

Overview

The LB1980 is a 3-phase brushless motor driver IC that is particularly well suited for driving VCR capstan motors.

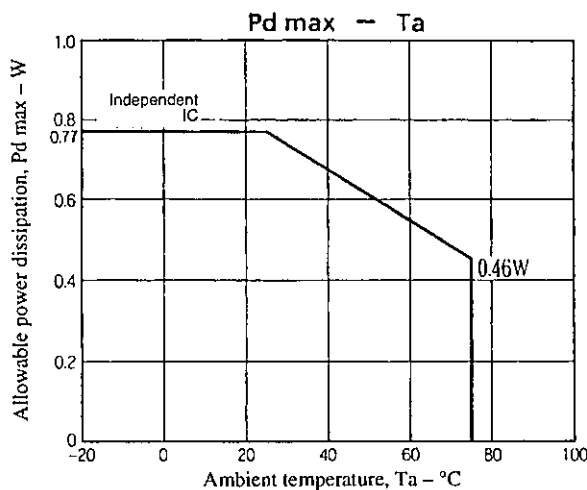
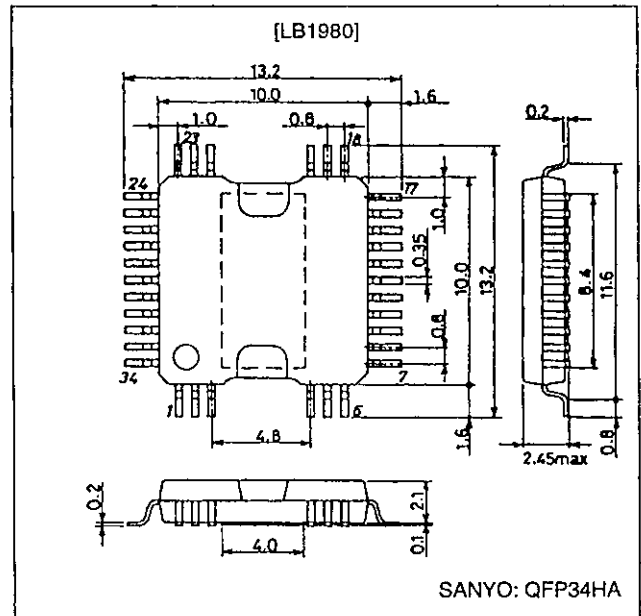
Functions

- Three-phase full wave current linear drive
- Torque ripple correction circuit with variable correction ratio
- Current limiter circuit
- Output stage up/down oversaturation protection circuit (no external capacitor required)
- FG amplifier
- Thermal shutdown circuit

Package Dimensions

unit: mm

3206A-QFP34HA



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7	V
	V _S max		24	V
Maximum output current	I _O max		1.3	A
Allowable power dissipation	Pd max	With an arbitrarily large heat sink	12.5	W
		Independent IC	0.77	W
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _S		5 to 22	V
	V _{CC}		4.5 to 5.5	V
Hall input amplitude	V _{HALL}	Between Hall inputs	±30 to ±80	mVo-p
GSENSE input range	V _{GSENSE}	With respect to the control system ground	-0.20 to +0.20	V

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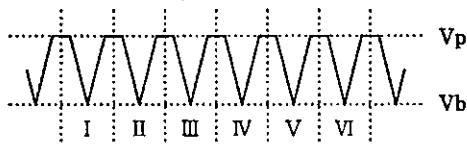
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Electrical Characteristics at Ta = 25°C, VCC = 5 V, VS = 15 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VCC current drain	I _{CC}	R _L = ∞, V _{CTL} = 0 V, V _{LIM} = 0 V(When stopped)	-	12	18	mA
[Output]						
Output saturation voltage	V _{o(sat)1}	I _O = 500 mA, R _f = 0.5 Ω, Sink + Source V _{CTL} = V _{LIM} = 5 V(With saturation protection)	-	2.1	2.6	V
	V _{o(sat)2}	I _O = 1.0 A, R _f = 0.5 Ω, Sink + Source V _{CTL} = V _{LIM} = 5 V(With saturation protection)	-	2.6	3.5	V
Output leakage current	I _{o leak}		-	-	1.0	mA
[FR]						
FR pin input threshold voltage	V _{FSR}		2.25	2.50	2.75	V
FR pin input bias current	I _{b(FSR)}		-5.0	-	-	μA
[Control]						
CTLREF pin voltage	V _{CREF}		2.05	2.15	2.25	V
CTLREF pin input range	V _{CREFIN}		1.50	-	3.50	V
CTL pin input bias current	I _{b(CTL)}	V _{CTL} = 5 V, with CTLREF open	-	-	4.0	μA
CTL control start voltage	V _{CTL(ST)}	With R _f = 0.5 Ω, V _{LIM} = 5 V, I _O ≥ 10 mA With the Hall input logic fixed(u, v, w = H, H, L)	2.00	2.15	2.30	V
CTL pin control Gm	G _{m(CTL)}	With R _f = 0.5 Ω, ΔI _O = 200 mA With the Hall input logic fixed(u, v, w = H, H, L)	0.46	0.58	0.70	A/V
[Current Limiter]						
LIM current limiter offset voltage	V _{off(LIM)}	With R _f = 0.5 Ω, V _{CTL} = 5 V, I _O ≥ 10 mA With the Hall input logic fixed(u, v, w = H, H, L)	140	200	260	mV
LIM pin input bias current	I _{b(LIM)}	V _{CTL} = 5 V, CTLREF: OPEN, V _{LIM} = 0 V	-2.5	-	-	μA
LIM pin current limit level	I _{lim}	With R _f = 0.5 Ω, V _{CTL} = 5 V, V _{LIM} = 20.6 V With the Hall input logic fixed(u, v, w = H, H, L)	830	900	970	mA
[Hall Amplifier]						
Hall amplifier input offset voltage	V _{off(HALL)}		-6	-	+6	mV
Hall amplifier input bias current	I _{b(HALL)}		-	1.0	3.0	μA
Hall amplifier common-mode input voltage	V _{cm(HALL)}		1.3	-	3.3	V
[TRC]						
Torque ripple correction ratio	TRC	For the troughs and peaks in the R _f waveform at I _O = 200 mA(R _f = 0.5 Ω, ADJ: open)(note 1)	-	9	-	%
ADJ pin voltage	V _{adj}		2.37	2.50	2.63	V
[FG Amplifier]						
FG amplifier input offset voltage	V _{off(FG)}		-8	-	+8	mV
FG amplifier input bias current	I _{b(FG)}		-100	-	-	nA
FG amplifier output saturation voltage	V _{o(sat)(FG)}	For the sink side and the internal pull-up resistor load	-	-	0.5	V
FG amplifier voltage gain	V _{G(FG)}	For open loop at f = 10 kHz	41.5	44.5	47.5	dB
FG amplifier common-mode input voltage	V _{CM(FG)}		0.5	-	4.0	V
[Saturation]						
Saturation prevention circuit lower side voltage setting	V _{o(sat)(DET)}	I _O = 10 mA, R _f = 0.5 ΩThe voltage between each OUT and R _f when V _{CTL} = V _{LIM} = 5 V.	0.175	0.25	0.325	V
[TSD]						
TSD operating temperature	T-TSD	(Design target value)*	-	180	-	°C
TSD temperature hysteresis	ΔTSD	(Design target value)*	-	20	-	°C

Notes: *Items marked with an asterisk are design target values and are not measured.

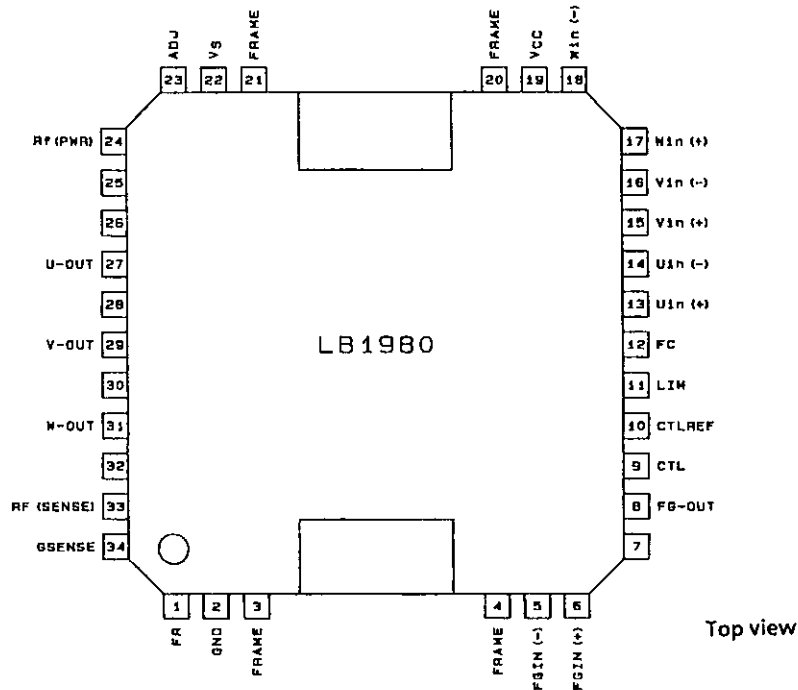
1. The torque ripple correction ratio is determined from the R_f voltage waveform as follows.



$$= \frac{2 \cdot (V_p - V_b)}{V_p + V_b} \cdot 100 (\%)$$

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Pin Assignment



Note: For ground potential stabilization, the FRAME pins must be connected to ground.

Truth Table and Control Functions

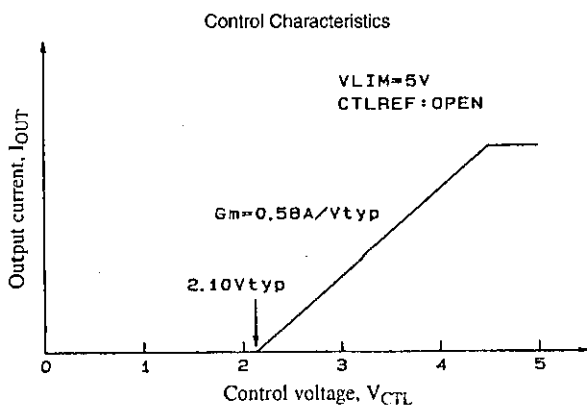
	Source → Sink	Hall input			FR
		U	V	W	
1	V → W	H	H	L	H
	W → V	H	H	L	L
2	U → W	H	L	L	H
	W → U	H	L	L	L
3	U → V	H	L	H	H
	V → U	H	L	H	L
4	W → V	L	L	H	H
	V → W	L	L	H	L
5	W → U	L	H	H	H
	U → W	L	H	H	L
6	V → U	L	H	L	H
	U → V	L	H	L	L

Note: An H in the FR column indicates a voltage of 2.75 V or higher, and an L indicates a voltage of 2.25 V or lower. (When $V_{CC} = 5$ V.)

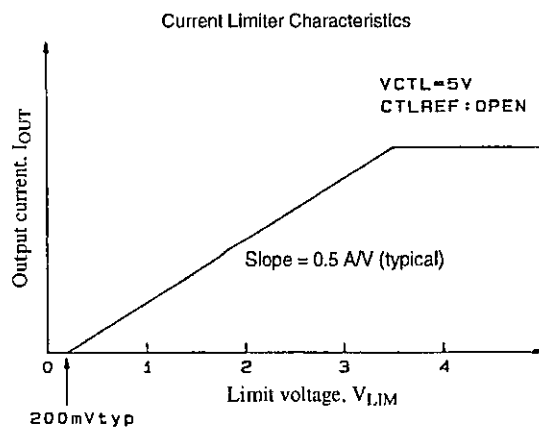
Note: For the Hall inputs, H indicates that the + input is 0.01 V or more higher than the - input, and L indicates that the + input is 0.01 V or more lower than the - input, for all phases.

Note: Since this drive technique is a 180° conducting technique, the phases other than the sink and source phases are never off.

[Control Function and Current Limiter Function]



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Pin Functions

Pin No.	Pin name	Pin functions	Equivalent circuit
1	FR	Forward/reverse selection pin. Forward or reverse is selected by the voltage applied to this pin. ($V_{th} = 2.5\text{ V}$ (typical) at $V_{CC} = 5\text{ V}$)	
23	ADJ	This pin allows the torque ripple correction ratio to be adjusted externally. Applications that adjust the correction ratio should apply a voltage to the ADJ pin with a low-impedance circuit. The correction ratio falls as the applied voltage increases, and increases as the applied voltage decreases. The correction ratio can be varied over a range from about 0 to twice the ratio when this pin is left open. (This voltage is set internally to about $V_{CC}/2$, and the input impedance is about $5\text{ k}\Omega$.)	
2	GND	Ground for circuits other than the output transistors The output transistor minimum potential is that of the resistor R_f .	
5	FGin-	When the FG amplifier is used as an inverting input amplifier, a feedback resistor must be inserted between FG-OUT and this pin.	
6	FGin+	This is the noninverting input when the FG amplifier is used as a differential input amplifier. There is no internally applied bias.	
8	FG-OUT	This is the FG amplifier output. It has an internal load resistance.	
12	FC	Frequency characteristics correction for the speed control loop	
9	CTL	Speed control connection. Speed control is implemented as a fixed current drive in which current feedback is applied from FR. $G_m = 0.58\text{ A/V}$ (typical) at $R_f = 0.5\text{ }\Omega$	
10	CTLREF	Control reference. Although this pin is set to about $0.43 * V_{CC}$ internally, it can be changed by applying a voltage with a low-impedance circuit. (It has an input impedance of about $4.3\text{ k}\Omega$ (typical).)	
11	LIM	Current limiter function control. The voltage applied to this pin changes the output current linearly. Slope = 0.5 A/V (typical) at $R_f = 0.5\text{ }\Omega$.	
13	Uin+	U phase Hall element input. IN^+ must be higher than IN^- for a logical high input level. V phase Hall element input. IN^+ must be higher than IN^- for a logical high input level. W phase Hall element input. IN^+ must be higher than IN^- for a logical high input level.	
14	Uin-		
15	Vin+		
16	Vin-		
17	Win+		
18	Win-		

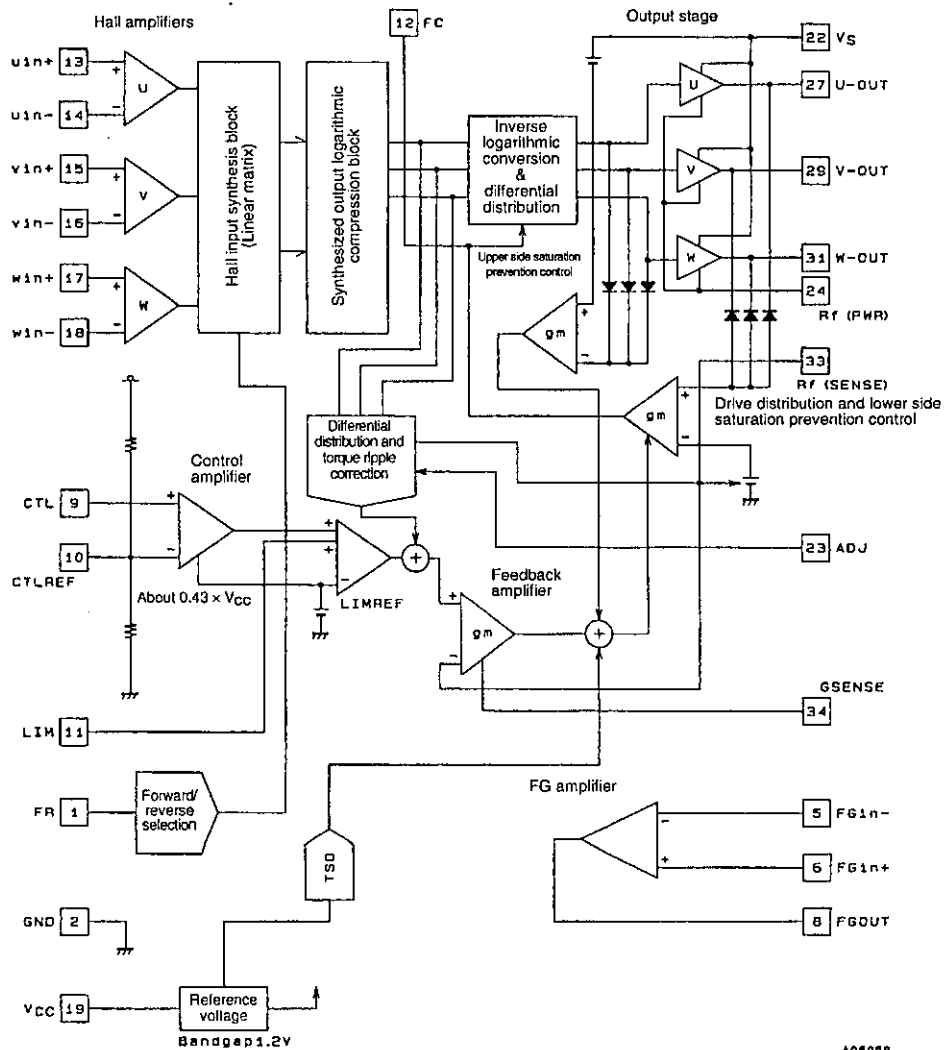
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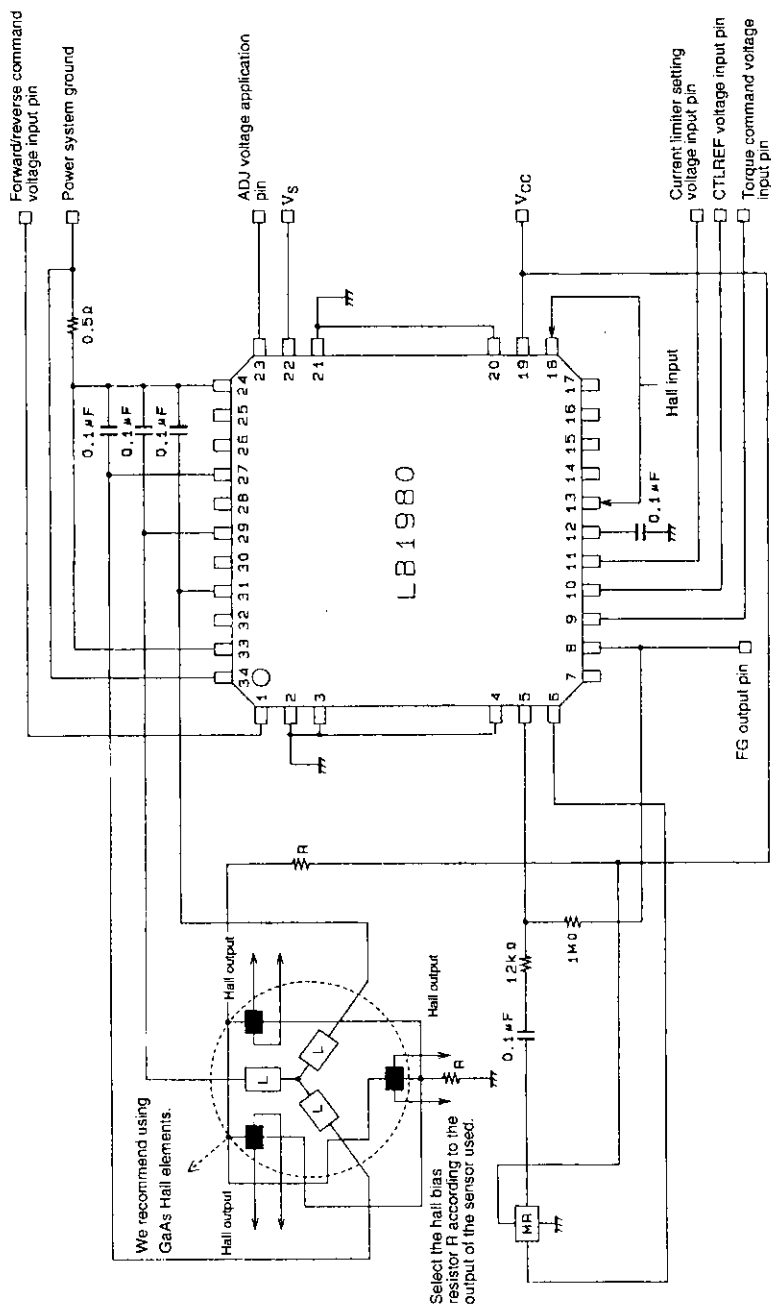
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Pin No.	Pin name	Pin functions	Equivalent circuit
19	V _{CC}	Power supply for all IC internal circuits except for the output block. This voltage must be stabilized so that ripple and noise do not enter the IC circuits.	
22	V _S	Output block power supply	
24	R _f (PWR)	These are the output current detection pins, and the control block current feedback is applied by connecting the resistor R _f between these pins and ground. Additionally, the lower side oversaturation protection circuit and the torque ripple correction circuit operate according to the voltages on these pins. In particular, since the oversaturation protection level is set by the voltages on these pins, if the value of R _f is lowered excessively, the effectiveness of the lower side oversaturation protection in the high-current region will be degraded. Note that the POWER and SENSE pins must be connected together.	
33	R _f (SENSE)		
27	U-OUT	U phase output. (A spark killer diode is built in.)	
29	V-OUT	V phase output. (A spark killer diode is built in.)	
31	W-OUT	W phase output. (A spark killer diode is built in.)	
34	GSENSE	Ground sense. By connecting this pin near the ground for the R _f resistor side of the motor ground wiring that includes R _f , the influence that the common ground impedance has on R _f can be removed. (This pin must not be left open.)	

Block Diagram



Sample Application Circuit



Note: The constants presented in this sample application circuit are examples, and the circuit characteristics for these values are not guaranteed.

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