



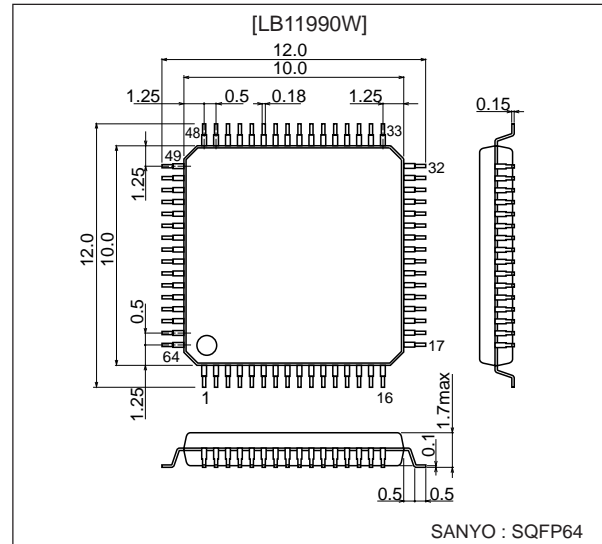
# LB11990W

## Three-Phase Brushless Motor Driver

### Package Dimensions

unit: mm

3190-SQFP64



### Specifications

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V <sub>CC1</sub> max		7	V
Maximum supply voltage 2	V <sub>CC2</sub> max		8.5	V
Maximum supply voltage 3	VS_C max	Capstan motor driver	7.0	V
Maximum supply voltage 4	VS_D max	Drum motor driver	7.0	V
Maximum supply voltage 5	VS_L max	Loading motor driver	7.0	V
Applied output voltage	Vo max		8.0	V
Applied input voltage	VI1 max	Control circuits	-0.3 to V <sub>CC1</sub> + 0.3	V
	VI2 max	U, V, W, COM	8.0	V
Capstan motor output current	IOC max		1.0	A
Drum motor output current	IOD max		1.0	A
Loading motor output current	IOL max		0.6	A
Allowable power dissipation	Pd max	IC only	0.6	W
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

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## Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage 1	V <sub>CC1</sub>	V <sub>CC1</sub> ≤ V <sub>CC2</sub>	2.7 to 6.0	V
Power supply voltage 2	V <sub>CC2</sub>		3.5 to 8.5	V
Power supply voltage 3	V <sub>S_C</sub>	V <sub>S_C</sub> ≤ V <sub>CC2</sub>	to 7.0	V
Power supply voltage 4	V <sub>S_D</sub>	V <sub>S_D</sub> ≤ V <sub>CC2</sub>	to 7.0	V
Power supply voltage 5	V <sub>S_L</sub>	V <sub>S_L</sub> ≤ V <sub>CC2</sub>	2.2 to 7.0	V
Hall input amplitude	VHALL	Capstan motor	±20 to ±80	mVp-p

## Electrical Characteristics/Capstan Motor Driver Block at Ta = 25°C, V<sub>CC1</sub> = 3V, V<sub>CC2</sub> = 4.75V, V<sub>S</sub> = 1.5V

	Parameter	Symbol	Conditions	Ratings			Unit
				min	typ	max	
Power supply current	Vcc1 power supply current	I <sub>cc1</sub>	I <sub>out</sub> = 100 mA V <sub>STBY_C</sub> = 3V		4	8	mA
	Vcc2 power supply current	I <sub>cc2</sub>	I <sub>out</sub> = 100 mA V <sub>STBY_C</sub> = 3V		6	12	mA
	Vcc1 idle current	I <sub>cc1Q</sub>	V <sub>STBY_C</sub> = 0V		2.1	4	mA
	Vcc2 idle current	I <sub>cc2Q</sub>	V <sub>STBY_C</sub> = 0V			100	μA
	Vs idle current	I <sub>sQ</sub>	V <sub>STBY_C</sub> = 0V		75	100	μA
VX1	Upper side residual voltage	VXH1	I <sub>out</sub> = 0.2A	0.15	0.22	0.29	V
	Lower side residual voltage	VXL1	I <sub>out</sub> = 0.2A	0.15	0.20	0.25	V
VX2	Upper side residual voltage	VXH2	I <sub>out</sub> = 0.5A		0.25	0.40	V
	Lower side residual voltage	VXL2	I <sub>out</sub> = 0.5A		0.25	0.40	V
	Output saturation voltage	V <sub>osat</sub>	I <sub>out</sub> = 0.8A, Sink + Source			1.40	V
	Overlap amount	O.L	RL = 39Ω × 3, R <sub>angle</sub> = 20 kΩ Note 2	73	80	87	%
Hall amplifier	Input offset voltage	V <sub>HOFF</sub>	Note 1 Design target value	-5		+5	mV
	Common mode input range	V <sub>HCM</sub>	R <sub>angle</sub> = 20 kΩ	0.95		2.1	V
	Input/output voltage gain	V <sub>GVH</sub>	R <sub>angle</sub> = 20 kΩ	24.5	27.5	30.5	dB
Standby pin	High level voltage	V <sub>STH</sub>		2.5		V <sub>CC1</sub>	V
	Low level voltage	V <sub>STL</sub>		-0.2		+0.7	V
	Input current	I <sub>STIN</sub>	V <sub>STBY_C</sub> = 3V			50	μA
	Leakage current	I <sub>STLK</sub>	V <sub>STBY_C</sub> = 0V			-30	μA
FRC pin	High level voltage	V <sub>FRC</sub> H		2.5		V <sub>CC1</sub>	V
	Low level voltage	V <sub>FRC</sub> L		-0.2		+0.4	V
	Input current	I <sub>FRC</sub> IN	V <sub>FRC_C</sub> = 3V		20	30	μA
	Leakage current	I <sub>FRC</sub> CLK	V <sub>FRC_C</sub> = 0V			-30	μA
VH	Hall power supply voltage	VHALL	I <sub>H</sub> = 5 mA, V <sub>H</sub> (+) - V <sub>H</sub> (-)	0.75	0.85	0.95	V
	(-) pin voltage	VH(-)	I <sub>H</sub> = 5 mA	0.81	0.88	0.95	V
FG comparator	Input offset voltage	V <sub>FGOFF</sub>		-3		+3	mV
	Input bias current	I <sub>bFG</sub>	V <sub>FGIN+</sub> = V <sub>FGIN-</sub> = 1.5V			500	nA
	Input bias current offset	ΔI <sub>bFG</sub>	V <sub>FGIN+</sub> = V <sub>FGIN-</sub> = 1.5V	-100		+100	nA
	Common mode input range	V <sub>FGCM</sub>		1.2		2.5	V
	High level output voltage	V <sub>FGOH</sub>	With internal pull-up	2.8			V
	Low level output voltage	V <sub>FGOL</sub>	With internal pull-up			0.2	V
	Voltage gain	V <sub>GF</sub> G	Note 1 Design target value		100		dB
	Output current (Sink)	I <sub>FGO</sub> s	At output pin "L"			5	mA

Note 1: Design target value, not measured

Note 2: The overlap amount specification is taken as the measurement specification.

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### Cylinder Motor Driver Block at $T_a = 25^\circ\text{C}$ , $V_{CC1} = 3\text{V}$ , $V_{CC2} = 4.75\text{V}$ , $V_S = 3\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply current 4	ICC2	$IO = 76\text{ mA}$ $VSTBY\_D = 3\text{V}$ $VSTBY\_C = 0\text{V}$		0.75	2.5	mA
Output idle current 4	ICC2Q	$VSTBY\_D = VSTBY\_C = 0\text{V}$			100	$\mu\text{A}$
Output idle current 5	IS(D)Q	$VSTBY\_D = VSTBY\_C = 0\text{V}$		100	300	$\mu\text{A}$
Output saturation voltage, upper side 1	VOU1	$IO = 0.1\text{A}$ $RF = 0.25\Omega$		0.3	0.5	V
Output saturation voltage, lower side 1	VOD1	$IO = 0.1\text{A}$ $RF = 0.25\Omega$		0.3	0.5	V
Output saturation voltage, upper side 2	VOU2	$IO = 0.4\text{A}$ , $VS = 3\text{V}$ $RF = 0.25\Omega$		0.5	0.8	V
Output saturation voltage, lower side 2	VOD2	$IO = 0.4\text{A}$ , $VS = 3\text{V}$ $RF = 0.25\Omega$		0.5	0.8	V
COM pin common mode input voltage range	VIC		0.3		$V_{CC2}-0.9$	V
Standby pin High level voltage	VSTBYH		2		$V_{CC1}$	V
Standby pin Low level voltage	VSTBYL		-0.2		+0.7	V
Standby pin input current	ISTBYH	$VSTBY\_D = 3\text{V}$			50	$\mu\text{A}$
Standby pin leakage current	ISTBYL	$VSTBY\_D = 0\text{V}$	-10			$\mu\text{A}$
FRC pin High level voltage	VFRCH		2		$V_{CC1}$	V
FRC pin Low level voltage	VFRCL		-0.2		+0.7	V
FRC pin input current	IFRCI	$VFRC\_D = 3\text{V}$			50	$\mu\text{A}$
FRC pin leakage current	IFRCL	$VFRC\_D = 0\text{V}$	-10			$\mu\text{A}$
Slope pin source current ratio	RSOURCE	$ICSLP1SOURCE/ICSLP2SOURCE$	-15		+15	%
Slope pin sink current ratio	RSINK	$ICSLP1SINK/ICSLP2SINK$	-15		+15	%
CSLP1 source/sink current ratio	RCSLP1	$ICSLP1SOURCE/ICSLP1SINK$	-35		+15	%
CSLP2 source/sink current ratio	RCSLP2	$ICSLP2SOURCE/ICSLP2SINK$	-35		+15	%
Startup frequency	Freq	$Cosc = 0.1\ \mu\text{F}$ , OSC frequency (Target)		11.5		Hz
Phase delay-width	Dwidth	(Target)		30		deg
SELCSLP pin High level voltage	VSELH		2		$V_{CC1}$	V
SELCSLP pin Low level voltage	VSELL		-0.2		+0.7	V
SELCSLP pin input current	ISELH	$VSELCSLP = 3\text{V}$			50	$\mu\text{A}$
SELCSLP pin leakage current	ISELL	$VSELCSLP = 0\text{V}$	-10			$\mu\text{A}$

Note) Items shown to be "Target" are not measured.

### FG/PG Amplifier Block at $T_a = 25^\circ\text{C}$ , $V_{CC1} = 3\text{V}$ , $V_{CC2} = 4.75\text{V}$ , $V_S = 3\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FG amplifier]						
Input offset voltage	VIO	(Target)		$\pm 1$	$\pm 5$	mA
Input bias current	IBIN-	(Target)			250	nA
Common mode input voltage range	VICOM	(Target)	1		2	V
Open loop gain	GVFG	$f = 1\text{ kHz}$ (Target)		55		dB
Output ON voltage	VOL	At $IO = 10\ \mu\text{A}$			0.4	V
Output OFF voltage	VOH	At $IO = 10\ \mu\text{A}$	$V_{CC1}-0.5$			V
Schmitt amplifier hysteresis width	VSHIS	(Target)		50		mV
Reference voltage	VREF		1.15	1.30	1.45	V
[PG amplifier]						
Input offset voltage	VIO	(Target)		$\pm 1$	$\pm 5$	mV
Input bias current	IBIN-	(Target)			250	nA
Common mode input voltage range	VICOM	(Target)	1		2	V
Open loop gain	GVPG	$f = 1\text{ kHz}$ (Target)		55		dB
Output ON voltage	VOL	At $IO = 10\ \mu\text{A}$			0.4	V
Output OFF voltage	VOH	At $IO = 10\ \mu\text{A}$	$V_{CC1}-0.5$			V
Schmitt amplifier hysteresis width	VSHIS	(Target)		50		mV

Note) Items shown to be "Target" are not measured.

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## Loading Motor Driver Block at Ta = 25°C, V<sub>CC1</sub> = 3V, V<sub>CC2</sub> = 4.75V, V<sub>S</sub> = 3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VCC1 power supply current 1	ICC11	VSTBY_C = VSTBY_D = 0V (standby)		2.1	4	mA
VCC1 power supply current 2	ICC12	VSTBY_C = VSTBY_D = 0V (forward/reverse)		14	19	mA
VCC1 power supply current 3	ICC13	VSTBY_C = VSTBY_D = 0V (at braking)		10	14	mA
VCC2 power supply current 1	ICC21	VSTBY_C, D = 0V (standby (V <sub>CC1</sub> = OPEN))			100	μA
VCC2 power supply current 2	ICC22	VSTBY_C, D = 0V (standby (V <sub>CC1</sub> = 3.0V))			100	μA
VCC2 power supply current 3	ICC23	VSTBY_C, D = 0V (forward/reverse)		15.0	25	mA
VS L power supply current	I VS L	VSTBY_C, D = 0V (standby)			20	μA
[Logic input (DEC1 pin, DEC2 pin)]						
High level input voltage	VINH	V <sub>CC1</sub> = 2.7 to 4.0V	2.0		V <sub>CC1</sub>	V
High level flowing current	IINH	VIN = 3.0V		41	65	μA
Low level input voltage	VINL	V <sub>CC1</sub> = 2.7 to 4.0V	-0.2		0.6	V
Low level flowing current	IINL	VIN = 0.6V		5	10	μA
[Loading motor driver]						
Output saturation voltage 1	VOH	IO = 200 mA (upper/lower composition)		0.2	0.3	V
Output saturation voltage 2	VSHIS	IO = 400 mA (upper/lower composition)		0.4	0.6	V
[Reel FG amplifier]						
Input offset voltage	VIO			±1	±5	mV
Input bias current	IB				1	μA
Common mode input voltage range	VICM		1		2	V
Open loop gain	GV1			55		dB
[Thermal shutdown circuit]						
TSD operating temperature	T-TSD	(Target)		180		°C
TSD temperature hysteresis width	ΔTSD	(Target)		15		°C

Note) Items shown to be "Target" are not measured.

## Truth Table

### Capstan Motor Truth Table

	Source → Sink	Hall input			FRC
		U	V	W	
1	V → W	H	H	L	H
	W → V				L
2	U → W	H	L	L	H
	W → U				L
3	U → V	H	L	H	H
	V → U				L
4	W → V	L	L	H	H
	V → W				L
5	W → U	L	H	H	H
	U → W				L
6	V → U	L	H	L	H
	U → V				L

Note: "H" for FR means a voltage of 2.50V or above. "L" for FR means a voltage of 0.4V or below.  
(V<sub>cc1</sub> = 3V)

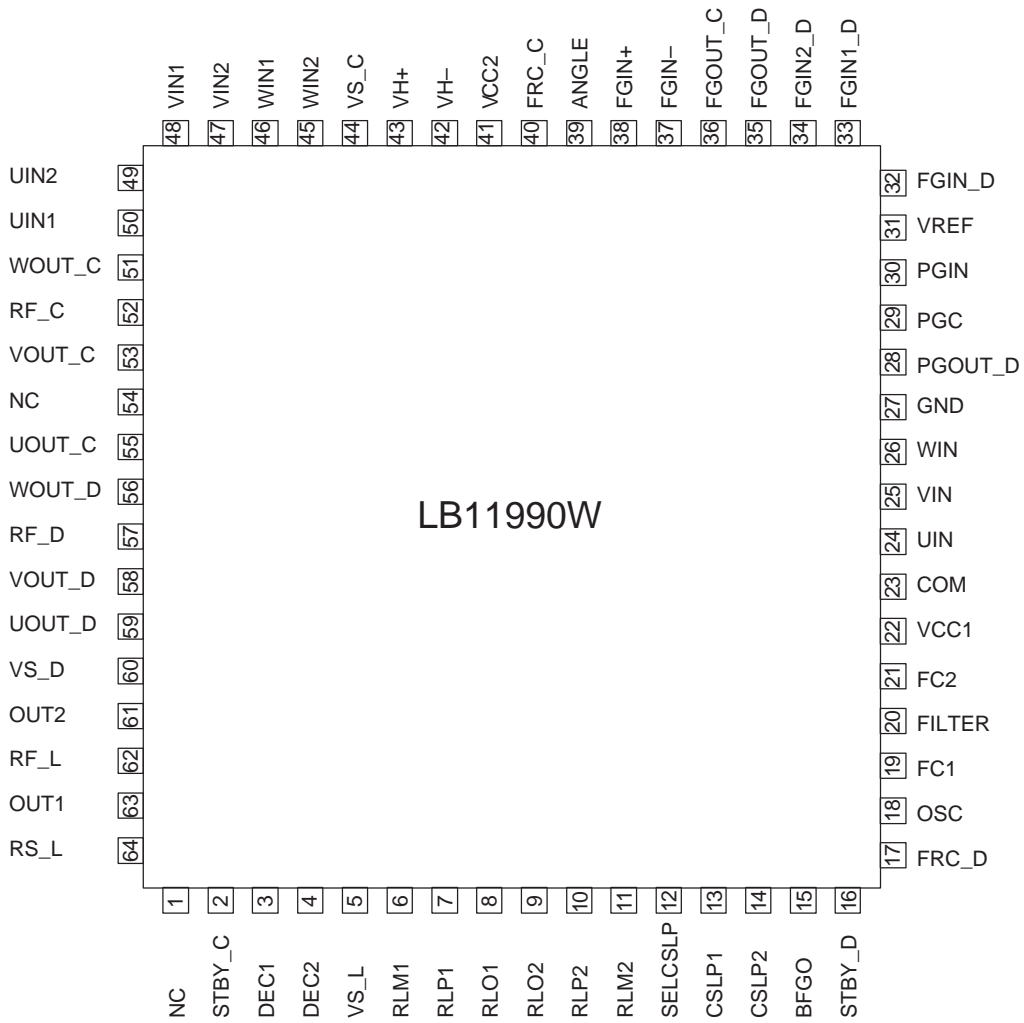
Note: At the Hall input, "H" means that the potential of the (+) terminal for each phase input is at least 0.02V higher than the (-) terminal.  
"L" means that the potential of the (+) terminal for each phase input is at least 0.02V lower than the (-) terminal.

### Loading Motor Truth Table

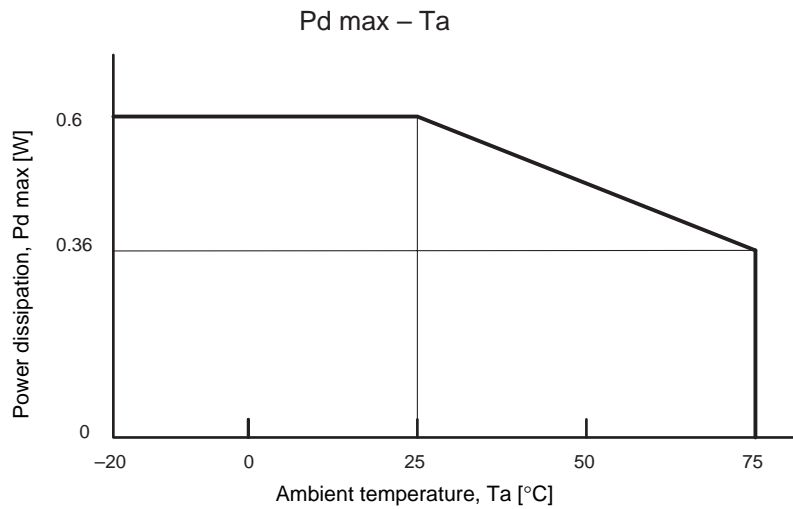
Input		Output		Mode
DEC1	DEC2	OUT1	OUT2	
L	L	Off	Off	Standby
H	L	H	L	Forward
L	H	L	H	Reverse
H	H	L	L	Brake

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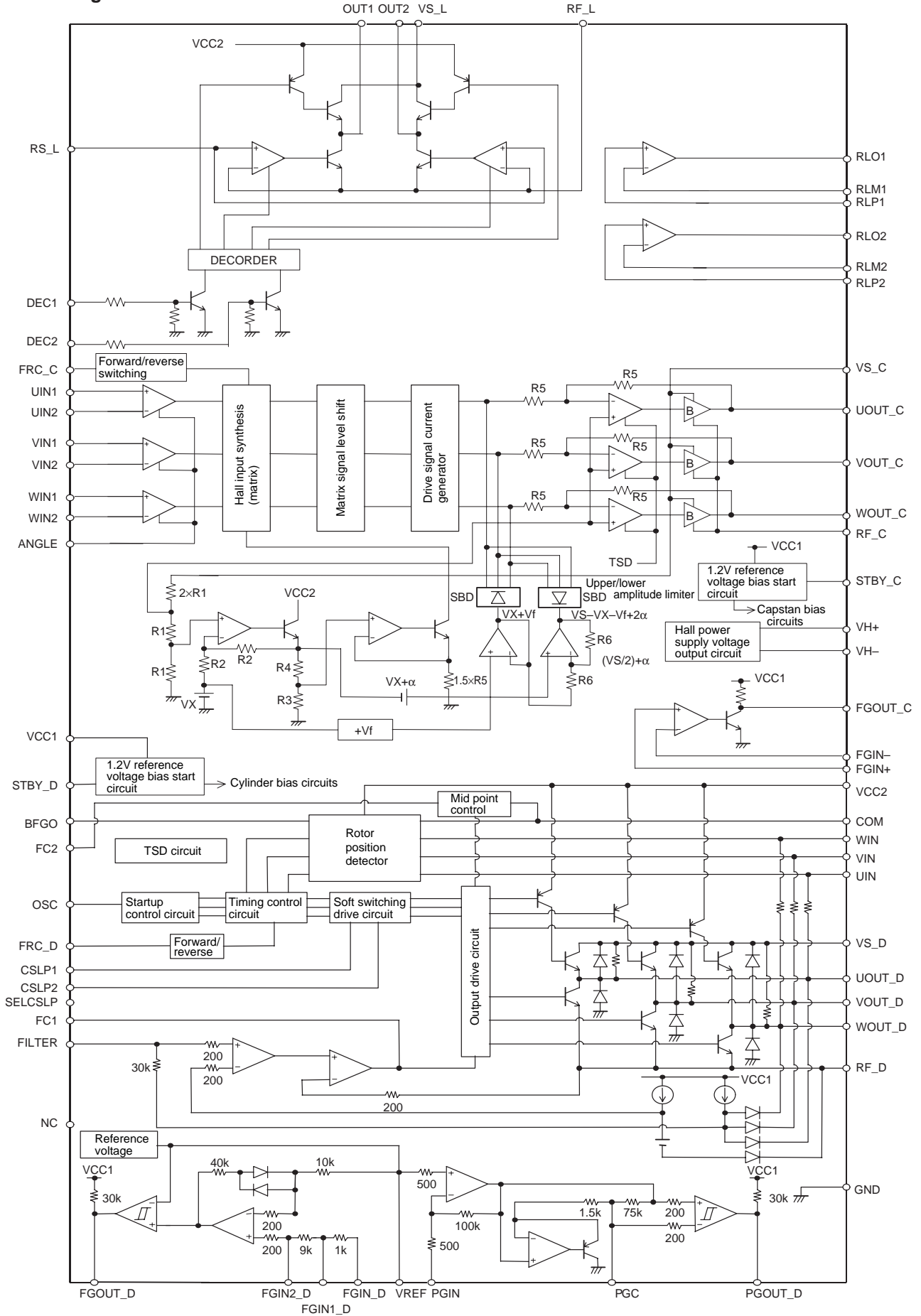
## Pin Assignment



Top view



Block Diagram



Unit (resistance: Ω)

Pin Description

Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
50 49 48 47 46 45	Uin1 Uin2 Vin1 Vin2 Win1 Win2	0 to V <sub>CC1</sub>		Capstan motor driver U, V, W phase Hall element input/output pins. Logic High means IN1 > IN2.
39	ANGLE			
44	VS_C	0 to V <sub>CC2</sub>		Capstan motor output amplitude control power supply pins. Voltage must be lower than V <sub>CC2</sub> .
55 53 51 52	U-OUT_C V-OUT_C W-OUT_C RF_C			Capstan motor driver U, V, W phase output pins.
43	VH+			Hall element bias voltage supply pins. A voltage of 0.85V (typ.) is generated between VH+ and VH- (at I <sub>H</sub> = 5 mA).
42	VH-			

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
37	FGIN-	0 to V <sub>CC1</sub>		FG comparator inverted input pin. No internal bias is applied.
38	FGIN+			FG comparator non-inverted input pin. No internal bias is applied.
36	FGOUT_C			FG comparator output pin. Internal load impedance is 20 kΩ.
40	FRC_C	0 to V <sub>CC1</sub>		Capstan motor forward/reverse select pin. The voltage at this pin (with hysteresis) selects forward or reverse rotation.
2	STBY_C			This pin selects bias supply to capstan circuits other than FG comparator. Setting the pin to Low cuts off the bias supply. Capstan motor standby pin.
35	FGOUT_D			FG amplifier output pin.
18	OSC			Pin for connecting triangular wave oscillator capacitor. Serves for forced startup waveform generation.

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
19	FC1			<p>Frequency characteristics pin. Connecting a capacitor between this pin and ground serves to prevent closed-loop oscillation in the current control circuitry.</p>
20	FILTER			<p>Connecting a capacitor between this pin and ground activates the coil output saturation prevention function. In this condition, the VS pin is controlled for motor voltage control. By adjusting the external capacitor, torque ripple compensation can be varied.</p>
28	PGOUT D			<p>PG amplifier output pin.</p>
29	PGC			<p>PG amplifier peak hold capacitor connection pin.</p>

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
30	PGIN	max2.0V  min1.0V (At $V_{CC} = 3V$ )		PG amplifier input pin. Connect PG coil between this pin and VREF.
31	VREF			Internal 1.3V reference voltage. Used as reference voltage for FG and PG amplifiers.
32	FGIN_D	max2.0V  min1.0V (At $V_{CC1} = 3V$ )		FG amplifier input pin. Connect FG coil between this pin and VREF.
33	FGIN1_D			FG amplifier input signal noise filter capacitor connection.
34	FGIN2_D			FG amplifier input signal noise filter capacitor connection.
16	STBY_D	0 to $V_{CC1}$		When this pin is at 0.7V or lower or when it is open, only the FG/PG amplifier operates. In the motor drive state, the pin should be at 2V or higher. Drum motor standby pin.

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
17	FRC_D	0 to V <sub>CC1</sub>		Drum motor forward/reverse rotation select pin. Low: forward (-0.2V to 0.7V or open) High: reverse (2V to V <sub>CC1</sub> )
60	VS_D	0V to V <sub>CC2</sub>		Power supply pin for determining output amplitude by supplying drum motor voltage. Must be lower than V <sub>CC2</sub> voltage.
41	V <sub>CC2</sub>	3.5V to 8.5V		Power supply pin for supplying source side predriver voltage and coil waveform detect comparator voltage. Common for loading, capstan, and drum motors.
22	V <sub>CC1</sub>	2.7V to 6V		Power supply pin for circuits except motor voltage, source side predriver voltage, and coil waveform detect comparator voltage. Common for loading, capstan, and drum motors.
13	CSLP1			Pins for connecting triangular wave oscillator capacitor. This triangular wave coil output performs waveform soft switching.
14	CSLP2			
27	GND			Ground pin for all circuits except output.

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
26 24 25	WIN UIN VIN			Coil waveform detect comparator input pins.
23	COM			Motor coil midpoint input pin. Using this voltage as a reference, the coil voltage waveform is detected.
56 59 58	WOUT_D UOUT_D VOUT_D			U, V, W phase coil output pins.
57	RF_D			Drum motor driver output transistor ground. Constant current drive is performed by detecting the voltage at this pin.
21	FC2			Output midpoint control. Oscillation prevention capacitor connection pin.
12	SELCSLP	0 to V <sub>CC1</sub>		When High, this pin sets CSLP slant to 15 times the slant at Low. When V <sub>CC1</sub> = 3.0V 2.0V or higher: High 0.7V or lower: Low

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
15	BFGO			<p>Motor counter EMF voltage FG pulse pin.</p> <p>Outputs a pulse using W phase counter EMF voltage as FG.</p> <p>Connect to ground if not used.</p>
5	VS_L	2.2 to $V_{CC2}$		<p>Loading motor power supply pin.</p> <p>Stabilize against noise in the same way as for <math>V_{CC2}</math>.</p>
62	RF_L			<p>Output transistor P-GND</p> <p>Output current can be detected for motor current control by inserting a resistor between Rf pin and ground.</p>
63 61	OUT1 OUT2			<p>Loading motor driver output pins.</p> <p>Connect to loading motor.</p>
6 7 11 10	RLM1 RLP1 RLM2 RLP2	0 to $V_{CC1}$		<p>L-FG amplifier input pins.</p> <p>RLM1 and RLM2 are negative input.</p> <p>RLP1 and RLP2 are positive input.</p>

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
8 9	RLO1 RLO2			R-FG amplifier output pins.
3 4	DEC1 DEC2	0 to $V_{CC1}$		Loading motor input pins. When $V_{CC1} = 3.0V$ 2.0V or higher: High 0.6V or lower: Low
64	RS_L	0 to $V_{CC1}$ -1.5V		Current limiter setting pin. Set voltage between RF pin and ground, for limiting current.

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