



CD Player Analog Signal Processor (ASP)

Overview

The LA9251M is a servo signal-processing IC for CD players. In combination with a CD DSP such as the LC78626KE, it can implement a CD player with a minimal number of external components.

Functions

- I/V amplifier
- SLC
- FE
- · Focus servo amplifier
- Spindle servo amplifier (with gain switching function)
- Focus detection (DRF and FZD)
- · Defect detection
- · RF amplifier with AGC
- APC
- TE (with variable gain and auto balance function)
- · Tracking servo amplifier
- Sled servo amplifier (with turn-off function)
- Track detection (HFL, TES)
- Shock detection

Features

- Low-voltage operation: 2.4 V (minimum)
- Low current drain: 15 mA (at $V_{CC} = 3.0 \text{ V}$, typical)

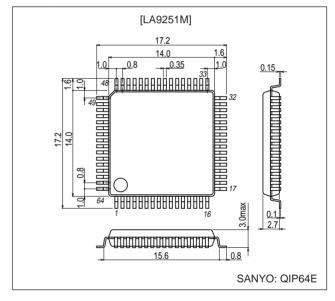
• Built-in EF balance adjustment

- Built-in RF level AGC function
- RF level follower function for the tracking servo gain (with turn-off function)

Package Dimensions

unit: mm

3159-QIP64E



Specifications

Maximum Ratings at $Ta = 25^{\circ}C$, with pin 46 tied to ground

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	Pin 56	7	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	200	mW
Operating temperature	Topr		-15 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

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Operating Conditions at $Ta = 25^{\circ}C$, with pin 46 tied to ground

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	Vcc		3	V
Allowable operating supply voltage range	V _{CC} op		2.4 to 5.5	V

Electrical Characteristics at $Ta = 25^{\circ}C$, with pin 46 tied to ground, pin 56 = 3 V

vth SLC th SP8 vth EFE th EST vth LAS R = FIN The tt The x1 FD0	OF 8: 8 cm mode BAL TA	min 8 1.2	14 1.5 0.8 0.8 2.3 2.3 0.8 35	max 21 1.8	V V V V V Hz
vth SLC th SP8 vth EFE th EST vth LAS R = FIN The tt The x1 FD0	OF 8: 8 cm mode BAL TA SER = 390 k Ω , C = 0.1 μ F	1.2	1.5 0.8 0.8 2.3 2.3 0.8 35	1.8	V V V V V
th SLC th SP8 th SP8 th EFF th EST th LAS R = FIN FIN th The	OF 8: 8 cm mode BAL TA SER = 390 k Ω , C = 0.1 μ F	25	0.8 0.8 2.3 2.3 0.8 35	45	V V V
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th SPE th SPE th EFE th EST th LAS R = in FIN FIN tt The tx1 FDO	8: 8 cm mode BAL TA SER = 390 k Ω , C = 0.1 μ F M1, FIN2: 1 M Ω -input, PH1 = 2 V, f = 200 kHz, RF		0.8 2.3 2.3 0.8 35		V V V
vth EFE tth EST vth LAS R = iin FIN FIN tth The x1 FDO	BAL TA SER = 390 kΩ, C = 0.1 μF		2.3 2.3 0.8 35		V
rth EST vth LAS R = in FIN FIN tt The xx1 FDC	TA SER = 390 kΩ, C = 0.1 μF		2.3 0.8 35		V
vth LAS R =	SER = 390 kΩ, C = 0.1 μF 11, FIN2: 1 MΩ-input, PH1 = 2 V, f = 200 kHz, RF		0.8 35		V
R =	= 390 kΩ, C = 0.1 μF J1, FIN2: 1 MΩ-input, PH1 = 2 V, f = 200 kHz, RF		1.00		-
FIN FIN The x1 FD0	N1, FIN2: 1 MΩ-input, PH1 = 2 V, f = 200 kHz, RF		1.00		Hz
FIN The x1 FD0		0.75		,	
FIN The x1 FD0		0.75			
FIN The			4.5	1.25	V
t The	J1, FIN2: 1 MΩ-input, FDO		-15		dB
t The	V1, FIN2: 1 MΩ-input, FDO				
x1 FD0		3.5	5.0	6.5	dB
	e difference from the reference voltage, servo on.	-340	0	+340	mV
1 [[]	O, FSS = GND		0.8		V
n1 FD0	O, FSS = GND		-0.8		V
x2 FD0	O, FSS = V _{CC}		0.8		V
n2 FD0	O, FSS = V _{CC}		0		V
ax f = f	10 kHz, E: 1 MΩ-input, PH1 = 0.5 V, TGRF = open	-3.6	-3.0	-2.4	dB
nin f = 1	10 kHz, E: 1 MΩ-input, PH1 = 2 V, TGRF = open	-11.0	-9.0	-7.0	dB
	1 MΩ-input		70		kHz
TH	→ TO gain, THLD mode	10.0	12.0	14.0	dB
	rvo on, TGL = high, TO	-260	0	+260	mV
		-35	0	+35	mV
_		-35	0	+35	mV
_		-25	0	+25	mV
			+35		dB
_					dB
		0.8		1.8	V
_	e difference from RESM				V
					V
					V
	,			00	V
		2.0		0.5	V
	the difference from VR	0		0.0	V
	•				V
	<u>, </u>	-0.25		-0.05	V
_	, and amoronou nom vic	_		3.00	V
		2.0		0.5	V
	SI the difference from VR	_0.15			V
	· · · · · · · · · · · · · · · · · · ·				V
	oi, alo difference from viv			0.10	V
		2.5		0.5	V
L	P = 3 V, at TO, the difference from TJP = 1.5 V	0.05	U	0.5	V
	Oost TG	TGL = low, the difference from the TGL offset, TO THLD mode, the difference from the TGL offset, TO TOST THLD mode, the difference from the TGL offset, TO TOST TOFF = High L-H	TGL = low, the difference from the TGL offset, TO	lost TGL = low, the difference from the TGL offset, TO -35 0 lost THLD mode, the difference from the TGL offset, TO -35 0 lost TOFF = High -25 0 H AGainE/F input, TB = 3 V, TBC = open +35 L AGainE/F input, TB = 0 V, TBC = open -35 vth 0.8 1.5 lo The difference from RFSM -0.90 -0.65 vth At RFSM, the difference from VR -0.50 -0.25 F-H 2.5 2.9 F-L 0 0.2 D1 FE, the difference from VR 0 0.2 D2 FE, the difference from VR 0 0.2 D2 FE, the difference from VR -0.25 -0.10 -H 2.5 2.9 -L 0 -0.15 -0.10 -HL TESI, the difference from VR 0.05 0.10 -HL TESI, the difference from VR 0.05 0.10 -H 2.5 2.9 <	lost TGL = low, the difference from the TGL offset, TO -35 0 +35 lost THLD mode, the difference from the TGL offset, TO -35 0 +35 lost TOFF = High -25 0 +25 H AGainE/F input, TB = 3 V, TBC = open +35 L AGainE/F input, TB = 0 V, TBC = open -35 vth 0.8 1.5 1.8 lo The difference from RFSM 0.8 1.5 1.8 lo The difference from RFSM 0.40 0.65 0.90 vth At RFSM, the difference from VR -0.50 -0.25 -0.10 F-H 2.5 2.9 F-L 0 0.5 D1 FE, the difference from VR 0 0.2 F2, the difference from VR -0.25 -0.10 -0.05 -H 2.5 2.9 -LL 0 0.5 -LH TESI, the difference from VR -0.15 -0.10 -0.05 -HL TESI, the differen

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Parameter	Symbol	Conditions	min	typ	max	Unit	
[Spindle Amplifier]							
Offset 12	SPD12ost	At SPD, the difference from VR, SP8 = 0 V: 12 cm mode	-40	0	+40	mV	
Offset 8	SPD8ost	At SPD, the difference from VR, SP8 = 3 V: 8 cm mode	-40	0	+40	mV	
Offset off	SPDof	At SPD, the difference from VR, SP8 = 3 V: 8 cm mode	-40	0	+40	mV	
Output voltage H12	SPD-H12	The difference from offset 12, SP8 = 0 V, 12 cm mode, CLV = 3 V	0.35	0.50	0.65	٧	
Output voltage H8	SPD-H8	The difference from offset 8, SP8 = 3 V, 8 cm mode, CLV = 3 V	0.10	0.20	0.30	٧	
[Sled Amplifier]							
Offset SLD	SLDost	SLEQ = VR, the difference from VR	-80	0	+80	mV	
Offset off	SLDof	SLOF = High	-40	0	+40	mV	
SLC no-signal voltage	SLCo	SLC	1.0	1.5	2.0	V	
Shock no-signal voltage	SCIo	SCI, the difference from VR	-40	0	+40	mV	
Shock detection voltage (high)	SClvthH	SCI, the difference from VR	90	140	190	mV	
Shock detection voltage (low)	SCIvthL	SCI, the difference from VR	-190	-140	-90	mV	
DEF detection voltage	DEFvth	The difference between the LF2 voltage when DEF is detected with RF = 1.9 V and the LF2 voltage when RF = 1.9 V.	0.20	0.35	0.50	V	
DEF output voltage (high)	DEF-H		2.5	2.9		V	
DEF output voltage (low)	DEF-L			0	0.5	V	
APC reference voltage	LDS	The LDS voltage such that LDD = 1.5 V	120	170	220	mV	
APC off voltage	LDDof	LDD	2.7	2.9		V	

Pin Functions

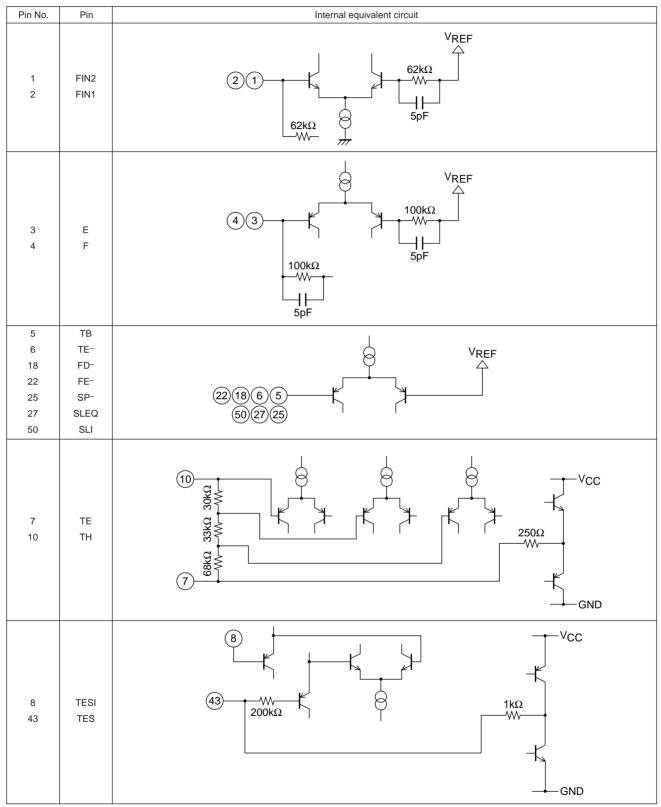
Pin No.	Pin	Function
1	FIN2	Pickup photodiode (focus, RF) connection
2	FIN1	Pickup photodiode (focus, RF) connection
3	E	Pickup photodiode (tracking) connection
4	F	Pickup photodiode (tracking) connection
5	ТВ	TE signal DC component input. Pickup photodiode (tracking) connection
6	TE-	TE signal gain setting resistor connection. A resistor is connected between this pin and TE.
7	TE	TE signal output
8	TESI	TES comparator input. Takes the bandpass filtered TE signal as its input.
9	SCI	Shock detection input
10	TH	Tracking gain time constant setting
11	TA	TA amplifier output
12	TD-	In conjunction with the TD and VR pins, used to form the tracking phase compensation circuit constant
13	TD	Tracking phase compensation setting
14	JP	Track jump signal amplitude setting
15	ТО	Tracking control signal output
16	(NC)	No connection
17	FD	Focusing control signal output
18	FD-	In conjunction with the FD and FA pins, used to form the focusing phase compensation circuit constant
19	FA	In conjunction with the FD- and FA- pins, used to form the focusing phase compensation circuit constant
20	FA-	In conjunction with the FA and FE pins, used to form the focusing phase compensation circuit constant
21	FE	FE signal output
22	FE-	FE signal gain setting resistor connection. A resistor is connected between this pin and FE.
23	SP	CLV pin input signal inverted output
24	SPG	Gain setting resistor connection (12 cm spindle mode)

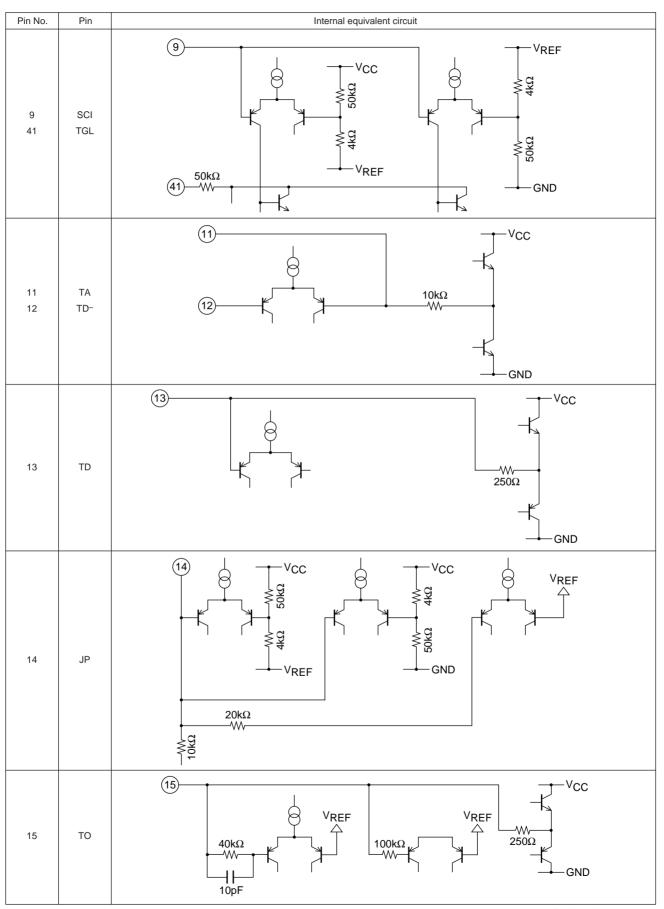
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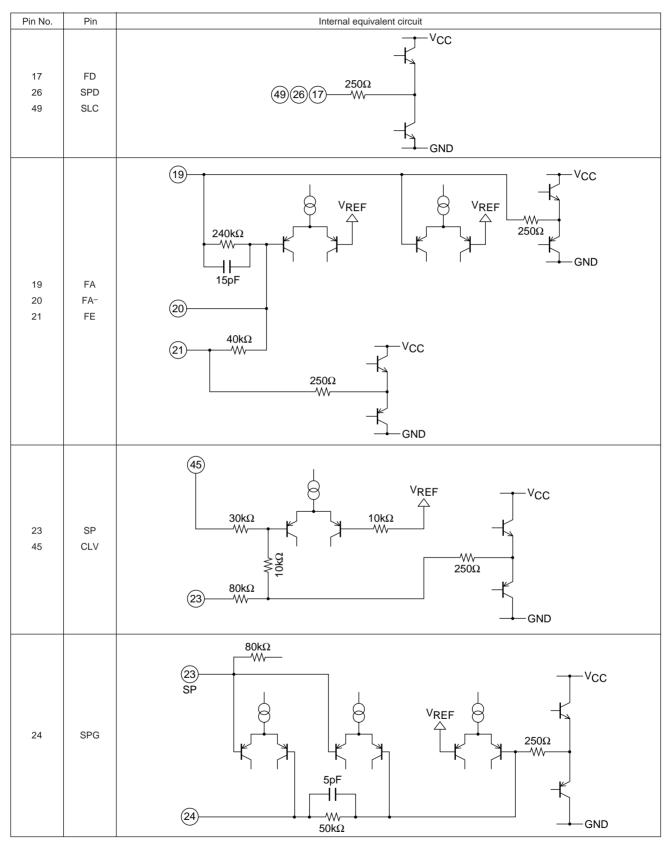
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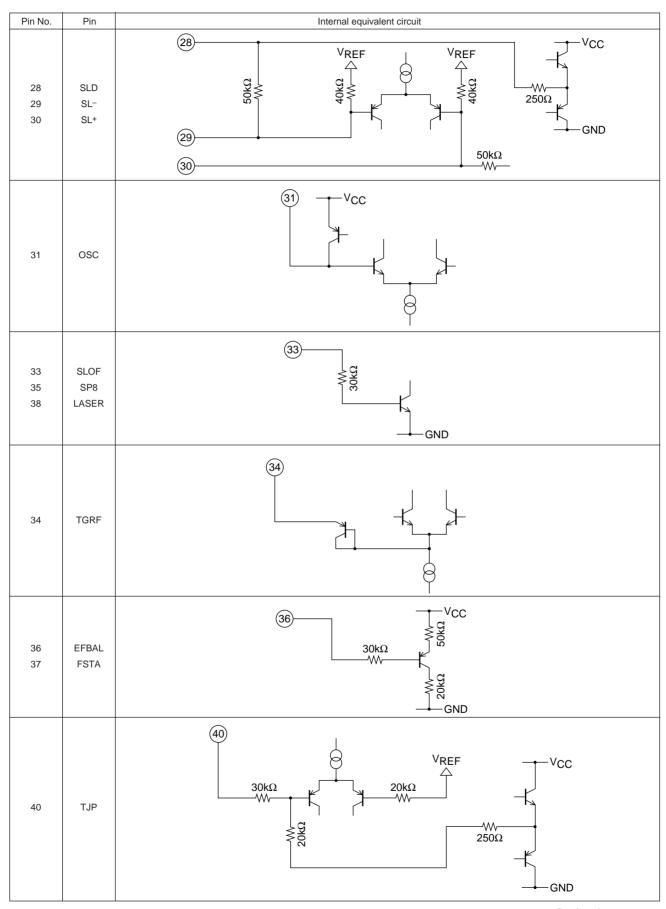
Pin No. Pin Function Function			
26 SPD Spindle control signal output 27 SLEG Sled phase compensation constant connection 28 SLD Sled control signal output 29 SL- Sled feed signal input from the microcontroller 30 SL* Sled feed signal input from the microcontroller 31 OSC Oscillator frequency setting 32 (NC) No connection 33 SLOF Sled serv off control input 34 TGRF Tracking serve gain RF level follower function setting 35 SP8 Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL EfF balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking off control signal input from the DSP 42 ToFF Tracking off control signal input from the DSP 43 TES TS Signal output to the DSP 44 TFL Quiput for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF R R output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 Disc defect detection output 52 DRF R Revel detection output 54 TRC E/F balance variation range setting 55 FSS Focus search smoothing capacitor connection 56 YCC VCC 57 REFI Reference voltage bypass capacitor connection 66 PM1 RF signal bottom hold capacitor connection 66 DRD APC circuit input	Pin No.	Pin	Function
SLEQ Sled phase compensation constant connection	25	SP-	In conjunction with the SPD pin, spindle phase compensation constant connection
SLD Sled control signal output 29 SL- Sled feed signal input from the microcontroller 30 SL+ Sled feed signal input from the microcontroller 31 OSC Oscillator frequency setting 32 (NC) No connection 33 SLOF Sled serv of control input 34 TGRF Tracking servo gain RF level follower function setting 35 SP8 Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL E/F balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Tracking pain control signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES Signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor connection 54 VR Reference voltage output 55 FSS Focus search smoothing capacitor connection 66 PM1 RF signal peak hold capacitor connection 67 REFI Reference voltage output 68 LDS APC circuit input	26	SPD	Spindle control signal output
SL* Sled feed signal input from the microcontroller 30 SL* Sled feed signal input from the microcontroller 31 OSC Oscillator frequency setting 32 (NC) No connection 33 SLOF Sled servo off control input 34 TGRF Tacking servo gain RF level follower function setting 35 SP8 Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL E/F balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES Signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLL Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 53 FSC Focus search smoothing capacitor output 54 TSC FSS Focus search smoothing capacitor output 55 PSF FSS Focus search mode setting 56 VCC VCC 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage bypass capacitor connection 59 LP2 Disc defect detection output 60 PHH R F signal peak hold capacitor connection 61 BHH R F signal bottom hold capacitor connection 62 LDD APC circuit input	27	SLEQ	Sled phase compensation constant connection
30 SL* Sled feed signal input from the microcontroller 31 OSC Oscillator frequency setting 32 (NC) No connection 33 SLOF Sled servo off control input 34 TGRF Tracking servo gain RF level follower function setting 35 SP8 Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL E/F balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Tracking pain control signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES TES signal output to the DSP 44 HFL Output for the HFL signal input from the DSP 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF R Foutput 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF R Flevel detection output 53 FSC Focus search mode setting 54 Vcc Vcc 57 REFI Reference voltage bypass capacitor connection 58 Vcc Vcc 59 Reference voltage bypass capacitor connection 69 LP1 RF signal peak hold capacitor connection 60 PH1 R F signal peak hold capacitor connection 61 BH1 RF signal peak hold capacitor connection 61 BH1 RF signal beat mold capacitor connection 62 LDD APC circuit input	28	SLD	Sled control signal output
31 OSC Oscillator frequency setting 32 (NC) No connection 33 SLOF Sted servo off control input 33 SLOF Tracking servo gain RF level follower function setting 35 SP8 Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL E/F balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking gain control signal input from the DSP 43 TES TES signal output to the DSP 44 THE L Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF R Foutput 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search mode setting 54 TSC Focus search mode setting 55 FSC Focus search mode setting 56 Vcc Vcc 57 REFI Reference voltage bypass capacitor connection 58 LPS APC circuit input	29	SL-	Sled feed signal input from the microcontroller
32 (NC) No connection 33 SLOF Sled servo off control input 34 TGRF Tracking servo gain RF level follower function setting 35 SP8 Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL E/F balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Tracking gain control signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking gain control signal input from the DSP 43 TES Signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF R Foutput 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data silce level according to the DSP 50 SLI Input for control of the data silce level according to the DSP 51 DEF Disc defect detection output 52 DRF R Flevel detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 VCC VCC 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection intime constant setting 60 PH1 R F signal peak hold capacitor connection 61 BH1 R F signal peak hold capacitor connection 62 LDD APC circuit input	30	SL+	Sled feed signal input from the microcontroller
33 SLOF Sled servo off control input 34 TGRF Tracking servo gain RF level follower function setting 35 SPS Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL EF balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES Signal output to the DSP 44 TES signal output to the DSP 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF R level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 VCC VCC 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage bypass capacitor connection 60 PH1 R F signal peak hold capacitor connection 61 BH1 RF signal peak hold capacitor connection 62 LDD APC circuit output	31	osc	Oscillator frequency setting
34 TGRF Tracking servo gain RF level follower function setting 35 SP8 Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL E/F balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking again control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES Signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 VC VC 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage bypass capacitor connection 60 PH1 RF signal beat hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit input	32	(NC)	No connection
SP8 Spindle 8 cm/12 cm mode switching control from the DSP 36 EFBAL E/F balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking gain control signal input from the DSP 43 TES signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF R Foutput 48 RF— In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF R level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 V _{CC} V _{CC} 77 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection indicated in the connection 60 PH1 R F signal bottom hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit input	33	SLOF	Sled servo off control input
36 EFBAL E/F balance adjustment signal input from the DSP 37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES TES signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 VC VCC 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 69 LP2 Disc defect detection time constant setting 60 PH1 RF signal bottom hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit input	34	TGRF	Tracking servo gain RF level follower function setting
37 FSTA Focus search control signal input from the DSP 38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking gain control signal input from the DSP 43 TES Signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 Vcc 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PHI RF signal bottom hold capacitor connection 61 BHI RF signal bottom hold capacitor connection 62 LDD APC circuit input	35	SP8	Spindle 8 cm/12 cm mode switching control from the DSP
38 LASER Laser on/off control from the DSP 39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES TES signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND SND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 Vcc Vcc 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection ine constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output	36	EFBAL	E/F balance adjustment signal input from the DSP
39 (NC) No connection 40 TJP Track jump signal input from the DSP 41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES Signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 Vcc Vcc 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal bottom hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output	37	FSTA	Focus search control signal input from the DSP
TJP Track jump signal input from the DSP TGL Tracking gain control signal input from the DSP TGL Tracking gain control signal input from the DSP TGS ignal output to the DSP TGS signal output for the HFL signal that indicates whether the main beam is positioned over pits or mirror CLV CLV error signal input from the DSP TGND GND TGND	38	LASER	Laser on/off control from the DSP
41 TGL Tracking gain control signal input from the DSP 42 TOFF Tracking off control signal input from the DSP 43 TES TES signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal beak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output	39	(NC)	No connection
TOFF Tracking off control signal input from the DSP TES signal output to the DSP Uput for the HFL signal that indicates whether the main beam is positioned over pits or mirror LUV CLV error signal input from the DSP REPORT	40	TJP	Track jump signal input from the DSP
TES TES signal output to the DSP 44 HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Fosus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output	41	TGL	Tracking gain control signal input from the DSP
HFL Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror 45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 Vcc Vcc 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output	42	TOFF	Tracking off control signal input from the DSP
45 CLV CLV error signal input from the DSP 46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 Vcc Vcc 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output	43	TES	TES signal output to the DSP
46 GND GND 47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 Vcc Vcc 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output	44	HFL	Output for the HFL signal that indicates whether the main beam is positioned over pits or mirror
47 RF RF output 48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 Vcc Vcc 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit input	45	CLV	CLV error signal input from the DSP
48 RF- In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant 49 SLC Output for control of the data slice level according to the DSP 50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	46	GND	GND
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50 SLI Input for control of the data slice level according to the DSP 51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	48	RF-	In conjunction with the RF pin, sets the RF gain and sets the EFM 3T compensation constant
51 DEF Disc defect detection output 52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	49	SLC	Output for control of the data slice level according to the DSP
52 DRF RF level detection output 53 FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	50	SLI	Input for control of the data slice level according to the DSP
FSC Focus search smoothing capacitor output 54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	51	DEF	Disc defect detection output
54 TBC E/F balance variation range setting 55 FSS Focus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	52	DRF	RF level detection output
55 FSS Focus search mode setting 56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	53	FSC	Focus search smoothing capacitor output
56 V _{CC} V _{CC} 57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	54	TBC	E/F balance variation range setting
57 REFI Reference voltage bypass capacitor connection 58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	55	FSS	Focus search mode setting
58 VR Reference voltage output 59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	56	V_{CC}	Vcc
59 LF2 Disc defect detection time constant setting 60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	57	REFI	Reference voltage bypass capacitor connection
60 PH1 RF signal peak hold capacitor connection 61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	58	VR	Reference voltage output
61 BH1 RF signal bottom hold capacitor connection 62 LDD APC circuit output 63 LDS APC circuit input	59	LF2	Disc defect detection time constant setting
62 LDD APC circuit output 63 LDS APC circuit input	60	PH1	RF signal peak hold capacitor connection
63 LDS APC circuit input	61	BH1	RF signal bottom hold capacitor connection
'	62	LDD	APC circuit output
64 (NC) No connection	63	LDS	APC circuit input
	64	(NC)	No connection

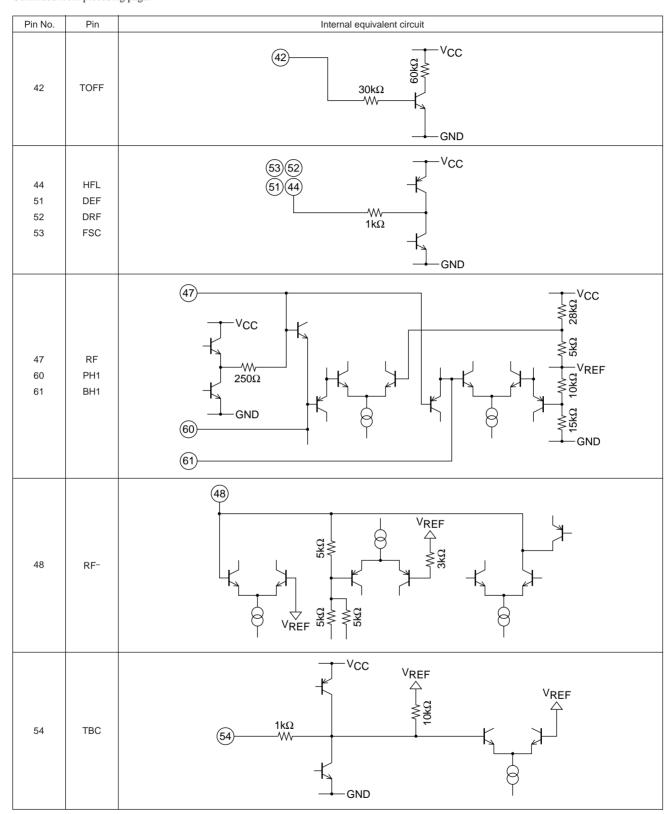
Pin Circuits

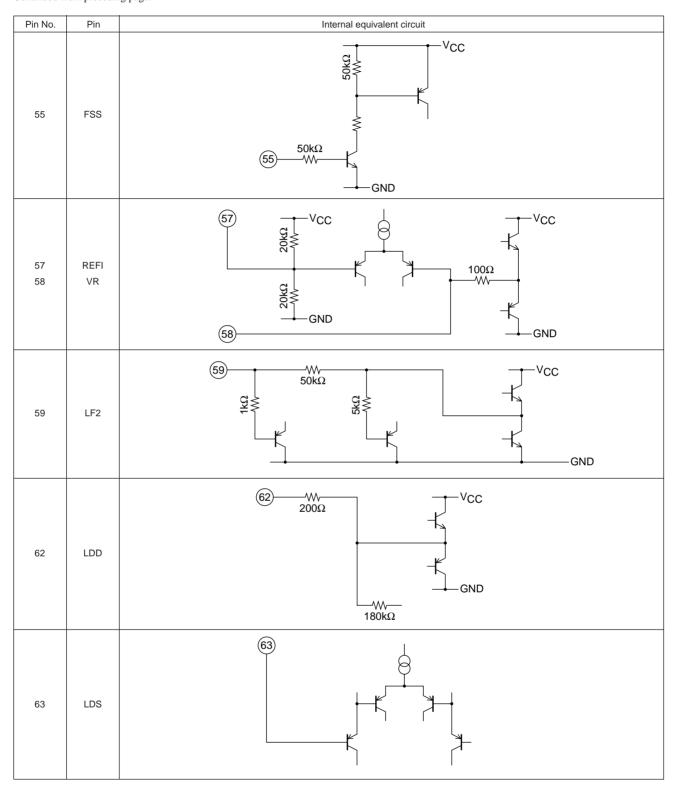




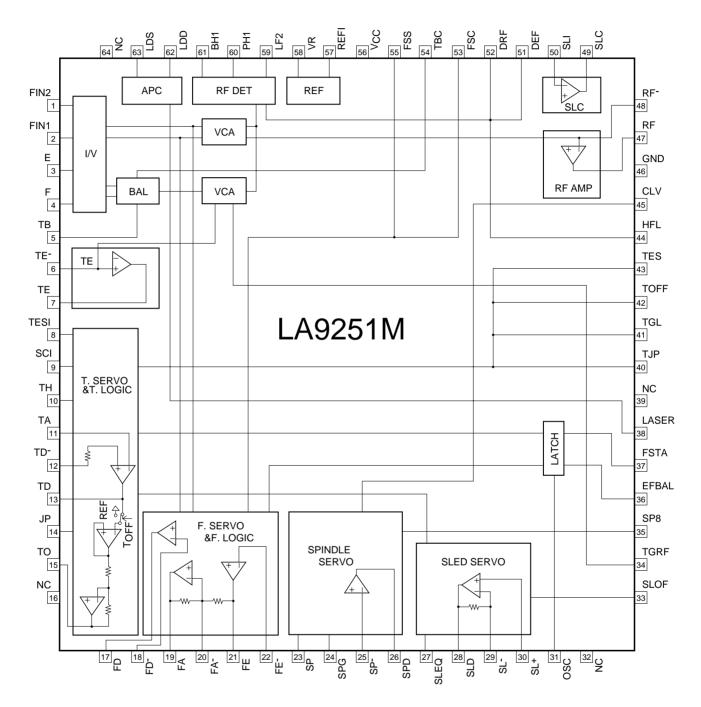








Equivalent Circuit



A12228

Operation

1. APC (Auto Laser Power Control)

This circuit controls the laser power, turning the laser on and off (pin 38). The laser is turned on when the LASER pin is high.

2. RF amplifier (eye pattern output)

The pickup photodiode output current input to FIN1 (pin 2) and FIN2 (pin 1) is I/V converted, passed through an AGC circuit, and output from the RFSUM amplifier RF pin (pin 47). The built-in AGC circuit has a variable range of about ± 4 dB, and its time constant is set by the external capacitor connected to PH1 (pin 60). The EFM signal bottom level is also controlled, and the response is set by the external capacitor attached to PH1 (pin 60). The center gain for the AGC variable range is set by the value of the resistor between RF (pin 47) and RF- (pin 48). If required, these pins can also be used for EFM signal 3T compensation.

3. SLC (Slice Level Controller)

Since the SLC circuit sets the duty of the EFM signal input to the DSP to 50%, the DC level is controlled by integrating the EFMO signal from the DSP.

4. Focus Servo

The focus error signal is acquired by detecting the difference between (A + C) and (B + D) from the pickup and the result is output from FE (pin 21). The FE signal gain is set by the value of the resistor between FE and FE- (pin 22). The FA amplifier is the pickup phase compensation amplifier, and its equalization curve is set by an external capacitor and resistor.

The FD amplifier provides a phase compensation circuit and a focus search signal synthesis function.

A focus search operation is started by switching FSTA (pin 37) from low to high. A ramp waveform is generated by an internal oscillator; this ramp completes in about 560 ms. We recommend holding FSTA (pin 37) high until another focus search is to be performed. Focus is detected (the focus zero cross state) from the focus error signal generated, in effect, by this waveform, and this turns the focus servo on. The ramp waveform amplitude is set by the value of the resistor between FD (pin 17) and FE⁻ (pin 18).

Since FSC (pin 53) is used to smooth the focus search ramp waveform, a capacitor is connected between FSC and VR (pin 58). FSS (pin 55) switches the focus search mode; when FSS is shorted to VCC the circuit performs a + search with respect to the reference voltage VR, and when open or shorted to ground, it performs $a \pm search$.

5. Tracking Servo

The pickup photodiode output current input to E (pin 3) and F (pin 4) is I/V converted and passed first through a balance adjustment VCA circuit and then through a VCA circuit that performs gain following for the RF AGC circuit. The resulting signal is then output from TE (pin 7). The gain follower function can be turned off by setting TGRF (pin 34) high.

The tracking error gain is set by the value of the resistor between TE- (pin 6) and TE (pin 7).

The TH amplifier detects either the JP signal or the TGL signal from the DSP, and functions to change the response characteristics of the servo according to the THLD signal generated internally. When a defect is detected, the circuit switches to THLD mode internally. Set DEF (pin 51) low to prevent this. Note that an external bandpass filter that extracts only the shock component from the tracking error signal is formed on SCI (pin 9), and that the gain is automatically increased if this signal is inserted.

The TA output (pin 11) has an internal resistor so that a low-pass filter can be formed.

The TD amplifier circuit is provided to perform servo loop phase compensation, and its characteristics are set by external RC components. This amplifier also provides a muting function, and the servo can be turned off by setting TOFF (pin 42) high.

The TO amplifier provides a function for synthesizing JP pulses, and JP (pin 14) is used to set the JP pulse conditions.

The E/F balance adjustment operation is started by switching EFBAL (pin 36) from low to high. After that, the adjustment operation is performed by a clock generated by an internal oscillator, and the adjustment completes in about 500 ms. We recommend holding EFBAL (pin 36) high until the next time an E/F balance operation is to be performed.

This adjustment operation must be performed over the disc pit area, not over the disc mirror area. Note that applications must take measures to assure that a stable TE signal is acquired so that track kick operations do not occur during the adjustment. (This includes sled feed commands from the microcontroller.)

The E/F balance adjustment precision and adjustment range can be set to be optimal for the pickup characteristics by the value of the resistor between TBC (pin 54) and the reference voltage, VR.

6. Sled Servo

The response characteristics are set at SLEQ (pin 27). The amplifier that follows SLEQ has a muting function, and the sled servo can be turned off by setting SLOF (pin 33) high.

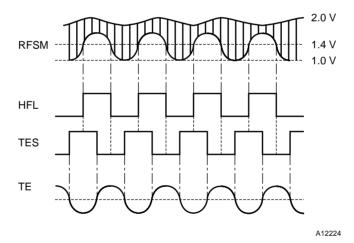
Sled feed is performed in a current input form at SL⁻ (pin 29) and SL⁺ (pin 30). In particular, a resistor is connected to a microcontroller output port and the feed gain is set by the value of that resistor.

7. Spindle Servo

A servo circuit that holds the disc at a constant linear velocity is formed by the internal servo circuit in conjunction with the DSP. A signal from the DSP is accepted by CLV (pin 45), and output from SPD (pin 26). The phase compensation characteristics are set by SP (pin 23), SP⁻ (pin 25), and SPD. The 12 cm mode amplifier gain is set by a resistor connected between SPG (pin 24) and the reference voltage. In 8 cm mode, this amplifier is internally buffered and not affected by SPG. The circuit switches to 8 cm mode when SP8 (pin 35) is set high.

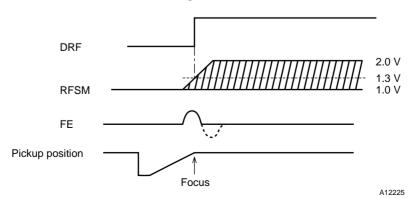
8. TES and HFL (Traversal signal)

The sub-beam signals from the pickup are connected to E (pin 3) and F (pin 4) so that HFL and TES have the phase relationship shown in the figure when the pickup moves from the outside towards the inside of the disc. The TES comparator has a hysteresis of about ± 100 mV at the minus polarity of the comparator with respect to the TESI (pin 8) input. An external bandpass filter is formed so that only the required signal is extracted from the TE signal.



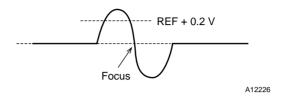
9. DRF (Optical level decision)

A peak hold operation is applied to the EFM signal (RF output) by a capacitor at PH1 (pin 60), and DRF goes high when the RF peak value exceeds about 1.3 V (when $V_{CC} = 3.0 \text{ V}$). The PH1 capacitor is related to the settings of both the DRF detection time constant and the RF AGC response.



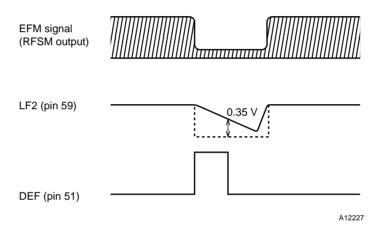
10. Focus Detection

The pickup is seen as being in focus when, after a VR + 0.2 V level is detected in the focus error signal S-curve, that S-curve next goes to the VR level.



11. Defect Detection

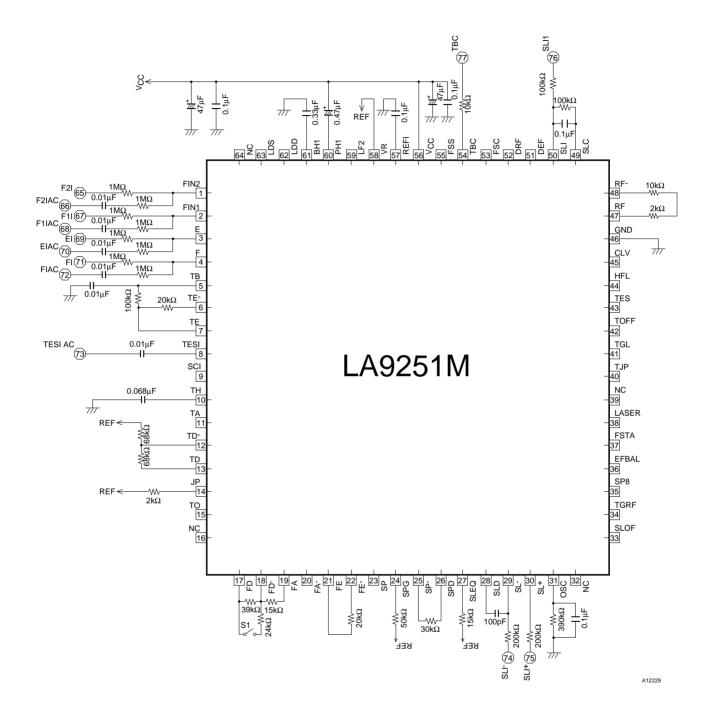
The mirror surface level is held by the capacitor on LF2 (pin 59), and DEF (pin 51) goes high if a drop in the EFM signal (RF output) exceeds about 0.35 V. When DEF goes high, the tracking servo goes to THLD mode. When a defect is detected applications can prevent the LA9251M from going to THLD mode either by setting DEF to low or by setting LF2 (pin 59) low and thus setting the LA9251M not to output DEF.



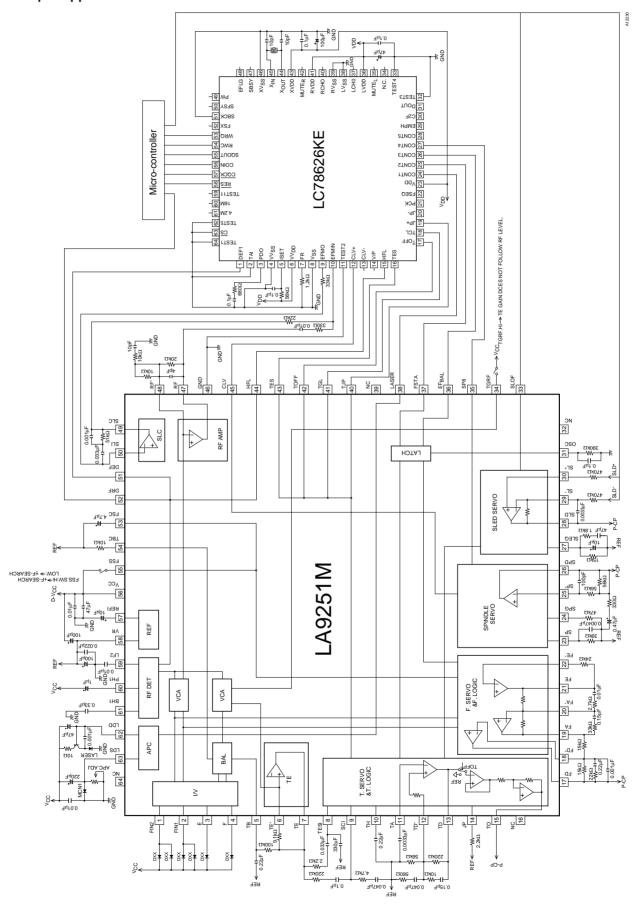
12. Oscillator Circuit

The oscillator frequency is set by the external RC circuit attached to OSC (pin 31). This oscillator frequency is used as the reference clock for focus search and E/F balance adjustment.

Test Circuit



Sample Application Circuit



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