

**SANYO****2-Channel BTL Power Amplifier(35W+35W)  
with Standby Switch for Car Stereos****Preliminary****Overview**

The LA4728 is a BTL two-channel power IC for car audios developed in pursuit of excellent sound quality. Low-region frequency characteristics have been improved through the use of a new NF capacitorless circuit, and crosstalk which causes "muddy" sound has been reduced by improving both circuit and pattern layout. As a result the LA4728 provides powerful bass and clear treble.

**Features**

- High power. supports total output of 35W+35W. [EIAJ power] ( $V_{CC}=14.4V$ , THD=30%,  $R_L=4\Omega$ )
- Less pop noise.
- Designed for excellent sound quality. ( $f_L < 10Hz$ ,  $f_H = 130kHz$ )
- Any rise time settable by an external capacitor.
- Standby switch circuit on chip. (microcontroller supported)
- Various protectors on chip. (output-to-ground short / output-to- $V_{CC}$  short / load short / overvoltage / thermal shutdown circuit)
- The LA4728 is pin-compatible with the LA4725.

**Specifications****Maximum Ratings** at  $T_a=25^\circ C$ 

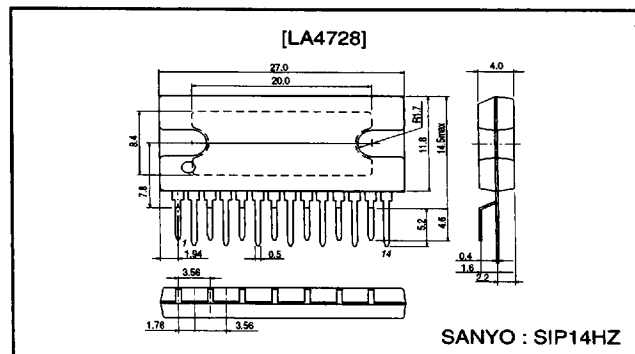
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		18	V
Surge supply voltage	$V_{CC}$ surge	$f \leq 0.2s$ , single giant pulse	50	V
Maximum output current	$I_O$ peak	Per channel	3.5	A
Allowable power dissipation	$P_d$ max	With arbitrarily large heat sink	32	W
Operating temperature	$T_{opr}$		-35 to +85	$^\circ C$
Storage temperature	$T_{stg}$		-40 to +150	$^\circ C$

**Recommended Conditions** at  $T_a=25^\circ C$ 

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}$		13.2	V
Operating voltage range	$V_{CC}$ op	Range where $P_d$ max is not exceeded	9 to 16	V
Recommended load resistance	$R_L$ op		4	$\Omega$

**Package Dimensions**

unit: mm

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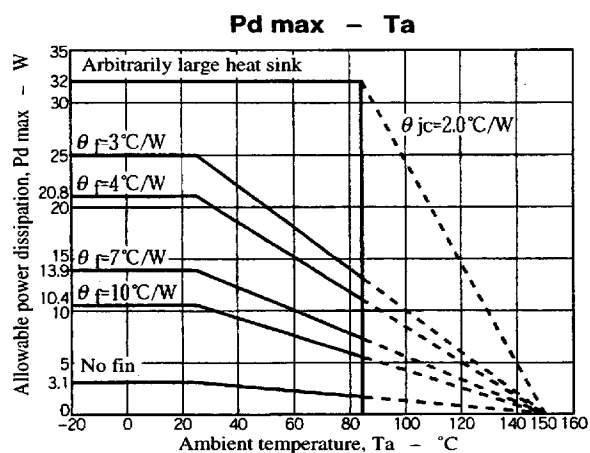
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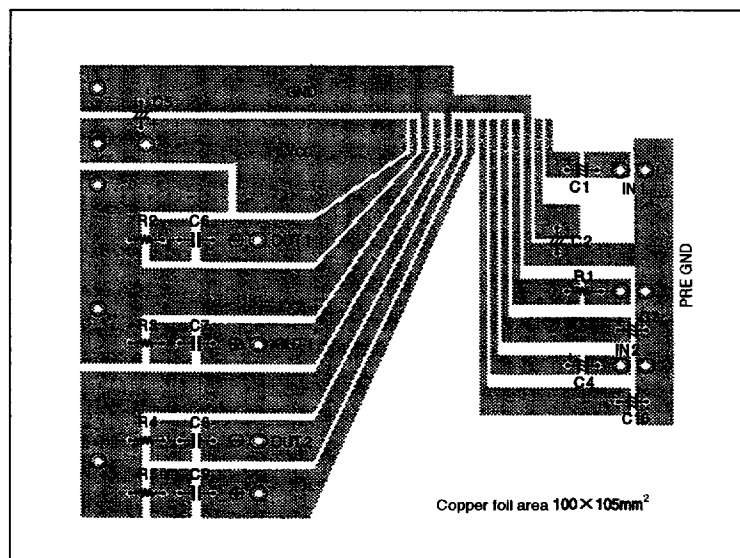
## LA4728

**Operating Characteristics** at  $T_a=25^\circ\text{C}$ ,  $V_{CC}=13.2\text{V}$ ,  $R_L=4\text{k}\Omega$ ,  $f=1\text{kHz}$ ,  $R_g=600\Omega$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	$I_{CCO}$	$R_g=0$	70	125	250	mA
Standby current	$I_{ST}$			10	60	$\mu\text{A}$
Voltage gain	VG		38	40	42	dB
Total harmonic distortion	THD	$P_O=1\text{W}$		0.06	0.2	%
Output power	$P_{O1}$	$R_L=4\Omega$ , THD=10%, $V_{CC}=13.2\text{V}$	16	20		W
	$P_{O2}$	$R_L=4\Omega$ , THD=10%, $V_{CC}=14.4\text{V}$		25		W
	$P_{O3}$	$R_L=4\Omega$ , THD=30%, $V_{CC}=14.4\text{V}$		35		W
Output offset voltage	$V_N$ offset	$R_g=0$	-300		+300	mV
Output noise voltage	$V_{NO}$	$R_g=0$ , B.P.F.=20Hz to 20kHz		0.1	0.5	mVrms
Ripple rejection ratio	SVRR	$R_g=0$ , $f_R=100\text{Hz}$ , $V_R=0\text{dBm}$	40	50		dB
Channel separation	Chsep	$R_g=10\text{k}\Omega$ , $V_O=0\text{dBm}$	50	60		dB
Input resistance	$R_i$		21	30		$\text{k}\Omega$
Standby pin applied voltage	$V_{st}$	Amp on, applied through $10\text{k}\Omega$	2.5		$V_{CC}$	V



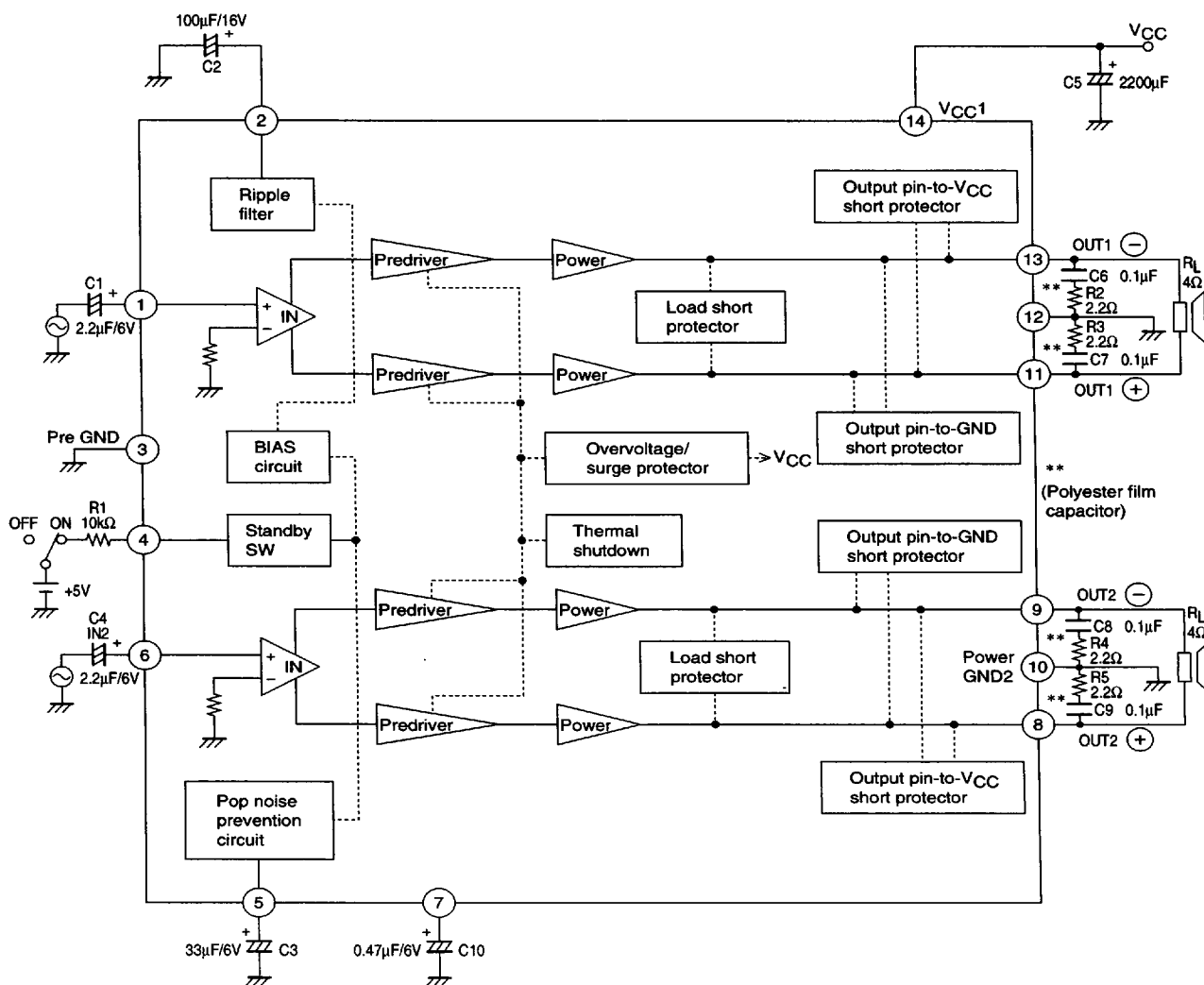
### Sample Print Pattern



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Block Diagram and Sample Application Circuit



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