SAMSUNG ELECTRONICS

KS88C8016
8-Bit CMOS Microcontroller

Data Sheet

DESCRIPTION

The KS88C8016 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. Important features include two 8-bit timer/counters, 16-bit and 20-bit timer/counter arrays with powerful data capture and compare functions, two-channel PWM output, A/D converter, and a serial I/O interface. The KS88C8016 is a powerful and flexible design solution for a wide range of general-purpose consumer electronics applications.

FEATURES

CPU

- SAM8 CPU core

Memory

- 336-byte internal register file
- 16-Kbyte program memory

Instruction Set

- 79 instructions
- IDLE and STOP instructions for power-down

Instruction Execution Time

- 500 ns at 12 MHz f_{OSC} (min.)

Interrupts

- 29 interrupt sources, 15 vectors, 8 levels
- Fast interrupt processing for one level

Clock Oscillation Circuit

- Maximum 12-MHz CPU clock

I/O Ports

- Five I/O ports (total 40 pins):
- Three nibble-programmable ports
- Two bit-programmable ports for external interrupts

Timer/Counters

- Two 8-bit timer/counters
- 16-bit timer/counter array (two modules)
- 20-bit timer/counter array with six modules

Serial I/O Interface

- One pin for serial data I/O
- One pin for serial clock I/O
- Selectable transmit and receive rates

A/D Converter

- Eight pins for analog or normal input
- 8-bit digital converter resolution
- 16-µs conversion speed with 12-MHz CPU clock

Pulse Width Modulation

- Two pins for PWM output
- Frequency: 11.72 kHz to 46.88 kHz with 12-MHz CPU clock
- 14-bit resolution (8-bit frame)
- Push-pull circuit type

Sync Signal Processing

- V-sync separation from C-sync input
- Pseudo H-sync pattern generator output

Backup Timer

- 16-bit clock update timer

Operating Temperature Range

- – 20°C to + 85°C

Operating Voltage Range

- 4.5 V to 6.0 V

Package Type

- 80-pin QFP

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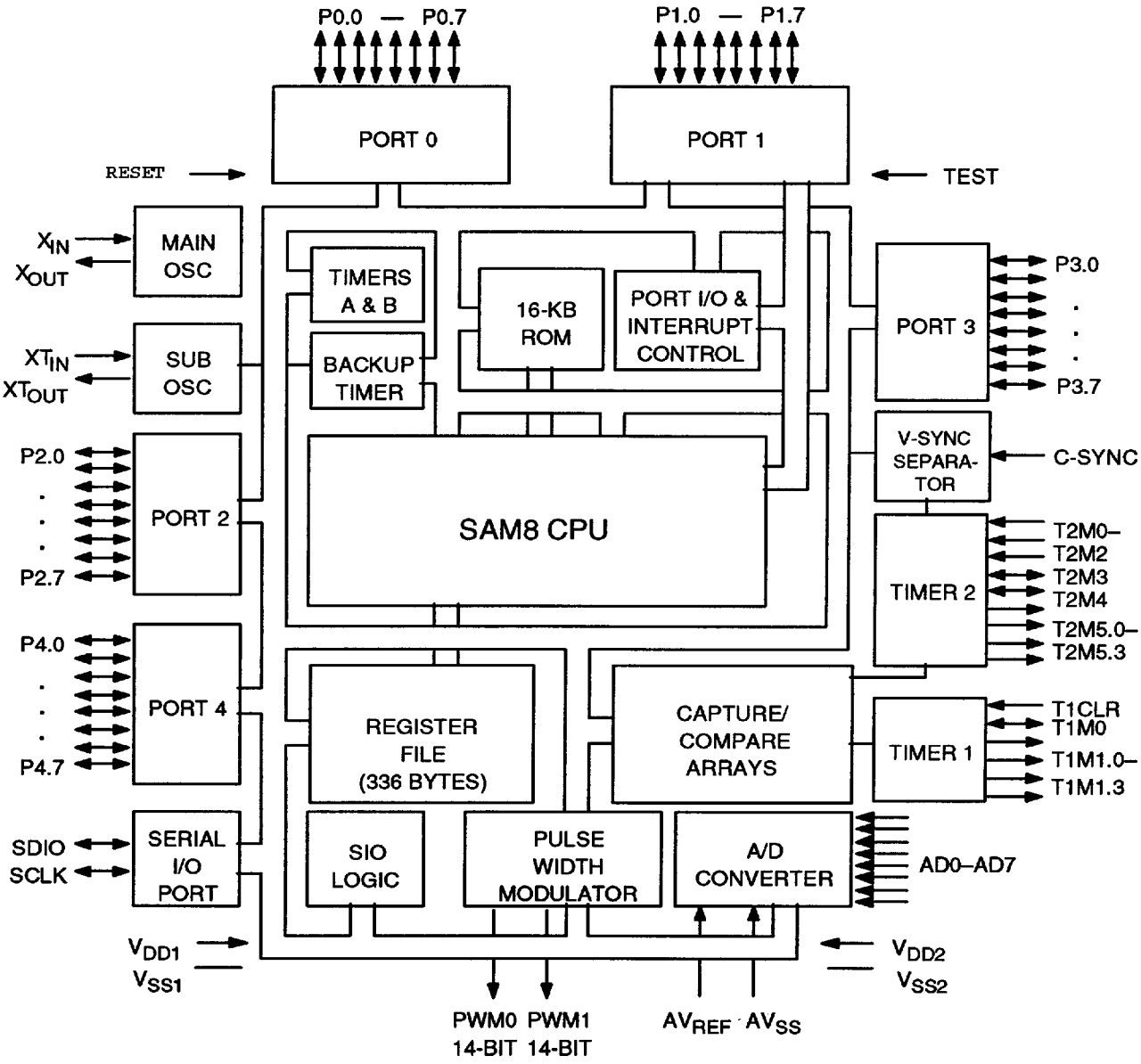
BLOCK DIAGRAM



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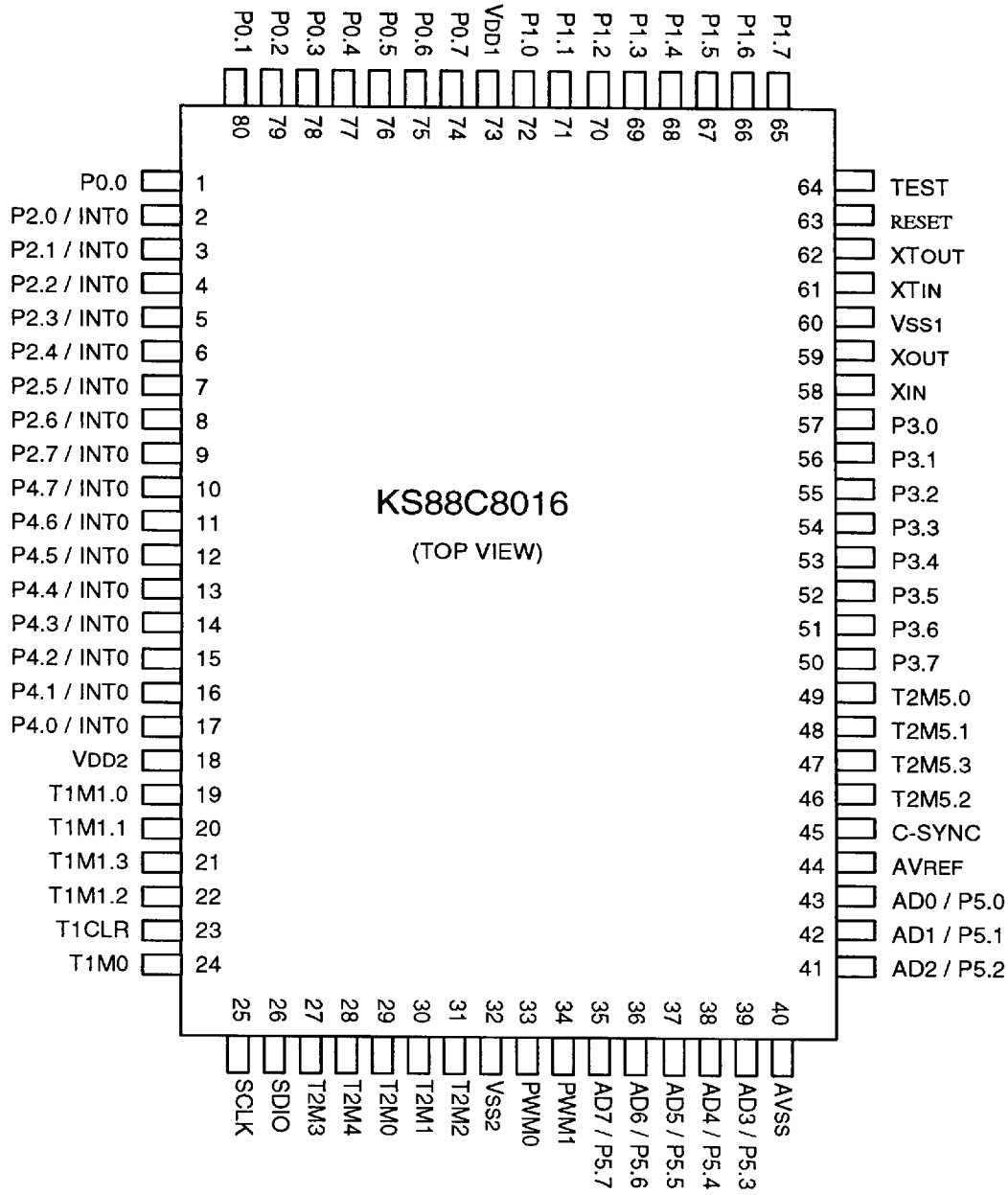
PIN ASSIGNMENTS



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PIN DESCRIPTIONS

Pin Name	Pin Type	Pin Description	Pin Number	Share Pins
P0.0–P0.7	I/O	General I/O port with nibble-programmable pins. Input or output mode and pull-ups are software-assignable. The output circuit type is designed for normal current only.	1, 80–74	–
P1.0–P1.7	I/O	General I/O port. Same as port 0, but with maximum 8-volt load capability	72–65	–
P2.0–P2.7 P4.0–P4.7	I/O	General I/O port. Input or output mode and pull-up resistors can be assigned by software. Alternately, pins can be configured individually as external interrupt inputs with interrupt control and noise filters	2–9, 17–10	–
P3.0–P3.7	I/O	Same as port 0	57–50	–
P5.0–P5.7	I	General input port. Alternately used for analog input to the A/D converter module	43–41, 39–35	AD0–AD2, AD3–AD7
T1M1.0– T1M1.3	O	Timer1 module1 (pattern generator) compare outputs. Alternately used for normal 4-bit data output	19–22	–
T1CLR	I	External clear signal input to timer1	23	–
T1M0	I/O	Data capture input or compare output for timer 1 module 0 (T1M0)	24	–
T2M0–T2M2	I	Data capture input pin for T2M0–T2M2	29–31	–
T2M3–T2M4	I/O	Data capture input or compare output for timer 2 module 3 and timer 2 module 4	27, 28	–
T2M5.0– T2M5.3	O	Timer 2 module 5 compare output pins. Alternately used for normal 4-bit data output	49–46	–
PWM0, PWM1	O	14-bit pulse width modulator output pins for the PWM0 and PWM1 signals	33, 34	–
C-SYNC	I	C-sync input for V-sync signal separation	45	–
AD0–AD7	I	Analog input pin for A/D converter. Alternately used as general input port 5	43–41, 39–35	P5.0–P5.2, P5.3–P5.7
AV_{REF}, AV_{SS}	–	Reference voltage inputs for A/D converter	44, 40	–
SCLK	I/O	Bi-directional serial data clock pin	25	–
SDIO	I/O	Bi-directional serial data pin	26	–
X_{IN}, X_{OUT}	–	System clock input and output pins	58, 59	–
XT_{IN}, XT_{OUT}	–	Suboscillator clock pins for backup timer	61, 62	–
V_{DD1}, V_{SS1}	–	Power input pins for CPU (internal)	73, 60	–
V_{DD2}, V_{SS2}	–	Power input pins for port output (external)	18, 32	–
RESET	I	System RESET pin (pull-up resistor: 220 k½)	63	–
TEST	I	Test signal input (connect to V_{SS})	64	–

NOTE: V_{DD1} and V_{DD2} must be connected in external circuit (same to V_{SS1} & V_{SS2})

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FUNCTION OVERVIEW

ADDRESS SPACES

Overview

The KS88C8016 microcontroller has two kinds of address space: registers (internal register file) and program memory (ROM).

A 16-bit address bus handles program memory operations. A separate 8-bit register bus carries addresses and data between the CPU and the internal register file. The KS88C8016 does not support external data or program memory.

Program Memory

The KS88C8016 has a 16-Kbyte mask-programmable ROM (0H–3FFFH). Program memory (ROM) stores program code and table data.

The SAM8 interrupt structure supports up to 127 vector addresses. The KS88C8016 interrupt structure uses only 16 vectors. The first 256 bytes of the ROM (0H–FFH) are reserved for this maximum number of vectors. Unused locations in this address range can be used as normal program memory. The RESET address in the ROM is 0020H.

Register File

The 256-byte internal register file is logically extended to duplicate the upper 64-byte area of the register file, as well as the lower 192-byte area, by a factor of two. This extension into separately addressable register sets, banks, and pages is supported by set bank instructions, the register page pointer, and addressing mode restrictions.

The total addressable register space is expanded from 256 bytes to 1120 bytes. The KS88C8016 can access 422 8-bit registers in this maximum 1120-byte space. Thirteen bytes in the internal register file are for system control registers, and 73 bytes for peripheral control and data registers. There are 336 general-purpose registers, including the 16-bit working register area.

Register Addressing

The SAM8 register architecture provides an efficient method of working register addressing that takes full advantage of shorter instruction formats to reduce execution times. Registers can be addressed either as a single 8-bit register or a 16-bit register pair.

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The SAM8 instruction set supports seven addressing modes. Not all of these addressing modes are available for each instruction. The seven addressing modes and their symbols are:

— Register (R)
— Indirect Register (IR)
— Indexed (X)
— Direct Address (DA)
— Indirect Address (IA)
— Relative Address (RA)
— Immediate (IM)

In Register (R) addressing mode, the operand value is the content of a specific register or register pair. You can use this mode to access all locations in the internal register file except for set 2. Working register addressing uses register pointers to select a specific register within a working register space.

To increase the speed of context switches during program execution, you use the register pointers to dynamically select movable 8-byte "slices" of the register file as active working register space.

System and User Stacks

SAM8 uses the system stack to implement subroutine calls and returns, for interrupt processing, and for dynamic data storage. The PUSH and POP instructions support system stack operations.

User stacks can be freely defined in the register file for dynamic data storage. The instructions PUSHUI, PUSHUD, POPUI, and POPUD support user-defined stack operations.

INTERRUPTS

The SAM8 interrupt structure has three basic components: levels, vectors, and sources. The CPU recognizes eight interrupt levels.

The KS88C8016 microcontroller has 29 peripheral interrupt sources. Fifteen vectors support these sources and the interrupt structure uses all eight interrupt levels (IRQ0–IRQ7).

When multiple interrupt levels are active, the interrupt priority register (IPR) determines the order in which contending interrupts are to be serviced.

INTERRUPTS (CONTINUED)

If multiple interrupts occur on the same interrupt level, the interrupt with the lowest vector address is processed first.

Optional high-speed ("fast") interrupt processing is available for external interrupts at ports 2 and 4.

INSTRUCTION SET

The SAM8 instruction set is designed to support a large register file. It includes 79 arithmetic and logical operations, including multiply and divide. Binary-coded decimal (BCD) operations include decimal adjustment of binary values.

Flexible instructions for bit addressing, and for rotate and shift operations complete the powerful data manipulation capabilities of the instruction set.

CLOCK CIRCUITS

An external crystal generates a maximum 12-MHz CPU clock. The X_{IN} and X_{OUT} pins connect the external oscillation source to the on-chip clock circuit. The main oscillator circuit generates the CPU clock signal. To increase processing speed and to reduce noise levels, the clock circuit has non-divided logic.

An on-chip suboscillator circuit runs the backup timer during normal operation and in Stop mode. If a secondary power source is used, it can run the backup timer during a power outage. It requires a separate external oscillation source with a typical operating frequency of 32768 Hz.

RESET and POWER-DOWN MODES

A RESET operation overrides all other operating conditions and puts the KS88C8016 into a known state. To initiate a RESET, the signal level at the RESET pin is held to low level for at least 22 CPU clocks.

Idle Mode

Idle mode is invoked by the instruction IDLE. In Idle mode, the CPU goes inactive while select peripherals (timer 0, and I/O ports 2 and 4) remain active. Port pins retain the mode (input or output) they had at the time Idle mode was entered.

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During Idle mode, the contents of system and peripheral control and data registers are retained. There are two ways to release Idle mode:

— Activate any enabled interrupt, causing Idle mode to be released.

  You can use an externally generated interrupt, the timer B non-maskable interrupt, or a fast interrupt to release Idle mode.

— Execute a RESET operation. If interrupts are masked, a RESET is the only way to release Idle mode.

Stop Mode

The instruction STOP invokes Stop mode. In Stop mode, both the CPU and its peripherals "sleep." In other words, the main oscillator stops and all system functions are halted. Data stored in the internal register file and in peripheral control and data registers is retained. The only way to release Stop mode is by a RESET. All system and peripheral registers are RESET to their default values.

When the signal level at the RESET pin goes High, the CPU executes the program starting from ROM address 0020H.

If the backup timer module is connected to a separate suboscillator, the backup timer remains active during Stop mode.

I/O PORTS

The KS88C8016 has five 8-bit I/O ports, ports 0–4. The CPU accesses these ports by directly writing to or reading from respective port register addresses. Each port can be flexibly configured to meet various system design requirements.

Port 2 and port 4 pins can be configured selectively to either input or output mode. They also can be used as input pins for external interrupt signals.

A/D converter input pins AD0–AD7 can be alternately used as an 8-bit input port 5 (P5.0–P5.7). In addition, the four output pins for timer 1 module 1 (T1M1.0–T1M1.3), and for timer 2 module 5 (T2M5.0–T2M5.3), can alternately serve as normal 4-bit output ports.

TIMER/COUNTER T0 (TIMERS A AND B)

The timer/counter module T0 consists of two 8-bit timer/ counters called timer A and timer B. Each timer/counter has an 8-bit counter with 4-bit prescaler, an 8-bit data register, and an 8-bit comparator. The control registers T0CON and TBINT control module 0 operation. Both timers run continuously and the corresponding count registers cannot be set or RESET directly.

Timer A and timer B operate in either interval mode or pulse width modulation (PWM) mode. However, because the KS88C8016 does not have output pins for PWM output, the timers are restricted to interval mode operation only.

The same clock input drives both timers. There is only one input clock option — the CPU clock frequency divided by 1000. When CPU clock input is disabled, the T0 module also is disabled.

In interval mode, both timers generate a match signal when the count value and the referenced data value in the TADATA or TBDATA register is the same. When a match is detected, the count register is cleared, an interrupt request is generated, and counting resumes.

TIMER/COUNTER ARRAY T1

The timer 1 array (T1) has the following components:

— 16-bit counter (counter 1) with 8-bit prescaler
— 16-bit compare/capture function block (T1M0)
— Pattern generator function block (T1M1)
— Timer 1 control register (T1CON)
— Module control registers (T1M0CON, T1M1CON)
— External timer clear signal input pin (T1CLR)
— One I/O pin for T1M0; four output pins for T1M1

The 16-bit compare/capture module (T1M0) can be set to either capture mode or to compare mode. In capture mode, T1M0 register settings control edge selection (rising, falling, or both).

The pattern generator module (T1M1) has three operating modes: direct output mode, toggle mode, and pattern generation mode. The T1M1 output pins, T1M1.0–T1M1.3, can be programmed to operate in the same mode, or individually in different modes.

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TIMER/COUNTER ARRAY T2

The timer 2 array, commonly used for servo-motor applications, has the following components:

- 16-bit counter (counter 2)
- 4-bit extension counter (T2EX)
- Three 16-bit capture modules (modules 0, 1, 2)
- Two 16-bit capture/compare modules (3 and 4)
- Five 8-bit prescalers for modules 0–4
- 16-bit pattern generator (module 5)
- Timer 2 control register (T2CON)
- Control registers for each module (T2M0CON–T2M5CON)
- One I/O pin each for modules T2M0–T2M4
- Four output pins for the pattern generator T2M5

Modules 0, 1, and 2 are identical capture-only modules with four programmable operating modes. Each module has an input pin connected to an 8-bit prescaler. Module 3 is a capture/compare module with four modes and high-current drive capability. The T2M3 pin input can be used to generate the T2M3 interrupt.

Timer 2 module 4 is similar to module 3 except that it also has a V-sync separator unit. The input to T2M4 can be one of three sources: 1) C-sync signal, 2) V-sync output of the V-sync separator unit, or 3) external input at the T2M4 pin. Eight-bit prescalers are directly connected to the input pins of T2M0–T2M4 for use in timing applications.

T2M5 is a 16-bit pattern generator with a 4-bit output register. It operates exactly like the timer 1 module 1 pattern generator: in direct output mode, toggle mode, or pattern generation mode.

You can use T2M5 to generate head switching outputs, control head pulses in "Record" mode, or to generate a V-lock signal for VCR applications. The T2M5.3 pin also can output an H-sync waveform that conforms to either the NTSC or PAL standard

PULSE WIDTH MODULATION

The KS88C8016 pulse width modulation (PWM) function block has two PWM modules, PWM0 and PWM1.

Each module has the following components:

PULSE WIDTH MODULATION (CONTINUE)

- 8-bit counter with 6-bit extension counter for 14-bit output resolution
- 8-bit reference data register
- 8-bit comparator
- 8-bit extension data register (6 bits are used)
- PWM output pin

Both PWM modules use a single control register, PWMCON. It contains a 2-bit prescaler to permit modification of the CPU clock frequency. By comparing the extension counter value with the extension register value, the duty cycle of the PWM output is "stretched" at specific intervals.

PWM output can be used, for example, in voltage synthetic tuning (VST) tasks in color televisions, and to control on/off timing for external circuits that require high base frequencies.

BACKUP TIMER

The 16-bit backup timer can be used to update the current time for application-specific clock time functions.

A suboscillator clock pulse drives the backup timer. This clock pulse is divided by 32768 (2^{15}) Hz to produce the internal timer clock. (A 32768-Hz crystal generates a slow 1-Hz clock pulse).

To start the backup timer, you write any value to its control register BTCON (E7H). Because the counter value itself cannot be written, this write operation simply clears the counter to ensure that counting will resume from 0000H. The CPU can always read the current counter value.

NOTE

The interrupt generation function controlled by BTCON is not included in the KS88C8016.

A/D CONVERTER

The 8-bit A/D converter (ADC) module uses successive approximation logic to convert analog levels at one of the eight input channels to equivalent

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8-bit digital values. The analog input level must lie between the AV_{REF} and AV_{SS} values.

The A/D converter has the following components:

— Analog comparator
— Successive approximation register
— D/A converter logic (resistor ladder type)
— ADC control register (ADCON)
— Eight multiplexed analog data input pins (AD0–AD7)
— 8-bit A/D conversion data output register (ADOUT)
— 8-bit digital input register (ADIN, port 5)
— AV_{REF} and AV_{SS} input pins

An analog-to-digital conversion procedure is initiated when the CPU writes a value to the ADCON register at address 28H to select the ADn input pin. You select the desired input channel (AD0–AD7) by setting the appropriate SCHn bits in the ADCON register.

The KS88C8016 performs 8-bit conversions for only one input channel at a time. Channels can be selected dynamically by manipulating the SCH bits (SCH0–SCH2) in ADCON.

The A/D conversion process requires 24 CPU clocks to convert each bit and therefore requires 192 clocks to complete an 8-bit conversion. The digital result is then dumped into the output register ADOUT at address 2AH. The A/D converter unit then enters an idle state. Because the ADC does not generate an interrupt to signal a completed conversion, the contents of ADOUT must first be read out before another conversion starts. Otherwise, the previous result will be overwritten.

SERIAL I/O INTERFACE

The serial data I/O (SIO) module can interface with various external devices requiring serial data transfer. SIO operations start when the CPU writes data to the SIO shift register (address E9H, set 1, bank 0).

On the basis of current SIOCON register settings, the SIO unit either transmits or receives eight bits of data, one bit at a time, on each edge of its internal or external shift clock.

When one 8-bit serial transmit or receive operation is completed, the SIO unit enters an idle state until the CPU again writes data to the shift register.

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D.C. ELECTRICAL CHARACTERISTICS

(T_A = −20°C to +85°C, V_{DD} = 4.5 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	All input pins except as specified for V_{IH2}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}, XT_{IN}	V_{DD} – 0.5		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}, XT_{IN}			0.4	
Output High Voltage	V_{OH1}	V_{DD} = 4.5 V to 6.0 V I_{OH} = −1 mA Port 1, T2M3, and T2M5.2	V_{DD} – 1.0	–	–	V
		If I_{OH} = −200 µA	V_{DD} – 0.5			
	V_{OH2}	V_{DD} = 4.5 V to 6.0 V I_{OH} = −200 µA All output pins except V_{OH1}	V_{DD} – 1.0			
		If I_{OH} = −60 µA	V_{DD} – 0.5			
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 15 mA Port 1, T2M3, and T2M5.2	–	–	1.0	V
	V_{OL2}	I_{OL} = 2 mA All output pins except V_{OL1}			0.4	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN} and XT_{IN}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN} and XT_{IN}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, XT_{IN}, and RESET	–	–	−3	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN}, and XT_{IN}			−20	
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0 V	–	–	−3	µA
Pull-up Resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Port 0, 1, 2, 3, and 4	25	47	70	KΩ

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	R_{L2}	V_{DD} = 5 V ± 10% RESET only	120	220	320	

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D.C. ELECTRICAL CHARACTERISTICS (Continued)

(T_A = −20°C to +85°C, V_{DD} = 4.5 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current (See Note)	I_{DD1}	V_{DD} = 5 V ± 10% 8-MHz crystal oscillator	–	19	45	mA
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10% 8-MHz crystal oscillator		2.7	10	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10% 32-kHz crystal suboscillator		90	200	µA
		If V_{DD} = 3 V ± 10%		10	50	
	I_{DD4}	Stop mode; XT_{IN} = 0 V Crystal suboscillator stopped V_{DD} = 5 V ± 10%	–	1.5	20	µA
		If V_{DD} = 3 V ± 10%		0.1	5	

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

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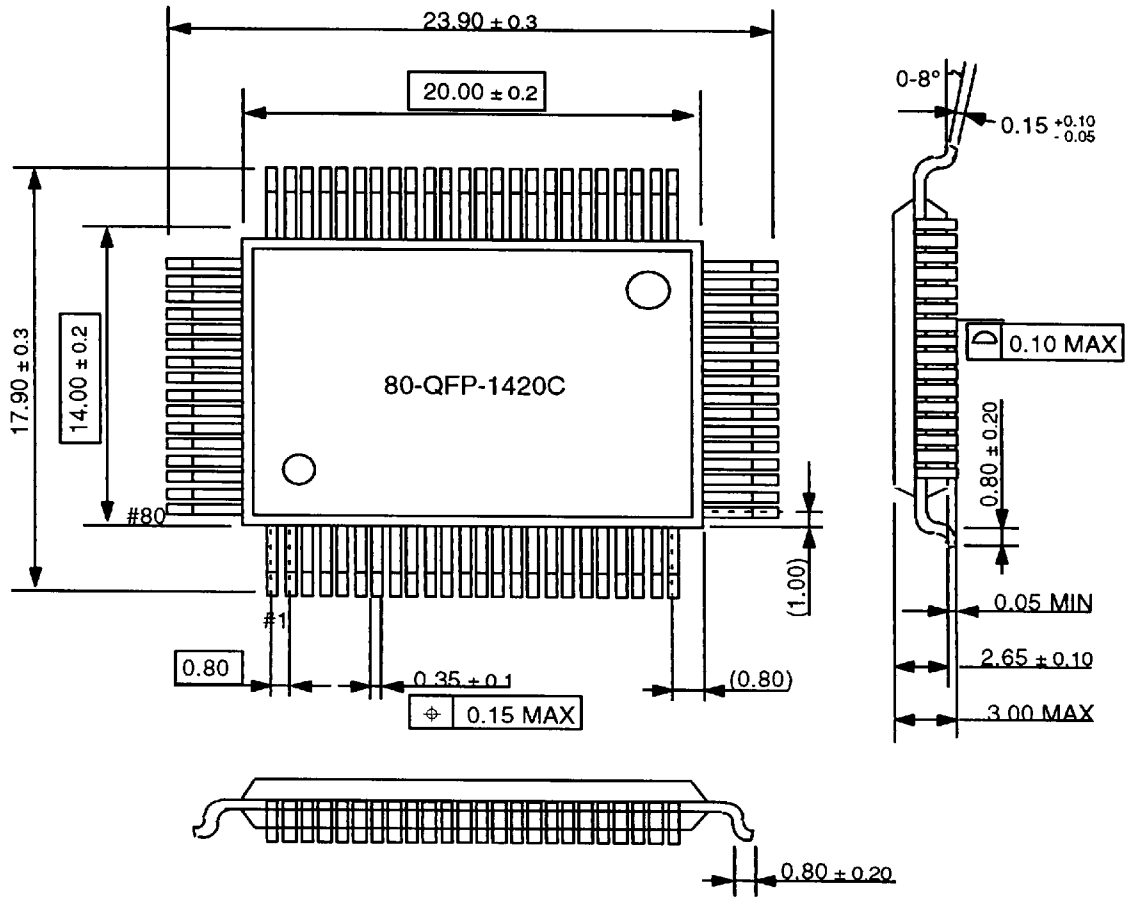
PACKAGE DIMENSIONS



NOTE: Dimensions are in millimeters.

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