FAN8047G3

4-CH Motor Driver (5 Input & 4 Output)

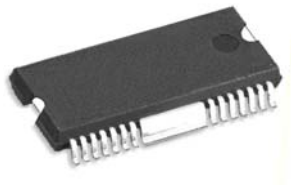
Features

- 4-CH Balanced transformerless (BTL) driver
- Optional input (CH4,5) for output CH4
- Operating supply voltage : 4.5 V ~ 14V
- Built-in thermal shut down circuit (TSD)
- Built-in channel mute circuit
- Built-in 3.3 volt regulator

Description

The FAN8047G3 is a monolithic integrated circuit suitable for a 4-ch motor driver which drives a tracking actuator, a focus actuator, a sled motor, a spindle motor, and a tray motor of the CDP/CAR-CD/DVDP systems.

28-SSOPH-375SG2



Typical Application

- Compact disk player
- Video compact disk player
- Car compact disk player
- Digital video disk player

Ordering information

DEVICE	PACKARE	OPERATING TEMP
FAN8047G3	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8047G3X[note1]	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8047G3_NL[note2]	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8047G3X_NL	28-SSOPH-375-SG2	-35°C ~ +85°C

Notes:

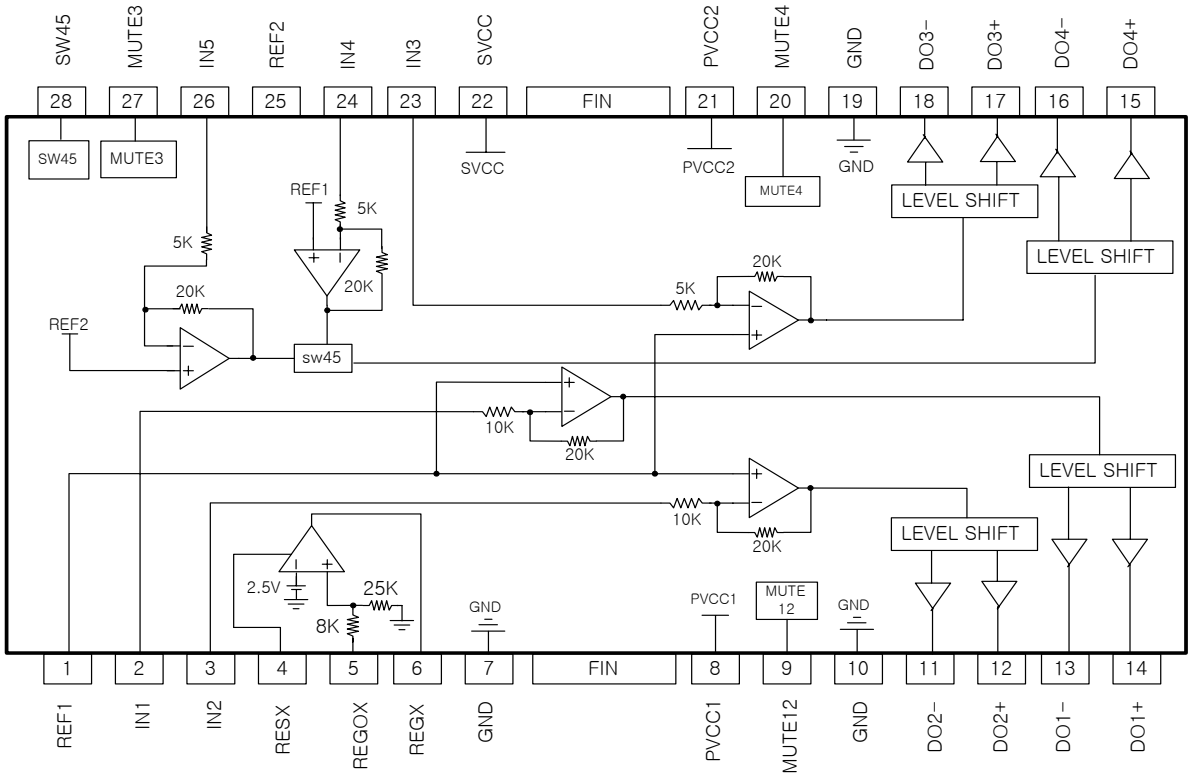
1. X : Tape&Reel
2. NL : Lead free

Pin assignments

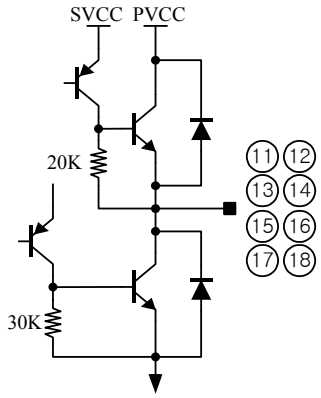
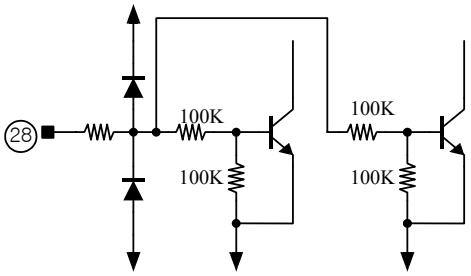
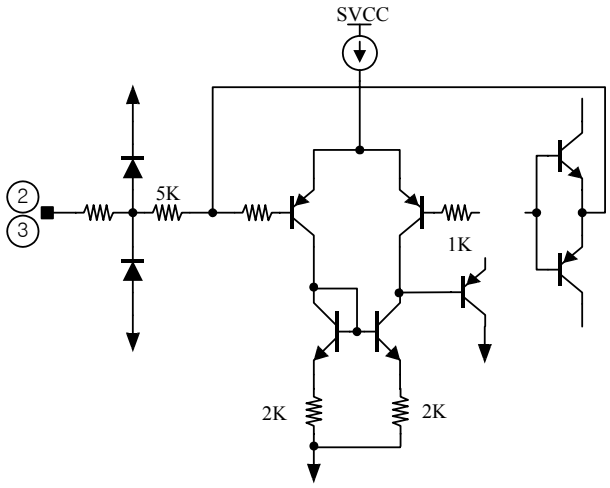
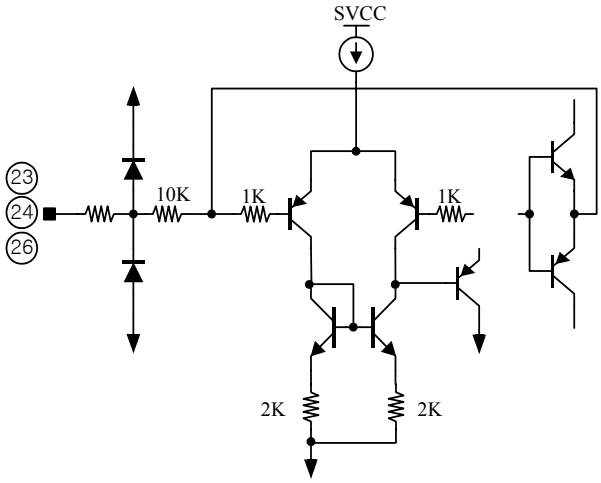
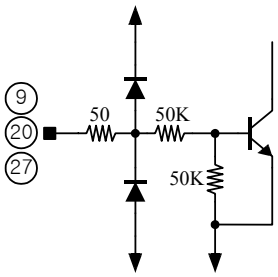
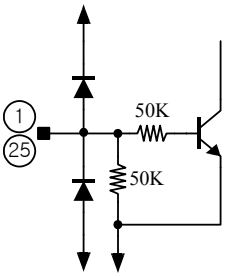
Pin definitions

PIN NUMBER	PIN NAME	I/O	PIN FUNCTION DESCRITION
1	REF1	I	Bias voltage input
2	IN1	I	CH1 Input
3	IN2	I	CH2 Input
4	RESX	I	Regulator reset
5	REGOX	I	Regulator feedback input
6	REGX	O	Regulator output
7	GND	-	Signal ground
8	PVcc1	-	Power Vcc (CH1,CH2)
9	MUTE12	I	Mute 1,2
10	GND	-	Power ground (CH1,CH2)
11	DO2-	O	CH2 Drive output (-)
12	DO2+	O	CH2 Drive output (+)
13	DO1-	O	CH1 Drive output (-)
14	DO1+	O	CH1 Drive output (+)
15	DO4+	O	CH4 Drive output (+)
16	DO4-	O	CH4 Drive output (-)
17	DO3+	O	CH3 Drive output (+)
18	DO3-	O	CH3 Drive output (-)
19	GND	-	Power ground (CH3,CH4)
20	MUTE4	I	Mute 4
21	PVcc2	-	Power Vcc (CH3,CH4)
22	SVcc	-	Signal Vcc
23	IN3	I	CH3 Input
24	IN4	I	CH4 Input
25	REF2	I	REF2
26	IN5	I	CH5 Input
27	MUTE3	I	Mute 3
28	SW45	I	Select switch for CH4,5

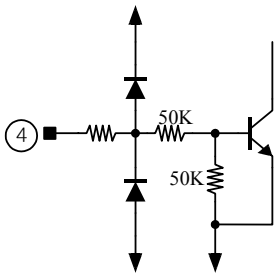
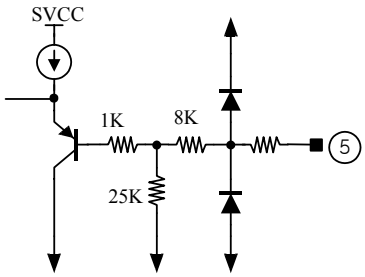
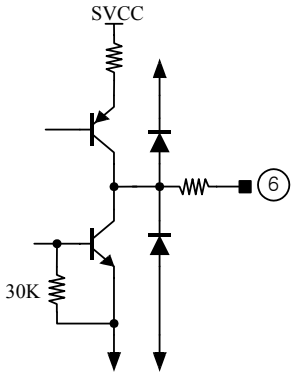
Internal block diagram



Equivalent circuits

BTL Driver output	SW45
	
BTL Input(CH1,2)	**BTL Input(CH3,4,5)**
	
Mute	**Reference**
	

Equivalent circuits(Continued)

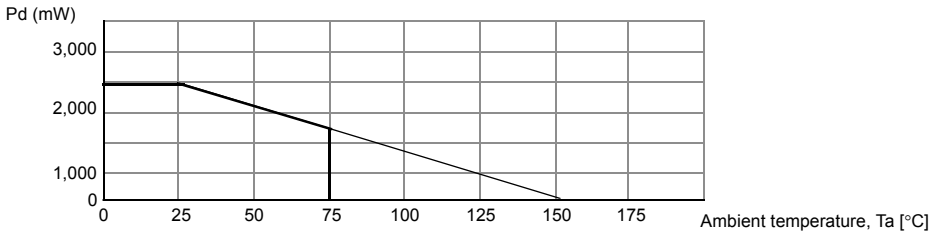
Regulator reset	Regulator feedback input
	
Regulator output	
	

Absolute maximum ratings (Ta=25°C)

PARAMETER	SYMBOL	VALUE	UNIT
Maximum supply voltage	$SVCC_{MAX}$	18	V
	$PVCC1_{MAX}$	18	V
	$PVCC2_{MAX}$	18	V
Power dissipation	P_D	2.5[note1,2,3]	W
Operating temperature	T_{OPR}	−35 ~ +85	°C
Storge temperature	T_{STG}	−55 ~ +150	°C
Maximum output current	I_{OMAX}	1	A

Notes:

1. When it is mounted on 70mm × 70mm × 1.6mm PCB.
2. Power dissipation decreases at the rate of 20mW/°C in T_A >25°C.
3. Do not exceed P_D and SOA.



Recommended operating conditions (Ta=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating supply voltage	SVCC	4.5	-	14	V
	PVCC1	4.5	-	SVCC	V
	PVCC2	4.5	-	SVCC	V

Electrical characteristics

(SV_{CC} = PV_{CC2} = 12V, T_A = 25°C, PV_{CC1} = 5V, Ref1= 1.65V, Ref2 = 2.5V, RL = 8Ω)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent circuit current	I_{CC}	Under no-load	-	17	25	mA
BTL Driver circuit (R_L=8Ω)						
Output offset voltage(CH12)	V_{OOF1}	V_{IN}=1.65V	–50	-	+50	mV
Output offset voltage(CH34)	V_{OOF2}	V_{IN}=1.65V	–100	-	+100	mV
Output offset voltage(CH5)	V_{OOF3}	V_{IN}=2.5V	–100	-	+100	mV
Maximum output voltage(CH12)	V_{OM1}	PVcc1=5V, R_L=8Ω	3.6	4.0	-	V
Maximum output voltage(CH34)	V_{OM2}	PVcc2=12V, R_L=24Ω	9.6	10.5	-	V
Close-loop voltage gain(CH12)	A_{VF}	V_{IN}= 0.3V	15.5	17.5	19.5	dB
Close-loop voltage gain(CH34)	A_{VF}	V_{IN}= 0.3V	21.5	23.5	25.5	dB
Regulator circuit (SVCC,PVCC2=12V)						
Load regulation	ΔV_{RL}	I_L=0 →□ 200mA	-10	0	+10	mV
Line regulation	ΔV_{CC}	I_L=200mA, V=6V →□ 9V	-20	0	+30	mV
Regulator output voltage 1	V_{REG1}	I_L=100mA	3.135‘	3.3	3.465	V
Regulator reset on voltage	Reson	Pin4=Variation	-	-	0.5	V
Regulator reset off voltage	Resoff	Pin4=Variation	2	-	-	V
Mute and other function circuit						
Mute on voltage	V_{MON}	Pin9,20,27=Variation	-	-	0.5	V
Mute off voltage	V_{MOFF}	Pin9,20,27=Variation	2	-	-	V
SW on voltage	V_{SWL}	Pin28=Variation	-	-	0.5	V
SW off voltage	V_{SWH}	Pin28=Variation	2	-	-	V
Mute low level sink current	IMTL	VMUTE = 0V	-15	0	15	uA
Mute high level sink current	IMTH	VMUTE = 5V	-	85	170	uA
SW45 Low level sink current	ISWL45	SW45 = 0V	-15	0	15	uA
SW45 High level sink current	ISWH45	SW45 = 5V	-	85	170	uA
REF1 Sink current	IRL	REF1 = 1.65V	-	52	104	uA
REF2 Sink current	IRH	REF2 = 2.5V	-	85	170	uA

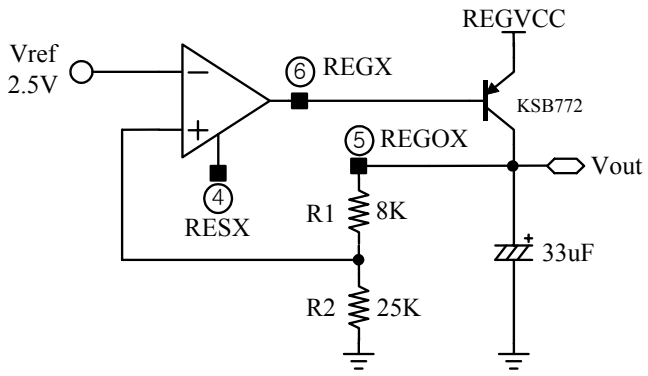
(* note) : Guaranteed field. (No EDS/ Final test .)

Application information

1. MUTE, REF & SW45 Function

INPUT						OUTPUT					
SW45	MUTE12	MUTE3	MUTE4	REF1	REF2	BTL			PRE-AMP		REG
						CH12	CH3	CH4	CH4	CH5	
H	H	H	-	H	-	ON	ON	IN4	ON	ON	ON
H	H	L	-	H	-	ON	OFF	IN4	ON	ON	ON
H	H	H	-	L	-	OFF	OFF	OFF	OFF	ON	ON
H	L	H	-	H	-	OFF	ON	OFF	ON	ON	ON
H	L	L	-	H	-	OFF	OFF	OFF	ON	ON	ON
L	-	-	L	-	-	OFF	OFF	OFF	OFF	ON	ON
L	-	-	H	-	H	OFF	OFF	IN5	OFF	ON	ON
L	-	-	H	-	L	OFF	OFF	OFF	OFF	ON	ON

2. Regulator & Reset function



- The external circuit is composed of the transistor, KSB772 and a capacitor, about 33uF.
- The capacitor is used as a ripple eliminator.
- The capacitor must have a good temperature characteristics.
- The regulator output voltage is decided as follows.

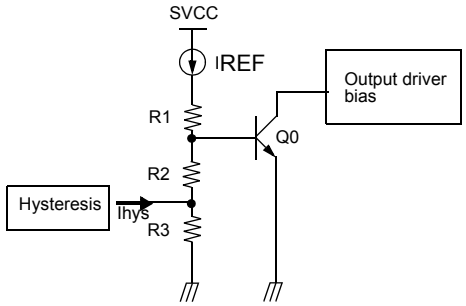
$$V_{out} = V_{ref} \times (1 + \frac{R1}{R2})$$

$$= 2.5 \times \frac{8K}{25K} = 3.3V$$

- When the voltage of the pin 4(RESX) is high, the regulator circuit operates normally. When the voltage of pin 4(RESX) is low, the regulator circuit is disabled.

3. TSD Function

- When the chip temperature reaches to 160°C by abnormal condition, the TSD circuit is activated.
- This makes the bias current of the output drivers shut down, and all the output drivers are on cut-off state. Therefore the chip temperature begins to decrease.
- When the chip temperature falls to 140°C, the TSD circuit is deactivated and the output drivers start to operate normally.
- The TSD function does not affect regulator operation.



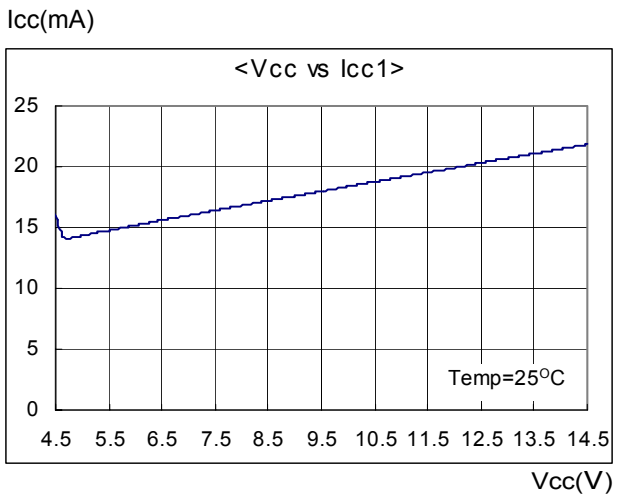
4. Notice

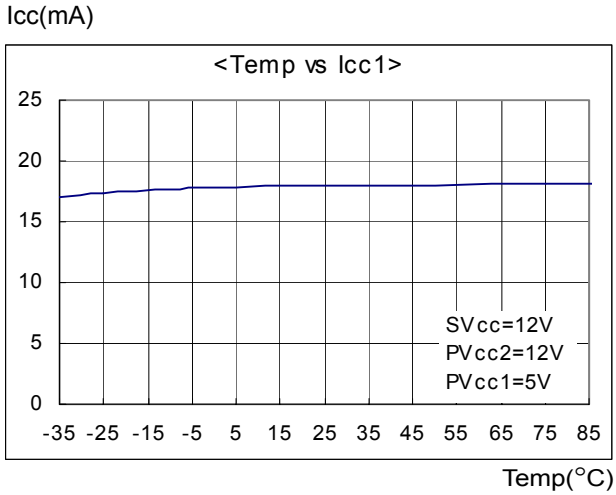
- When REF1(pin1) or REF2(pin25) is lower than 0.7V, BTL output is off.
- Under Voltage Protecton Function. (If SVcc is lower than 3.8V, Chip is disable. Hysterisis is 0.2V)
- Mute on BTL output voltage is as followed:
  - Mute ON BTL Output (CH1,2) = (PVcc1) / 2
  - Mute ON BTL Output (CH3,4) = ((PVcc2-0.6) / 2

Each output to output and output to GND short should be kept away.

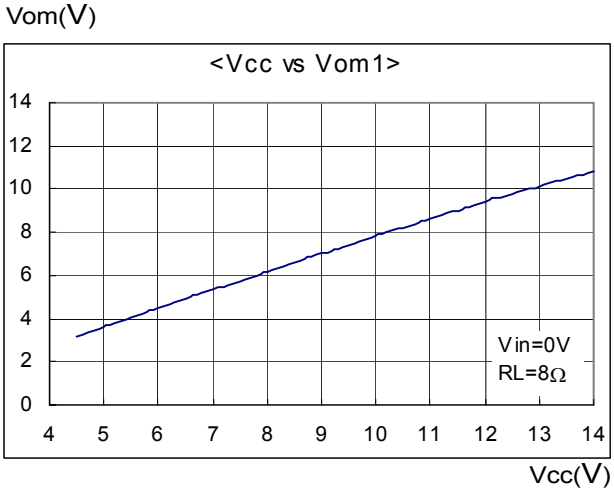
Typical performance characteristics

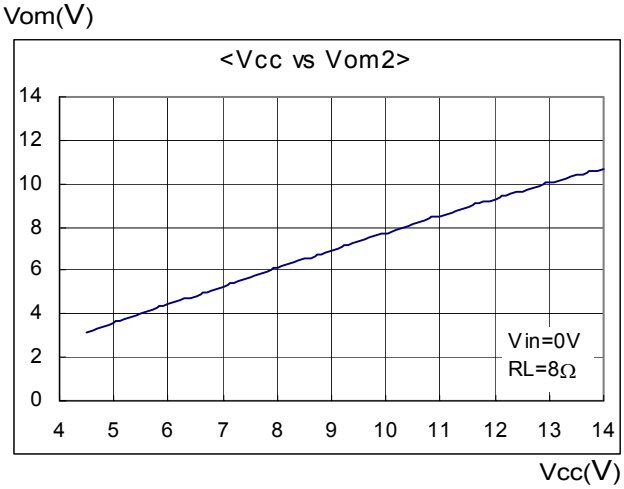
Total circuit

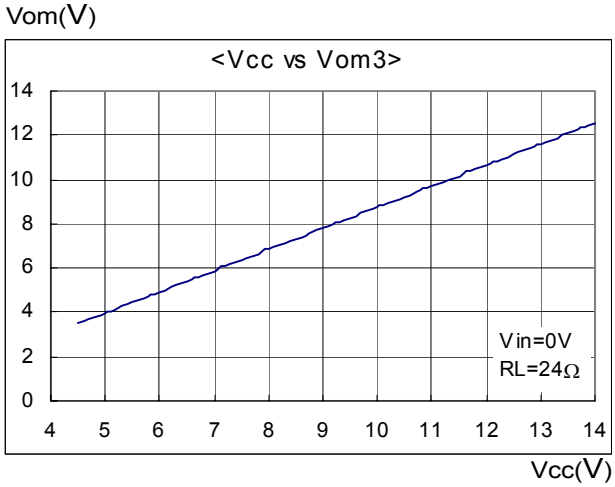


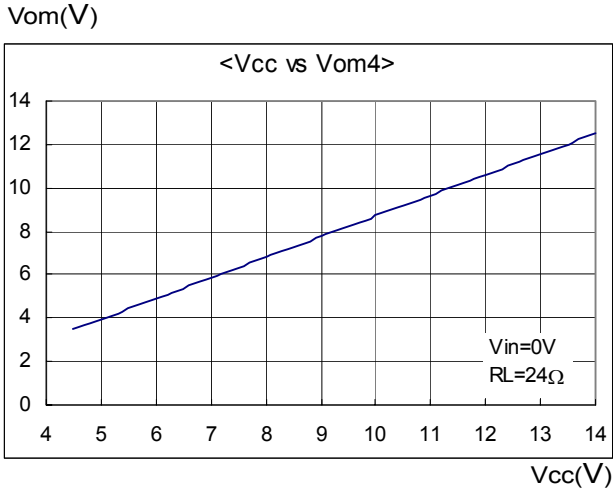


BTL Drive part

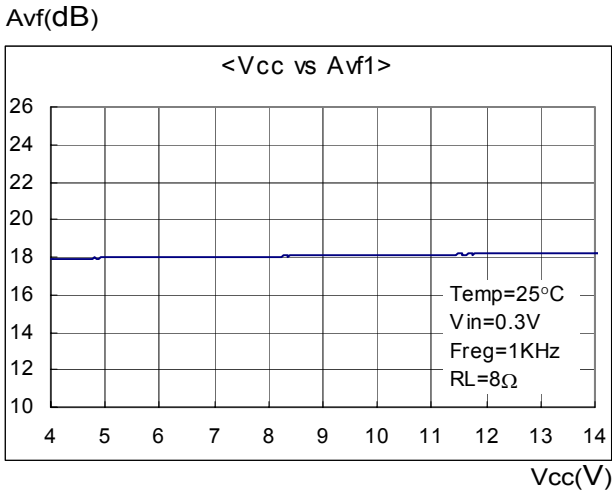


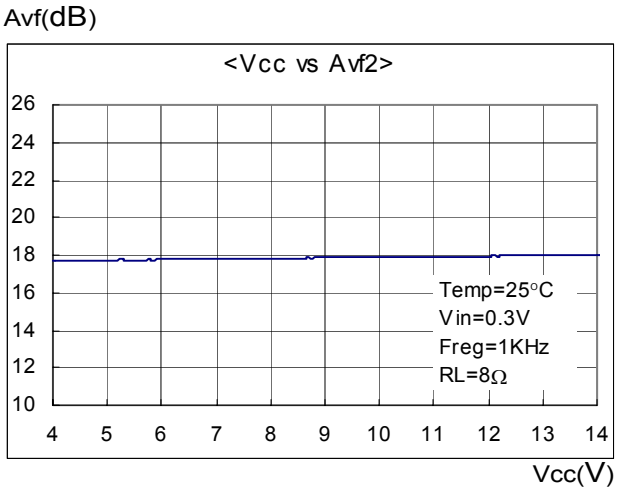


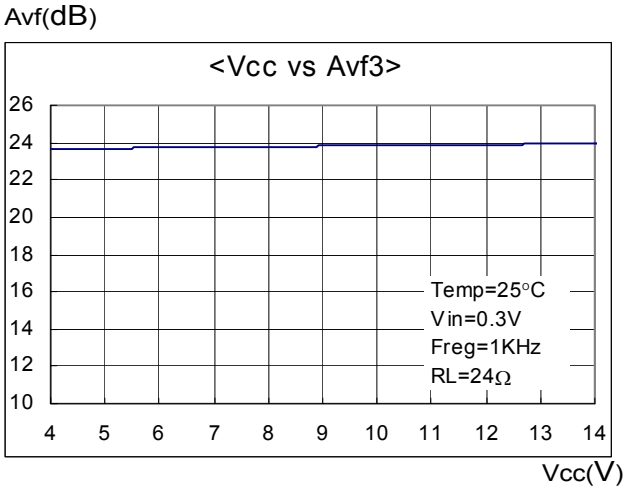


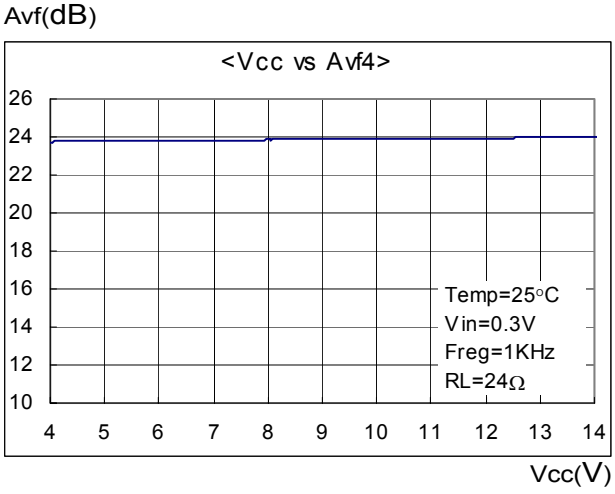


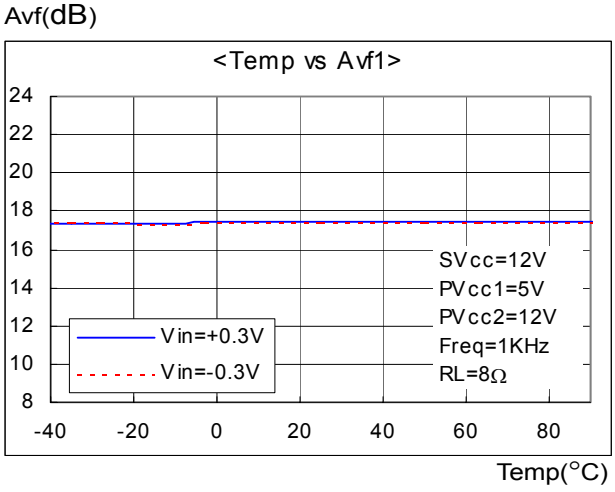
Typical performance characteristics (Continued)

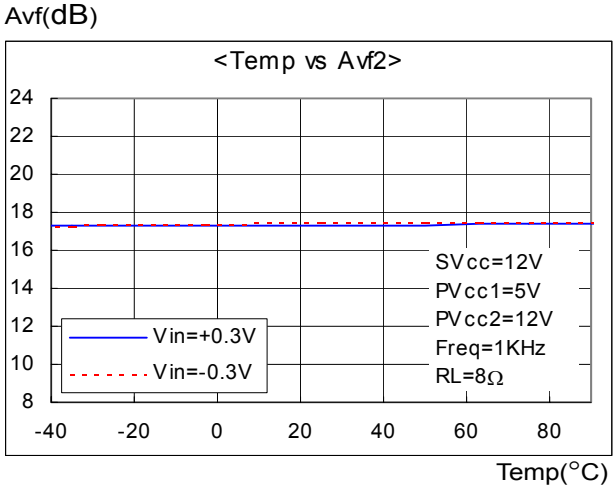












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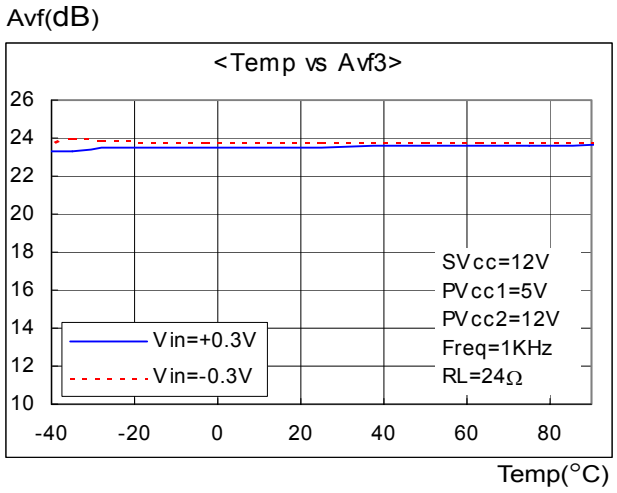
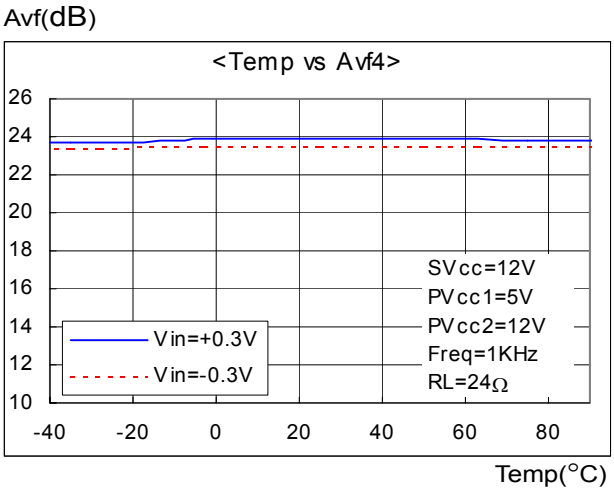
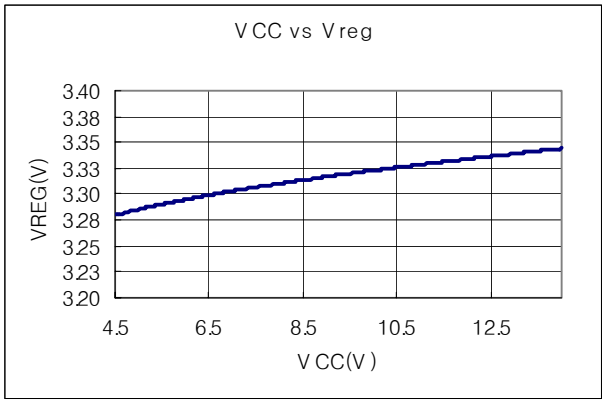
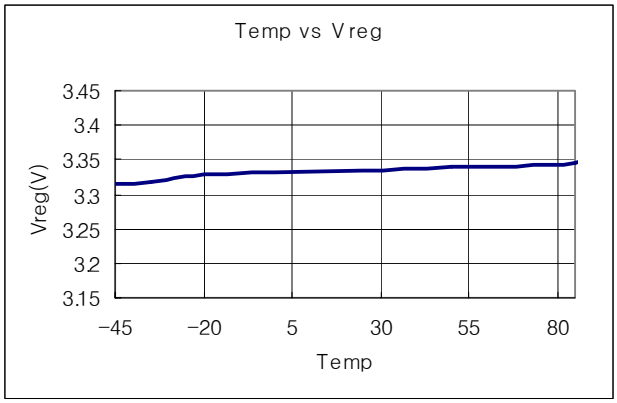


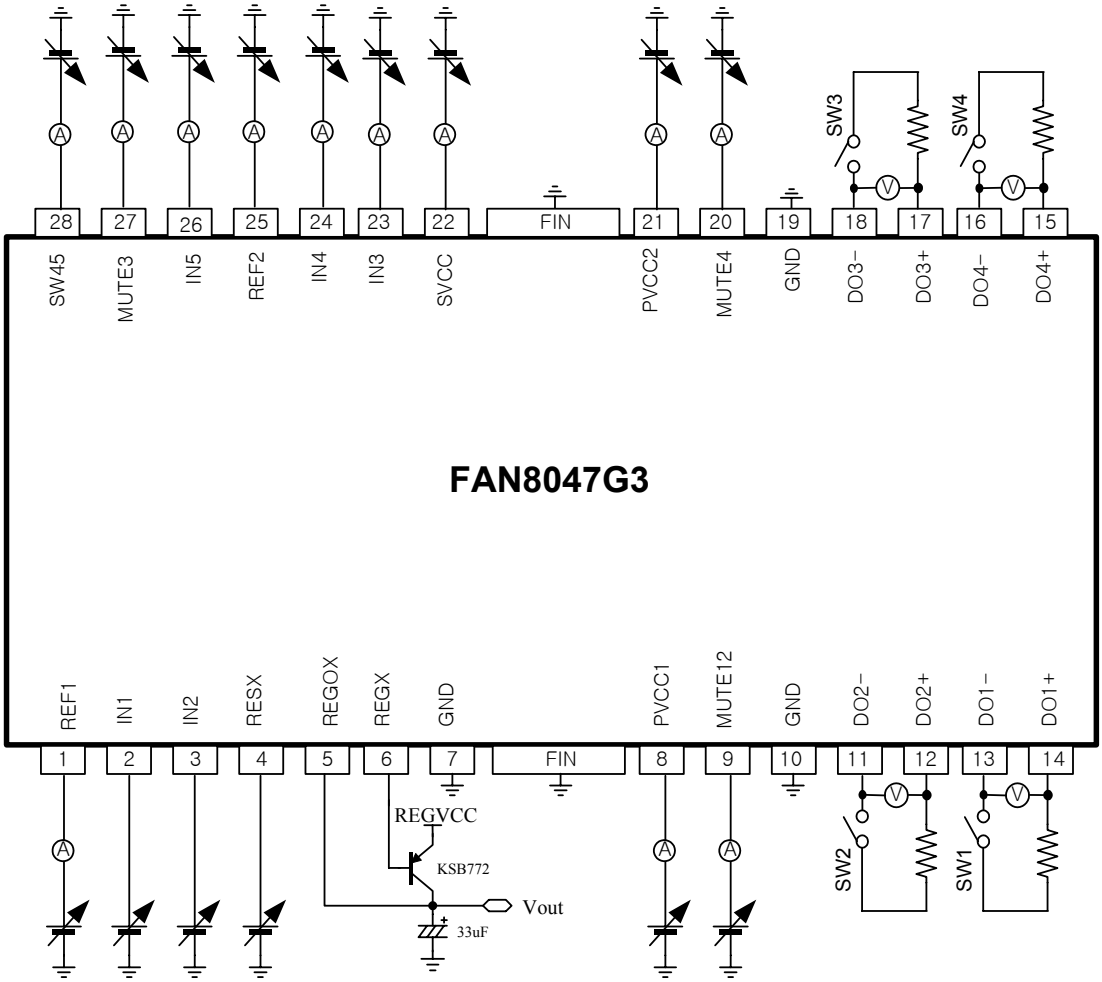


Regulator part

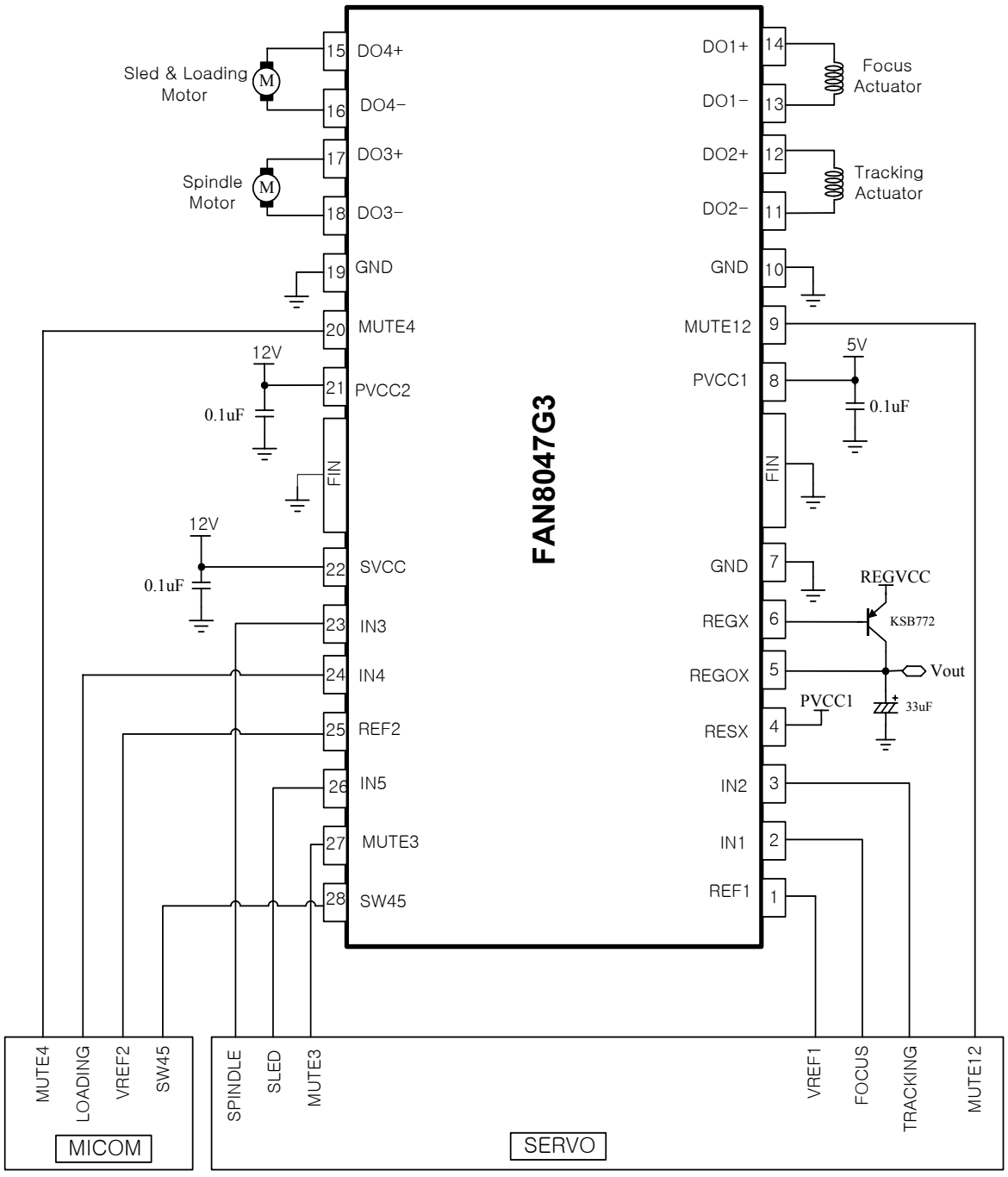




Test circuits

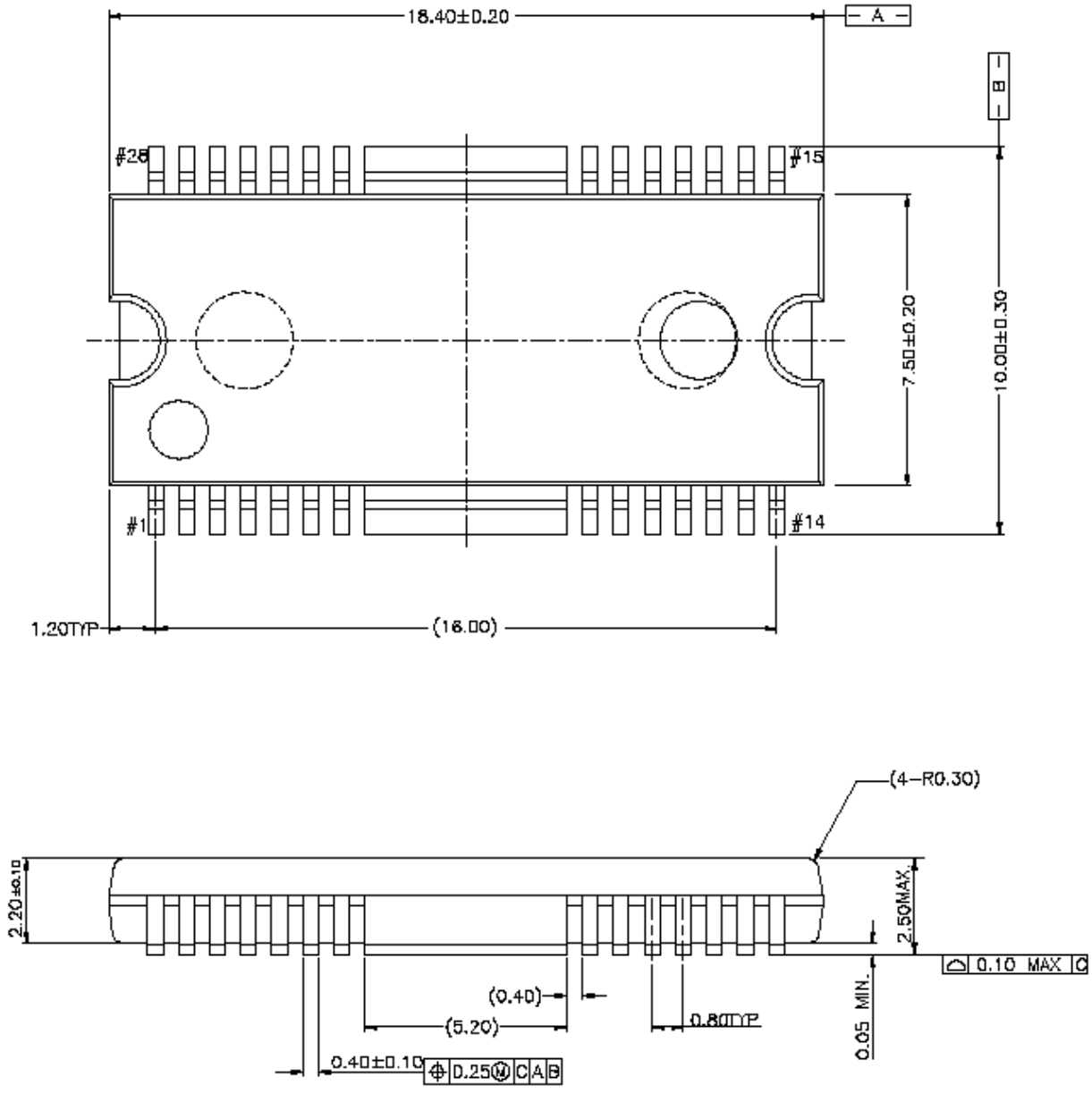


Typical application circuit



Package dimension

28-SSOPH-375-SG2



Unit : mm