



## KHTEK DA1196 - Digital to Audio Converter

### *24Bit, 192KHz, 6-Channel*

## General Description

DA1196 is a digital to analog converter especially designed to work with MPEG2/AC-3 decoded data in applications such as, DVD player, home theater, set-top box, and digital TV, etc. DA1196 integrates 6 DA channels providing customers a solution of both simplicity and excellent performance.

## Features

### High Resolution:

- 16/18/20/24/32 Bit Selectable

### High Performance:

Sampling Rate: 8KHz ~ 192KHz

THD+N: -98 dB

Dynamic Range: 104dB

S/N Ratio: 104dB

Channel Separation: 107dB

### High Integration:

- 6 Audio Channels, each contains:
  - Oversampling Digital Filter
  - High-Resolution Delta Sigma DAC
  - Analog Low Pass Filter
  - Output Amplifier

### High Versatility

- Control via 3-Wire Interface or Hardware Pins
- Left/Right-justified or IIS Format Selectable
- Selectable De-emphasis Sampling Rate:
  - 32KHz, 44.1KHz, 48KHz
- Selectable Multiple Functions:
  - Soft Mute
  - Attenuation
  - De-emphasis
  - Zero Detection On/Off Control
- Selectable Output Operation Mode:
  - Left, Right, Stereo, Mono, or Mute

### 28 Pin SSOP Package

## Pin Configuration

|    |        |        |    |
|----|--------|--------|----|
| 1  | VDD    | VCC1   | 28 |
| 2  | SCKI   | VOU1R1 | 27 |
| 3  | BCKIN  | AGND   | 26 |
| 4  | SRCIN  | VOU1L1 | 25 |
| 5  | DIN1   | AGND1  | 24 |
| 6  | DIN2   | VOU2R2 | 23 |
| 7  | DIN3   | AGND   | 22 |
| 8  | MODE   | VOU2L2 | 21 |
| 9  | MUTE   | AGND2  | 20 |
| 10 | NC     | VOU3R3 | 19 |
| 11 | DGND   | AGND   | 18 |
| 12 | ML/I2S | VOU3L3 | 17 |
| 13 | MC/TWL | CAP    | 16 |
| 14 | MD     | VCC2   | 15 |

## Pin Assignments

| Pin | Name   | I/O | Description   |
|-----|--------|-----|---|
| 1   | VDD    | PWR | Digital Power Supply  |
| 2   | SCKI   | IN  | Crystal Oscillator Input or External Master/System Clock Input                                  |
| 3   | BCKIN  | IN  | Bit Clock Input for Audio Data  |
| 4   | SRCIN  | IN  | Sample Rate Clock Input   |
| 5   | DIN1   | IN  | Audio Data Input to DAC1  |
| 6   | DIN2   | IN  | Audio Data Input to DAC2  |
| 7   | DIN3   | IN  | Audio Data Input to DAC3  |
| 8   | MODE   | IN  | Mode Control, "0"= Software Mode; "1"= Hardware Mode.   |
| 9   | MUTE   | IN  | Mute Control, Active "High". To Mute, Pull this Pin High.                                       |
| 10  | NC     |     | Not Connected (Don't Care)  |
| 11  | DGND   | GND | Digital Ground  |
| 12  | ML/I2S | IN  | Latch for Serial Control in Software Mode or Input Format Selection in Hardware Mode.           |
| 13  | MC/IWL | IN  | Clock for Serial Control Data in Software Mode or Input Word Length Selection in Hardware Mode. |
| 14  | MD     | IN  | Serial Control Data in Software Mode.   |
| 15  | VCC2   | PWR | Analog Power  |
| 16  | CAP    | -   | Analog Common Mode Pin  |
| 17  | VOU3L3 | OUT | L-Channel Output from DAC3  |
| 18  | AGND   | GND | Analog Ground   |
| 19  | VOU3R3 | OUT | R-Channel Output from DAC3  |
| 20  | AGND2  | GND | Analog Ground   |
| 21  | VOU2L2 | OUT | L-Channel Output from DAC2  |
| 22  | AGND   | GND | Analog Ground   |
| 23  | VOU2R2 | OUT | R-Channel Output from DAC2  |
| 24  | AGND1  | GND | Analog Ground   |
| 25  | VOU1L1 | OUT | L-Channel Output from DAC1  |
| 26  | AGND   | GND | Analog Ground   |
| 27  | VOU1R1 | OUT | R-Channel Output from DAC1  |
| 28  | VCC1   | PWR | Analog Power  |

Note:

- All digital input pins have Schmitt triggers and internal pull-up resistors except the SCKI pin and MUTE pin, which have internal pull-down resistors.
- Logic high is denoted as either "H" or "1"; logic low is denoted as either "L" or "0" in this document.

## Absolute Maximum Rating

|                             |                       |
|-----------------------------|-----------------------|
| Power Supply Voltage        | + 6.5V                |
| +VCC to VDD Difference      | +/- 0.1V              |
| Input Logic Voltage         | -0.3V to (VDD + 0.3V) |
| Power Dissipation           | 600mW                 |
| Operating Temperature Range | -25 C to +85 C        |
| Storage Temperature         | -55 C to +125 C       |



### ESD Sensitive Device

Although DA1196 is furnished with KHTEK's proprietary ESD protection circuitry, proper ESD precaution is still recommended to avoid performance degradation or permanent damage.

## Package Information

| Model  | Package     | Package Drawing No. |
|--------|-------------|---------------------|
| DA1196 | 28 pin SSOP | 128 -SS             |

Package drawing is at the end of this data sheet

# Specifications

## Electrical Characteristics:

At 25 °C, VCC1=VCC2=VDD=5V/3.3V, fs=48kHz, 24Bit input data, System Clock = 384/256fs.

| Parameter                      | Conditions                 | Min   | Type                            | Max     | Unit             |
|--------------------------------|----------------------------|-------|---------------------------------|---------|------------------|
| Sampling Frequency             |                            | 8     | 48                              | 192     | KHz              |
| System Clock Frequency         | 128fs                      | 1.024 | 6.144                           | 24.5760 | MHz              |
|                                | 192fs                      | 1.536 | 9.216                           | 36.8640 | MHz              |
|                                | 256fs                      | 2.048 | 12.288                          | 49.1520 | MHz              |
|                                | 384fs                      | 3.072 | 18.432                          | 73.7280 | MHz              |
|                                | 512fs                      | 4.096 | 24.576                          |         | MHz              |
|                                | 768fs                      | 6.144 | 36.864                          |         | MHz              |
| Audio Data Format              | Selectable                 |       | Right/<br>Left/I <sup>2</sup> S |         |                  |
| Data Bit Length                | Selectable                 |       | 16/20/24/32                     |         | Bits             |
| <b>Power Supply</b>            |                            |       |                                 |         |                  |
| Voltage Range: VCC1, VCC2, VDD | VCC1=VCC2=VDD=5V           | 4.5   | 5                               | 5.5     | V                |
|                                | VCC1=VCC2=VDD=3.3V         | 3.0   | 3.3                             | 3.7     | V                |
| @fs=44.1KHz                    |                            |       |                                 |         |                  |
| Supply Current: ICC1+ICC2+IDD  | VCC1=VCC2=VDD=5V           |       | 68                              |         | mA               |
|                                | VCC1=VCC2=VDD=3.3V         |       | 43                              |         | mA               |
| Power Dissipation:             | VCC1=VCC2=VDD=5V           |       | 340                             |         | mW               |
|                                | VCC1=VCC2=VDD=3.3V         |       | 142                             |         | mW               |
| @fs=96KHz                      |                            |       |                                 |         |                  |
| Supply Current: ICC1+ICC2+IDD  | VCC1=VCC2=VDD=5V           |       | 75                              |         | mA               |
|                                | VCC1=VCC2=VDD=3.3V         |       | 48                              |         | mA               |
| Power Dissipation:             | VCC1=VCC2=VDD=5V           |       | 375                             |         | mW               |
|                                | VCC1=VCC2=VDD=3.3V         |       | 158                             |         | mW               |
| <b>Digital Input/Output</b>    |                            |       |                                 |         |                  |
| <b>Input Logic Level</b>       | VCC1=VCC2=VDD              |       |                                 |         |                  |
| V <sub>IH</sub>                | Pin2                       | 40%   |                                 |         | VDD              |
| V <sub>IL</sub>                |                            |       |                                 | 16%     | VDD              |
| V <sub>IH</sub>                | Pin 3,4,5,6,7,8,9,12,13,14 | 52%   |                                 |         | VDD              |
| V <sub>IL</sub>                | ---Schmitt Trigger         |       |                                 | 16%     | VDD              |
| <b>Output Logic Level</b>      | VCC1=VCC2=VDD              |       |                                 |         |                  |
| V <sub>OH</sub>                |                            | 90%   |                                 |         | VDD              |
| V <sub>OL</sub>                |                            |       |                                 | 10%     | VDD              |
| <b>DC Accuracy</b>             |                            |       |                                 |         |                  |
| Gain Error                     |                            |       | +/- 1                           | +/- 3   | %FSR             |
| Gain Mismatch Ch to Ch         |                            |       | +/- 1                           | +/- 2   | %FSR             |
| <b>Analog Output</b>           |                            |       | VCC, VDD                        |         |                  |
| Voltage Range                  | V <sub>out</sub> =0dB      |       | 5V                              | 3.3V    |                  |
|                                |                            |       | 1.0                             | 0.66    |                  |
|                                |                            |       | 2.5                             | 1.65    |                  |
| Center Voltage                 |                            |       |                                 |         | V <sub>rms</sub> |
| Load Impedance                 | AC Load                    | 10    |                                 |         | KOhm             |
| Frequency Response             |                            | 0     |                                 | 20      | KHz              |

**Electrical Characteristics:(Cont.)**

At 25 °C, VCC1=VCC2=VDD=5V/3.3V, fs=48kHz, 24Bit input data, System Clock = 384/256fs.

| Parameter                  | Conditions       | Min | Type |      | Max  | Unit |
|----------------------------|------------------|-----|------|------|------|------|
|                            |                  |     | VCC  | VDD  |      |      |
| <b>Dynamic Performance</b> |                  |     |      |      |      |      |
|                            |                  |     | 5V   | 3.3V |      |      |
| @fs=48KHz                  |                  |     |      |      |      |      |
| THD+N at FS(0dB)           | Fout=1kHz        |     | -98  | -97  | -100 | dB   |
| THD+N at -60dB             | Fout=1kHz        |     | -44  | -42  | -46  | dB   |
| Dynamic Range              | EIAJ, A-weighted | 100 | 104  | 102  | 106  | dB   |
| SNR                        | EIAJ, A-weighted | 100 | 104  | 102  | 106  | dB   |
| Channel Separation         | Fout=1kHz        | 105 | 107  | 105  | 110  | dB   |
| @fs=96KHz                  |                  |     |      |      |      |      |
| THD+N at FS(0dB)           | Fout=1kHz        |     | -98  | -97  | -100 | dB   |
| THD+N at -60dB             | Fout=1kHz        |     | -43  | -41  | -45  | dB   |
| Dynamic Range              | EIAJ, A-weighted | 98  | 103  | 101  | 105  | dB   |
| SNR                        | EIAJ, A-weighted | 98  | 103  | 101  | 105  | dB   |
| Channel Separation         | Fout=1kHz        | 103 | 105  | 103  | 108  | dB   |
| @fs=192KHz                 |                  |     |      |      |      |      |
| THD+N at FS(0dB)           | Fout=1kHz        |     | -97  | -96  | -100 | dB   |
| THD+N at -60dB             | Fout=1kHz        |     | -42  | -39  | -43  | dB   |
| Dynamic Range              | EIAJ, A-weighted | 98  | 102  | 99   | 103  | dB   |
| SNR                        | EIAJ, A-weighted | 98  | 102  | 99   | 103  | dB   |
| Channel Separation         | Fout=1kHz        | 100 | 102  | 100  | 105  | dB   |

**Timing Characteristics:**

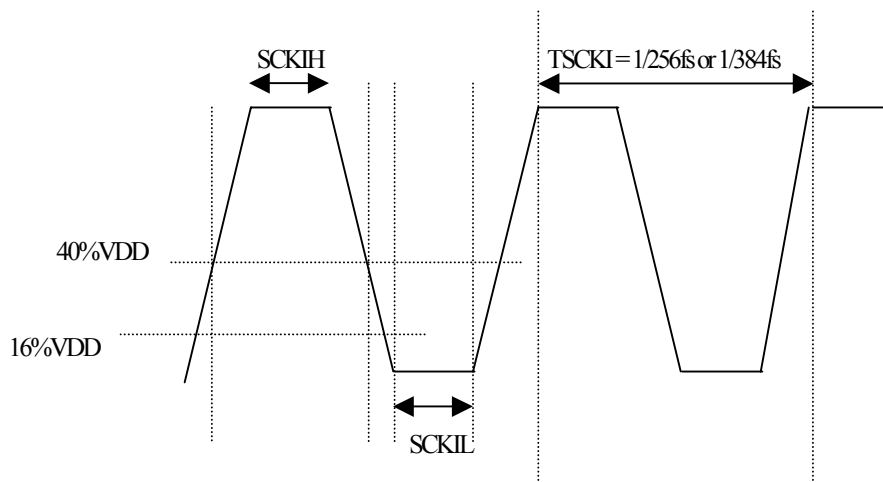
**SCKI/Master Clock Input Timing:**

**Timing Parameter**

| Parameter                  | Symbol | Value | Unit |
|----------------------------|--------|-------|------|
| <b>Master Clock Timing</b> |        |       |      |
| SCKI clock high level      | SCKIH  | >10   | ns   |
| SCKI clock low level       | SCKIL  | >10   | ns   |

At 25°C, VCC=VDD=5V/3.3V, fs=48kHz, 24Bit input data, System Clock = 384/256fs

**Timing Diagram**

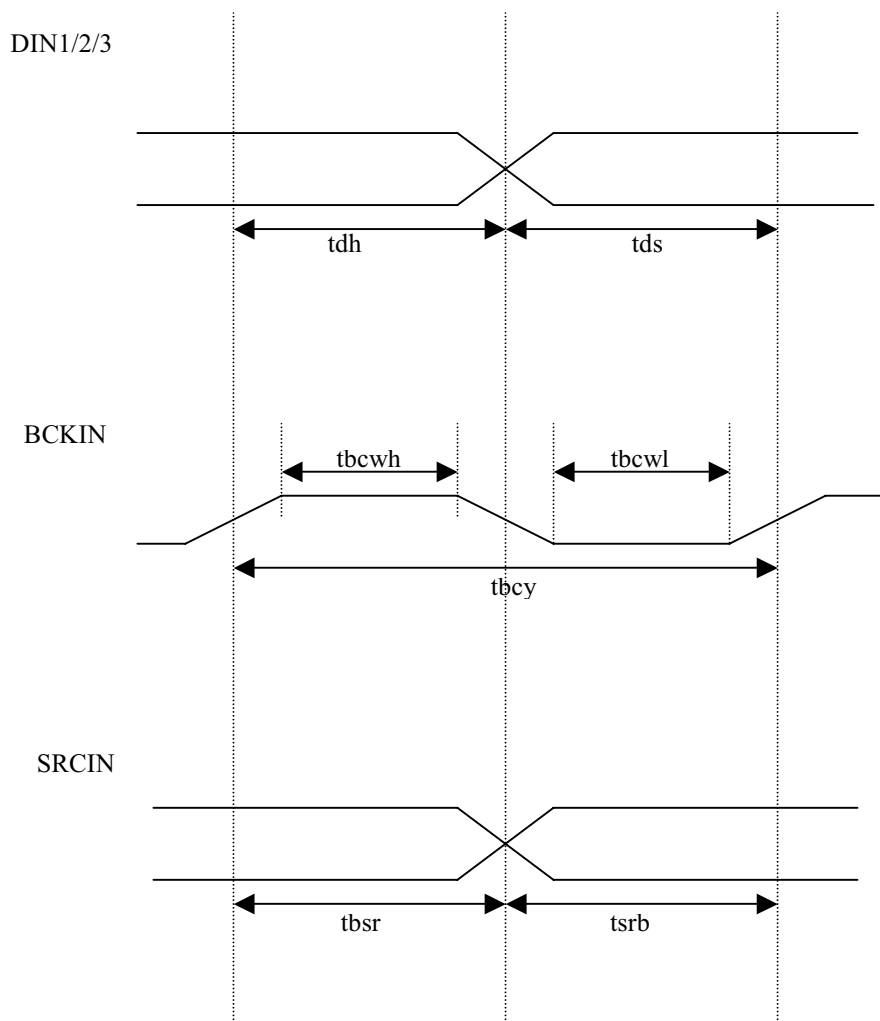


**Timing Parameter:**

| Parameter                   | Symbol       | Value | Unit |
|-----------------------------|--------------|-------|------|
| <b>Data Input Timing</b>    |              |       |      |
| DIN setup time              | tds          | >30   | ns   |
| DIN hold time               | tdh          | >30   | ns   |
| BCKIN high-level, low-level | tbcwh, tbcwl | >50   | ns   |
| BCKIN pulse cycle time      | tbcy         | >100  | ns   |
| BCKIN rising edge to SRCIN  | tbsr         | >30   | ns   |
| SRCIN to BCKIN rising edge  | tsrb         | >30   | ns   |

At 25°C, VCC=VDD=5V/3.3V, fs=48kHz, 24Bit input data, System Clock = 384/256fs

**Timing Diagram**



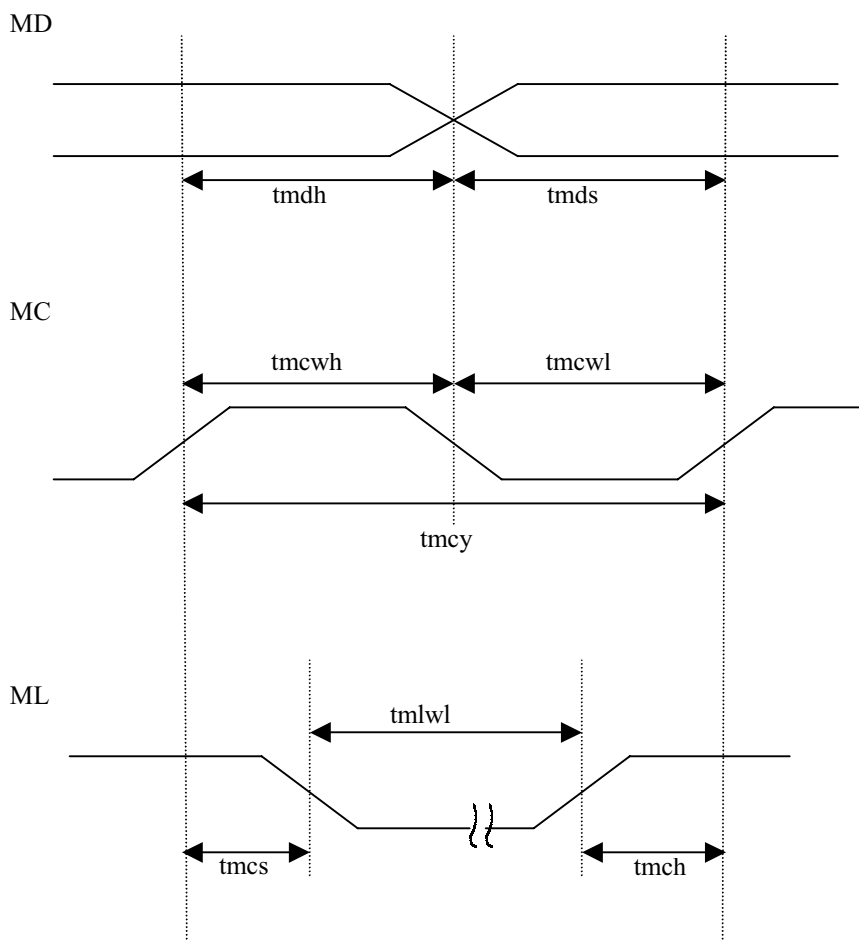
**3 Wire Serial Mode Control Timing:**

**Timing Parameter:**

| Parameter                           | Symbol       | Value    | Unit |
|-------------------------------------|--------------|----------|------|
| Serial Mode Control Timing          |              |          |      |
| MC pulse high-level, low-level      | tmcwh, tmcwl | >50      | ns   |
| MC pulse cycle time                 | tmcy         | >100     | ns   |
| MD setup time                       | tmds         | >30      | ns   |
| MD hold time                        | tmdh         | >30      | ns   |
| ML setup time                       | tmcs         | >30      | ns   |
| ML hold time                        | tmch         | >30      | ns   |
| ML pulsewidth high-level, low-level | tmlwh, tmlwl | >30+1/fs | ns   |

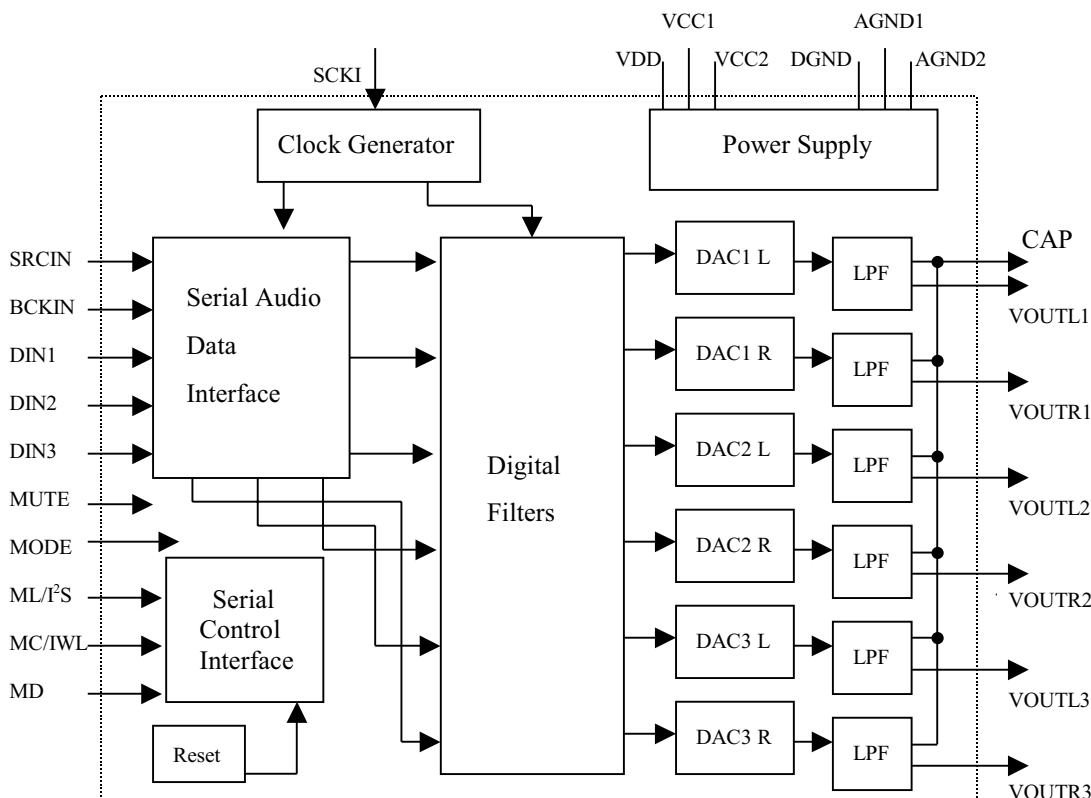
At 25°C, VCC=VDD=5V/3.3V, fs=48kHz, 24Bit input data, System Clock = 384/256fs

**Timing Diagram**



# Functional Description

## Functional Block Diagram



## System Clock

The system clock must be 128fs, 192fs, 256fs, 384fs, 512fs, or 768fs, where fs is the standard audio frequency including 32KHz, 44.1KHz, 48KHz, 96KHz, or 192KHz. The system clock can be input via SCKI (pin2) from an external clock and is used to operate the digital filter and delta sigma modulator. The system clock should be synchronized with SRCIN (pin4) – sampling rate clock. If the phase difference between them becomes greater than 6 bit BCKIN (pin3), the synchronization will be automatically performed and at this time the analog outputs are forced to VCC/2 by the chip.

**Table-1 System Clock and Sampling Rate**

| Sampling Rate<br>fs | System Clock Frequency (MHz) |         |                        |                        |                        |                        |
|---------------------|------------------------------|---------|------------------------|------------------------|------------------------|------------------------|
|                     | 128 fs                       | 192 fs  | 256fs                  | 384fs                  | 512fs                  | 768fs                  |
| 32KHz               | 4.0960                       | 6.1440  | 8.1920                 | 12.2880                | 16.3840 <sup>(1)</sup> | 24.5760 <sup>(1)</sup> |
| 44.1KHz             | 5.6448                       | 8.4670  | 11.2896                | 16.9340                | 22.5792 <sup>(1)</sup> | 33.8688 <sup>(1)</sup> |
| 48KHz               | 6.1440                       | 9.2160  | 12.2880                | 18.4320                | 24.5760 <sup>(1)</sup> | 36.8640 <sup>(1)</sup> |
| 96KHz               | 12.2880                      | 18.4320 | 24.5760                | 36.8640                | 49.1520 <sup>(1)</sup> | 73.7280 <sup>(1)</sup> |
| 192KHz              | 24.5760                      | 36.8640 | 49.1520 <sup>(1)</sup> | 73.7280 <sup>(1)</sup> | 98.3040 <sup>(2)</sup> | 147.456 <sup>(2)</sup> |

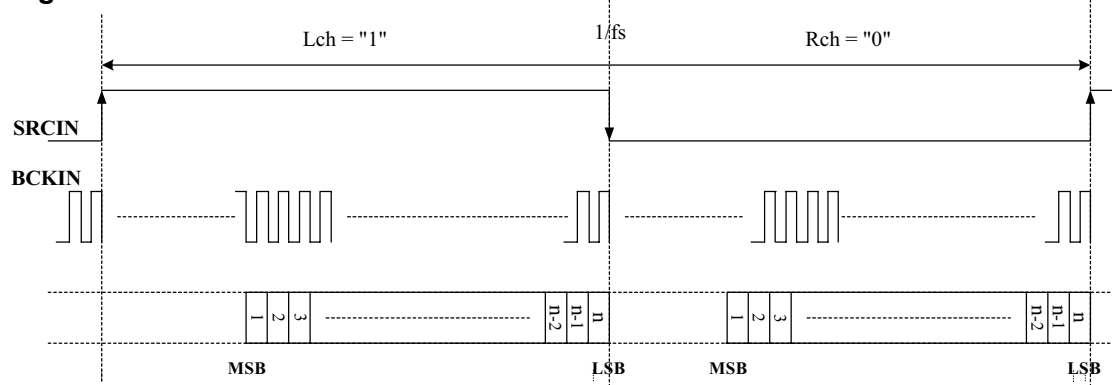
(1) For these sampling rate and system clock conditions, the SC1 bit of **Reg9** should be set to “0”; and the SC0 bit of **Reg9** should be set to “1”.

(2) For these sampling rate and system clock conditions, the SC1 bit of **Reg9** should be set to “1”; and the SC0 bit of **Reg9** should be set to “1”.

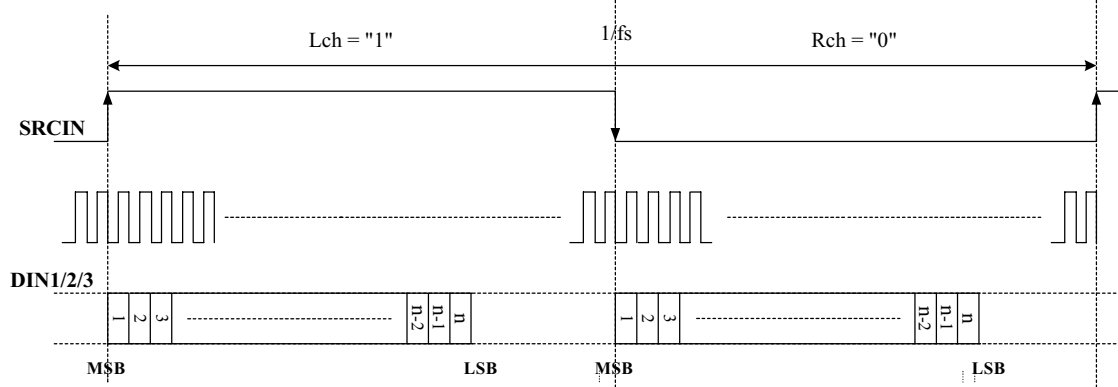
### Serial Digital Audio Data Input Interface

The digital audio information is applied to DA1196 via DIN1/2/3 (pin 5, 6, 7) for audio data input, via SRCIN (pin 4) for sampling rate clock, and via BCKIN (pin 3) for bit clock. The DA1196 supports right justified, left justified, and I<sup>2</sup>S data formats. All data formats are MSB first and two's complement. Both left justified format and I<sup>2</sup>S format support word length from 16 Bit to 32 Bit, but the right justified format supports word length only up to 24 Bit. The I<sup>2</sup>S data format, which is compatible with Philips serial data protocol, is left justified and one bit clock delay between SRCIN and data MSB. The relationship of the three audio input signals, DIN, SRCIN, and BCKIN is illustrated in the following figures for three formats:

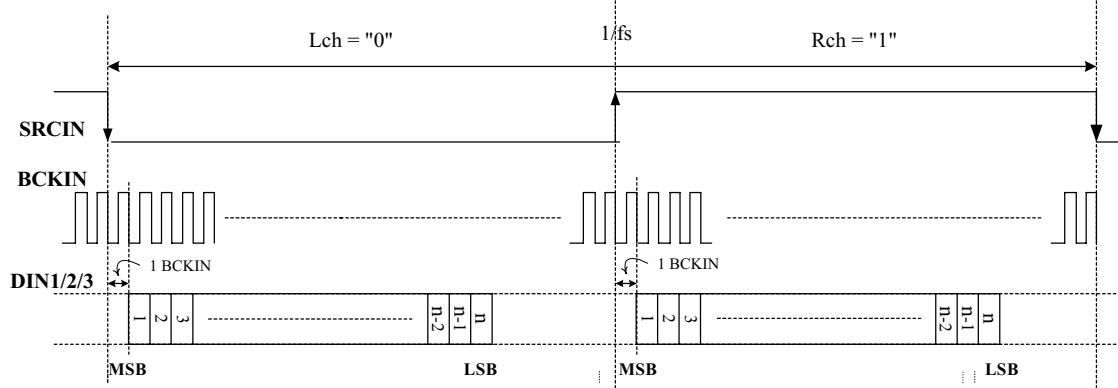
#### Right Justified Format



#### Left Justified Format



#### I<sup>2</sup>S Format



Note: 1. Logic high is denoted as either "H" or "1"; logic low is denoted as either "L" or "0" in this document.

2. With IIS format, the word length can go up to 32 Bit as long as the SRCIN period can accommodate.



## Multi-Functions & Mode Control

DA1196 can operate in two different control modes – serial (software) or parallel (hardware). Which mode to operate is selected by MODE pin (pin8) and is illustrated in following table:

**Table-2 Serial/Parallel Selection**

| MODE (pin8) | Selected Mode               | Selected Pins                      |
|-------------|-----------------------------|------------------------------------|
| Low         | Serial (or Software) Mode   | MD (pin14), MC (pin13), ML (pin12) |
| High        | Parallel (or Hardware) Mode | IWL (pin13), I2S (pin12)           |

### Hardware (Parallel) Mode Control, MODE="1"

When MODE pin (pin8) is set to "1", DA1196 is in hardware mode; the logic levels set on the hardware pins – pin9, pin12, pin13, and pin14 control a few functions implemented in the DA1196 for hardware mode.

A logic "0" on MUTE pin (pin 9) allows for a normal operation; but a logic "1" on MUTE pin (pin9) would force the outputs to be soft muted.

**Table-3 Selectable Mute Function**

| MUTE (pin 9) | Mute Function |
|--------------|---------------|
| 0            | OFF           |
| 1            | ON            |

I<sup>2</sup>S (pin12) and IWL (pin13) together can be used to obtain different input data format and word length. The proper settings are shown in the following table:

**Table-4 Selectable Input Data Formats**

| Input Data Format    | I <sup>2</sup> S (pin12) | IWL (pin13) |
|----------------------|--------------------------|-------------|
| Normal Format -16Bit | 0                        | 0           |
| Normal Format -20Bit | 0                        | 1           |
| Normal Format -24Bit | 1                        | 0           |
| I <sup>2</sup> S     | 1                        | 1           |

The De-emphasis function is not available in hardware mode. That is, in hardware mode the MD (pin14) becomes a NC pin and can be connected either to ground or power.

**Table-5 De-emphasis Function**

| MD (pin14) | De-emphasis |
|------------|-------------|
| 0          | OFF         |
| 1          | OFF         |

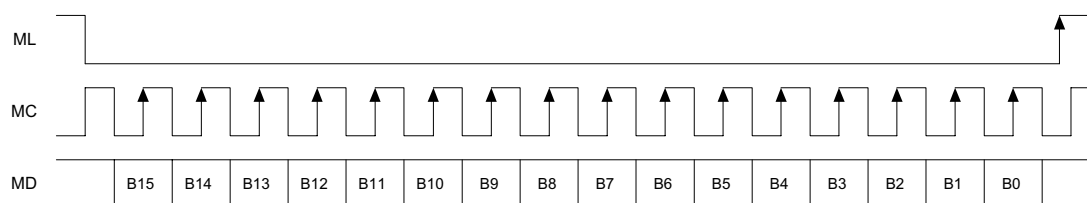
DA1196 provides several built-in functions in software (serial) mode, such as digital attenuation, de-emphasis, output control, and soft mute. Following **Table-6** shows the selectable functions and their default conditions:

**Table-6 Selectable Functions**

| Function                                   | Selections  | Default              |
|--|---|----------------------|
| Digital Audio Input Format Selection       | Right Justified, Left Justified, or I <sup>2</sup> S    | Right Justified      |
| Input Audio Data Word Length               | 16-bit, 20-bit, 24-bit, or 32-bit                       | 24bit                |
| BCKIN Polarity Selection                   | Sample on Rising Edge or Falling Edge                   | On Rising Edge       |
| Digital Attenuation for each channel       | 0dB ~ Mute  | 0dB                  |
| Master Digital Attenuation of all channels | 0dB ~ Mute  | 0dB                  |
| Soft Mute Control                          | ON or OFF   | OFF                  |
| De-emphasis Control                        | ON or OFF   | OFF                  |
| De-emphasis Sample Rate Selection          | OFF, 32KHz, 48kHz , or 44.1KHz                          | OFF                  |
| Modulator Over-sampling Selection          | 32X, 64X, or 128X                                       | 64X                  |
| Analog Output Control                      | L, R, Mono, Stereo, or Mute                             | Stereo               |
| Analog Output Reverse Control              | OUT1L/R, OUT2L/R, OUT3L/R, or OUT1R/L, OUT2R/L, OUT3R/L | OUTXL/R<br>X=1, 2, 3 |
| DAC Operation Control                      | Operate or Disabled                                     | Operated             |
| Infinite Zero Detection Control            | Enabled or Disabled                                     | Not Detected         |

These implemented functions are controlled via a 3-wire serial interface, namely, MD (pin14) is input pin for control data, MC (pin13) is input pin for control clock, and ML (pin12) is for control latch.

**Control Data Input**



The chip has ten 16-bit internal registers for programming and shown as below. In order to use all the built-in functions that DA1196 provides, the ten registers must be addressed via the three -wire interface using MD (pin 14), MC (pin 13), and ML (pin 12) ten separate times to set all desired register values.

**Ten Internal Registers**

| Reg | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8   | B7   | B6   | B5   | B4   | B3   | B2   | B1   | B0   |
|-----|-----|-----|-----|-----|-----|-----|----|------|------|------|------|------|------|------|------|------|
| 0   | Res | Res | Res | A3  | A2  | A1  | A0 | LDL1 | L1A7 | L1A6 | L1A5 | L1A4 | L1A3 | L1A2 | L1A1 | L1A0 |
| 1   | Res | Res | Res | A3  | A2  | A1  | A0 | LDR1 | R1A7 | R1A6 | R1A5 | R1A4 | R1A3 | R1A2 | R1A1 | R1A0 |
| 2   | Res | Res | Res | A3  | A2  | A1  | A0 | PL3  | PL2  | PL1  | PL0  | IZD  | ATC  | OPE  | DEM  | MUT  |
| 3   | Res | Res | Res | A3  | A2  | A1  | A0 | PRV2 | PRV1 | PRV0 | IW1  | IW0  | BCP  | Res  | FM1  | FM0  |
| 4   | Res | Res | Res | A3  | A2  | A1  | A0 | LDL2 | L2A7 | L2A6 | L2A5 | L2A4 | L2A3 | L2A2 | L2A1 | L2A0 |
| 5   | Res | Res | Res | A3  | A2  | A1  | A0 | LDR2 | R2A7 | R2A6 | R2A5 | R2A4 | R2A3 | R2A2 | R2A1 | R2A0 |
| 6   | Res | Res | Res | A3  | A2  | A1  | A0 | LDL3 | L3A7 | L3A6 | L3A5 | L3A4 | L3A3 | L3A2 | L3A1 | L3A0 |
| 7   | Res | Res | Res | A3  | A2  | A1  | A0 | LDR3 | R3A7 | R3A6 | R3A5 | R3A4 | R3A3 | R3A2 | R3A1 | R3A0 |
| 8   | Res | Res | Res | A3  | A2  | A1  | A0 | LDS  | SA7  | SA6  | SA5  | SA4  | SA3  | SA2  | SA1  | SA0  |
| 9   | Res | Res | Res | A3  | A2  | A1  | A0 | Res  | Res  | SC1  | SC0  | Res  | SF1  | SF0  | MC1  | MC0  |

Following Table-7 describes in detail the functions controlled by each register bit:

**Table-7 Register Mapping**

| Register name |                | Function   |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
|---------------|----------------|--|-----|---------------------|---------------------|-----|---------------------|---------------------|---|---|---|---|------|------|---|---|---|---|---|------|---|---|---|---|---|------|---|---|---|---|---------|------|---|---|---|---|------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------|---|---|---|---|---|------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------|---|---|---|---|---|------|---------|---|---|---|---|---|---------|---|---|---|---|---|---------|---|---|---|---|---------|---------|
| <b>Reg0</b>   |                | Attenuation Control of DAC1 Left Channel   |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg0</b> , set A3="0", A2="0", A1="0", A0="0".  |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B8</b>     | LDL1           | <u>DAC1 Left Channel Attenuation Data Load Control.</u><br>When LDL1="0", the attenuation data L1A7~L1A0 are loaded but do not affect the output level until LDL1="1". That is when LDL1="0", the left channel output level remains at the previous attenuation level; and when LDL1="1", the left channel output level becomes affected by L1A7~L1A0. Either LDL1 or LDR1 is set to "1", the L and R channel attenuation data become effective simultaneously.  |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B7~B0</b>  | L1A7~L1A0      | <u>DAC1 Left Channel Attenuation Data.</u><br>Attenuation level = $20 \cdot \log(L1A[7:0]/256)$ dB.  |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>Reg1</b>   |                | Attenuation Control of DAC1 Right Channel  |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg1</b> , set A3="0", A2="0", A1="0", A0="1".  |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B8</b>     | LDR1           | <u>DAC1 Right Channel Attenuation Data Load Control.</u><br>When LDR1="0", the attenuation data R1A7~R1A0 are loaded but do not affect the output level until LDR1="1". That is when LDR1="0", the right channel output level remains at the previous attenuation level; and when LDR1="1", the right channel output level becomes affected by R1A7~R1A0. Either LDL1 or LDR1 is set to "1", the L and R channel attenuation data become effective simultaneously.   |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B7~B0</b>  | R1A7~R1A0      | <u>DAC1 Right Channel Attenuation Data.</u><br>Attenuation level = $20 \cdot \log(R1A[7:0]/256)$ dB.   |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>Reg2</b>   |                | DAC Multi-function Control   |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg2</b> , set A3="0", A2="0", A1="1", A0="0".  |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B8~B5</b>  | PL3 ~ PL0      | <u>Analog Output Mode Selection.</u><br><table border="1"> <thead> <tr> <th>PL3</th> <th>PL2</th> <th>PL1</th> <th>PL0</th> <th>Lch (pin17, 21, 25)</th> <th>Rch (pin19, 23, 27)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Mute</td><td>Mute</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>L</td><td>Mute</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>R</td><td>Mute</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>(L+R)/2</td><td>Mute</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Mute</td><td>L</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>L</td><td>L</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>R</td><td>L</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>(L+R)/2</td><td>L</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Mute</td><td>R</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>L</td><td>R</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>R</td><td>R</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>(L+R)/2</td><td>R</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Mute</td><td>(L+R)/2</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>L</td><td>(L+R)/2</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>R</td><td>(L+R)/2</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>(L+R)/2</td><td>(L+R)/2</td></tr> </tbody> </table> | PL3 | PL2                 | PL1                 | PL0 | Lch (pin17, 21, 25) | Rch (pin19, 23, 27) | 0 | 0 | 0 | 0 | Mute | Mute | 0 | 0 | 0 | 1 | L | Mute | 0 | 0 | 1 | 0 | R | Mute | 0 | 0 | 1 | 1 | (L+R)/2 | Mute | 0 | 1 | 0 | 0 | Mute | L | 0 | 1 | 0 | 1 | L | L | 0 | 1 | 1 | 0 | R | L | 0 | 1 | 1 | 1 | (L+R)/2 | L | 1 | 0 | 0 | 0 | Mute | R | 1 | 0 | 0 | 1 | L | R | 1 | 0 | 1 | 0 | R | R | 1 | 0 | 1 | 1 | (L+R)/2 | R | 1 | 1 | 0 | 0 | Mute | (L+R)/2 | 1 | 1 | 0 | 1 | L | (L+R)/2 | 1 | 1 | 1 | 0 | R | (L+R)/2 | 1 | 1 | 1 | 1 | (L+R)/2 | (L+R)/2 |
| PL3           | PL2            | PL1  | PL0 | Lch (pin17, 21, 25) | Rch (pin19, 23, 27) |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 0             | 0              | 0  | 0   | Mute                | Mute                |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 0             | 0              | 0  | 1   | L                   | Mute                |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 0             | 0              | 1  | 0   | R                   | Mute                |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 0             | 0              | 1  | 1   | (L+R)/2             | Mute                |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 0             | 1              | 0  | 0   | Mute                | L                   |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 0             | 1              | 0  | 1   | L                   | L                   |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 0             | 1              | 1  | 0   | R                   | L                   |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 0             | 1              | 1  | 1   | (L+R)/2             | L                   |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 1             | 0              | 0  | 0   | Mute                | R                   |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 1             | 0              | 0  | 1   | L                   | R                   |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 1             | 0              | 1  | 0   | R                   | R                   |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 1             | 0              | 1  | 1   | (L+R)/2             | R                   |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 1             | 1              | 0  | 0   | Mute                | (L+R)/2             |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 1             | 1              | 0  | 1   | L                   | (L+R)/2             |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 1             | 1              | 1  | 0   | R                   | (L+R)/2             |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| 1             | 1              | 1  | 1   | (L+R)/2             | (L+R)/2             |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B4</b>     | IZD            | <u>Internal Zero Detection Circuit Control.</u><br>IZD="1" function enabled; IZD="0" disabled.   |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |
| <b>B3</b>     | ATC            | <u>Attenuator Control.</u><br>When ATC="1", L1A[7:0] in <b>Reg0</b> , L2A[7:0] in <b>Reg4</b> , and L3A[7:0] in <b>Reg6</b> are used as a common attenuation data for both left and right channels in DAC1, DAC2, and DAC3 respectively; and R1A[7:0] in <b>Reg1</b> , R2A[7:0] in <b>Reg5</b> , R3A[7:0] in <b>Reg7</b> are ignored. When ATC="0", L1A[7:0] in <b>Reg0</b> , L2A[7:0] in <b>Reg4</b> , and L3A[7:0] in <b>Reg6</b> are used as the attenuation data for left channels of DAC1, DAC2, and DAC3; and R1A[7:0] in <b>Reg1</b> , R2A[7:0] in <b>Reg5</b> , and R3A[7:0] in <b>Reg7</b> are for right channels of DAC1, DAC2, and DAC3.  |     |                     |                     |     |                     |                     |   |   |   |   |      |      |   |   |   |   |   |      |   |   |   |   |   |      |   |   |   |   |         |      |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |   |   |   |   |   |      |         |   |   |   |   |   |         |   |   |   |   |   |         |   |   |   |   |         |         |

|               |                |  |        |                        |         |         |         |         |
|---------------|----------------|--|--------|------------------------|---------|---------|---------|---------|
| <b>B2</b>     | OPE            | <u>Left and Right DAC Operation Control</u><br>When OPE="0", the device is in normal operation; when OPE="1", outputs are forced to VCC/2 and all registers hold at the present states.  |        |                        |         |         |         |         |
| <b>B1</b>     | DEM            | <u>De-emphasis Control.</u><br>DEM="0", de-emphasis OFF; DEM="1", de-emphasis ON.  |        |                        |         |         |         |         |
| <b>B0</b>     | MUT            | <u>Left and Right Soft Mute.</u><br>MUT="0", Mute OFF; MUT="1", Mute ON.   |        |                        |         |         |         |         |
| <b>Reg3</b>   |                | DAC Interface Control  |        |                        |         |         |         |         |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg3</b> , set A3="0", A2="0", A1="1", A0="1".  |        |                        |         |         |         |         |
| <b>B8~B6</b>  | PRV2~PRV0      | <u>Analog Output Phase Control.</u>  |        |                        |         |         |         |         |
|               |                |  | DAC1 L | DAC1 R                 | DAC2 L  | DAC2 R  | DAC3 L  | DAC3 R  |
|               |                | PRV2   | 0      | -                      | -       | -       | -       | -       |
|               |                | PRV2   | 1      | -                      | -       | -       | Reverse | Reverse |
|               |                | PRV1   | 0      | -                      | -       | -       | -       | -       |
|               |                | PRV1   | 1      | -                      | -       | Reverse | Reverse | -       |
|               |                | PRV0   | 0      | -                      | -       | -       | -       | -       |
|               |                | PRV0   | 1      | Reverse                | Reverse | -       | -       | -       |
| <b>B5~B4</b>  | IW1,IW0        | <u>Input Word Length Selection.</u>  |        |                        |         |         |         |         |
|               |                | IW1  | IW0    | Input Word Length      |         |         |         |         |
|               |                | 0  | 0      | 16 bit                 |         |         |         |         |
|               |                | 0  | 1      | 20 bit                 |         |         |         |         |
|               |                | 1  | 0      | 24 bit                 |         |         |         |         |
|               |                | 1  | 1      | 32 bit                 |         |         |         |         |
| <b>B3</b>     | BCP            | <u>Bit Clock Polarity Selection</u><br>When BCP="0", audio input data is sampled on the rising edge of BCKIN; when BCP="1", audio input data is sampled on the falling edge of BCKIN.  |        |                        |         |         |         |         |
| <b>B2</b>     | Res            | Reserved and should be set to "0".   |        |                        |         |         |         |         |
| <b>B1~B0</b>  | FM1~FM0        | <u>Audio Data Format Selection.</u>  |        |                        |         |         |         |         |
|               |                | FM1  | FM0    | Audio Interface Format |         |         |         |         |
|               |                | 0  | 0      | Right justified        |         |         |         |         |
|               |                | 0  | 1      | Left justified         |         |         |         |         |
|               |                | 1  | 0      | I <sup>2</sup> S       |         |         |         |         |
|               |                | 1  | 1      | Reserved               |         |         |         |         |
| <b>Reg4</b>   |                | Attenuation Control of DAC2 Left Channel.  |        |                        |         |         |         |         |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg4</b> , set A3="0", A2="1", A1="0", A0="0".  |        |                        |         |         |         |         |
| <b>B8</b>     | LDL2           | <u>DAC2 Left Channel Attenuation Data Load Control.</u><br>When LDL2="0", the attenuation data L2A7~L2A0 are loaded but do not affect the output level until LDL2="1". That is when LDL2="0", the left channel output level remains at the previous attenuation level; and when LDL2="1", the left channel output level becomes affected by L2A7~L2A0. Either LDL2 or LDR2 is set to "1", the L and R channel attenuation data become effective simultaneously.    |        |                        |         |         |         |         |
| <b>B7~B0</b>  | L2A7~L2A0      | <u>DAC2 Left Channel Attenuation Data.</u><br>Attenuation level = 20*log (L2A[7:0]/256)dB.   |        |                        |         |         |         |         |
| <b>Reg5</b>   |                | Attenuation Control of DAC2 Right Channel.   |        |                        |         |         |         |         |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg5</b> , set A3="0", A2="1", A1="0", A0="1".  |        |                        |         |         |         |         |
| <b>B8</b>     | LDR2           | <u>DAC2 Right Channel Attenuation Data Load Control.</u><br>When LDR2="0", the attenuation data R2A7~R2A0 are loaded but do not affect the output level until LDR2="1". That is when LDR2="0", the right channel output level remains at the previous attenuation level; and when LDR2="1", the right channel output level becomes affected by R2A7~R2A0. Either LDL2 or LDR2 is set to "1", the L and R channel attenuation data become effective simultaneously. |        |                        |         |         |         |         |
| <b>B7~B0</b>  | R2A7~R2A0      | <u>DAC2 Right Channel Attenuation Data.</u><br>Attenuation level = 20*log (R2A[7:0]/256)dB.  |        |                        |         |         |         |         |
| <b>Reg6</b>   |                | Attenuation Control of DAC3 Left Channel.  |        |                        |         |         |         |         |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg6</b> , set A3="0", A2="1", A1="1", A0="0".  |        |                        |         |         |         |         |

|               |                |  |     |                              |
|---------------|----------------|--|-----|------------------------------|
| <b>B8</b>     | LDL3           | <u>DAC3 Left Channel Attenuation Data Load Control.</u><br>When LDL3="0", the attenuation data L3A7~L3A0 are loaded but do not affect the output level until LDL3="1". That is when LDL3="0", the left channel output level remains at the previous attenuation level; and when LDL3="1", the left channel output level becomes affected by L3A7~L3A0. Either LDL3 or LDR3 is set to "1", the L and R channel attenuation data become effective simultaneously.    |     |                              |
| <b>B7~B0</b>  | L3A7~L3A0      | <u>DAC3 Left Channel Attenuation Data.</u><br>Attenuation level = $20 \cdot \log(L3A[7:0]/256)$ dB.  |     |                              |
| <b>Reg7</b>   |                | Attenuation Control of DAC3 Right Channel.   |     |                              |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg7</b> , set A3="0", A2="1", A1="1", A0="1".  |     |                              |
| <b>B8</b>     | LDR3           | <u>DAC3 Right Channel Attenuation Data Load Control.</u><br>When LDR3="0", the attenuation data R3A7~R3A0 are loaded but do not affect the output level until LDR3="1". That is when LDR3="0", the right channel output level remains at the previous attenuation level; and when LDR3="1", the right channel output level becomes affected by R3A7~R3A0. Either LDL3 or LDR3 is set to "1", the L and R channel attenuation data become effective simultaneously. |     |                              |
| <b>B7~B0</b>  | R3A7~R3A0      | <u>DAC3 Right Channel Attenuation Data.</u><br>Attenuation level = $20 \cdot \log(R3A[7:0]/256)$ dB.   |     |                              |
| <b>Reg8</b>   |                | Simultaneous Attenuation Control for All Channels.   |     |                              |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg8</b> , set A3="1", A2="0", A1="0", A0="0".  |     |                              |
| <b>B8</b>     | LDS            | <u>Simultaneous Attenuation Data Load Control.</u><br>When LDS="0", the attenuation data are loaded but the output level of all channels remain at the previous attenuation level until LDS is set to "1". When LDS="1", all channels output levels become affected by SA7~SA0.  |     |                              |
| <b>B7~B0</b>  | SA7~SA0        | <u>Simultaneous Attenuation Data for All Channels.</u><br>Attenuation level = $20 \cdot \log(SA[7:0]/256)$ dB.   |     |                              |
| <b>Reg9</b>   |                | DAC Multi-function Control   |     |                              |
| <b>B12~B9</b> | A3, A2, A1, A0 | <u>Register Address.</u><br>To access <b>Reg9</b> , set A3="1", A2="0", A1="0", A0="1".  |     |                              |
| <b>B8</b>     | Res            | Reserved and should be set to "0".   |     |                              |
| <b>B6~B5</b>  | SC1 ~ SC0      | <u>System Clock Control.</u>   |     |                              |
|               |                | SC1  | SC0 | System Clock                 |
|               |                | 0  | 0   | SCKI ÷ 1                     |
|               |                | 0  | 1   | SCKI ÷ 2                     |
|               |                | 1  | 0   | SCKI ÷ 2                     |
|               |                | 1  | 1   | SCKI ÷ 4                     |
| <b>B3~B2</b>  | SF1 ~ SF0      | <u>De-emphasis Sampling Rate Selection.</u>  |     |                              |
|               |                | SF1  | SF0 | De-emphasis Sampling Rate    |
|               |                | 0  | 0   | Reserved                     |
|               |                | 0  | 1   | 32kHz group                  |
|               |                | 1  | 0   | 48kHz group                  |
|               |                | 1  | 1   | 44.1kHz group                |
| <b>B1~B0</b>  | MC1 ~ MC0      | <u>Modulator Over-sampling Control.</u>  |     |                              |
|               |                | MC1  | MC0 | Modulator Over-sampling Rate |
|               |                | 0  | 0   | 64X                          |
|               |                | 0  | 1   | 128X                         |
|               |                | 1  | 0   | 32X                          |
|               |                | 1  | 1   | Reserved                     |

## Power-On Reset

When power is first up, a reset function is automatically performed. Refer to the **Table-8** below for reset states of the ten registers. During the first 3,072 cycles of the system clock after reset, control data can be loaded to the ten registers and at the same time the output is forced to bipolar zero state. After 3,072 cycles of system clock, a “Low” to “High” at ML (pin12) will initiate programming.

**Table-8 Register Reset States**

| Register Name | State               |
|---------------|---------------------|
| <b>Reg0</b>   | 0000 0001 1111 1111 |
| <b>Reg1</b>   | 0000 0011 1111 1111 |
| <b>Reg2</b>   | 0000 0101 0010 0000 |
| <b>Reg3</b>   | 0000 0110 0010 0000 |
| <b>Reg4</b>   | 0000 1001 1111 1111 |
| <b>Reg5</b>   | 0000 1011 1111 1111 |
| <b>Reg6</b>   | 0000 1101 1111 1111 |
| <b>Reg7</b>   | 0000 1111 1111 1111 |
| <b>Reg8</b>   | 0001 0001 1111 1111 |
| <b>Reg9</b>   | 0001 0010 0000 0000 |

## Audio Input Format

The register bits, FM1 and FM0 of **Reg3** together determine the audio input data format as shown in the following table:

**Table-9 Audio Interface Format Control**

| FM1 | FM0 | Audio Input Format Selected |
|-----|-----|-----------------------------|
| 0   | 0   | Right justified             |
| 0   | 1   | Left justified              |
| 1   | 0   | I <sup>2</sup> S            |
| 1   | 1   | Reserved                    |

## Audio Input Word Length

The register bits, IW1 and IW0 of **Reg3** together determine the audio input data word length as shown in the following table:

**Table-10 Audio Input Word Length Control**

| IW1 | IW0 | Audio Input Word Length Selected |
|-----|-----|----------------------------------|
| 0   | 0   | 16 bit                           |
| 0   | 1   | 20 bit                           |
| 1   | 0   | 24 bit                           |
| 1   | 1   | 32 bit                           |

## Digital Volume Control

**Reg0** [L1A7: L1A0] and **Reg1** [R1A7: R1A0] control the left and right channel attenuation for DAC1.

**Reg4** [L2A7: L2A0] and **Reg5** [R2A7: R2A0] control the left and right channel attenuation for DAC2.

**Reg6** [L3A7: L3A0] and **Reg7** [R3A7: R3A0] control the left and right channel attenuation for DAC3.

**Reg8** [SA7: SA0] controls the attenuation for all channels. The attenuation level for DAC is equal to  $20 \cdot \log(\text{data}/256)$  dB. The attenuation level varies linearly with the register bit value.

## Power-On Reset

When power is first up, a reset function is automatically performed. Refer to the **Table-8** below for reset states of the ten registers. During the first 3,072 cycles of the system clock after reset, control data can be loaded to the ten registers and at the same time the output is forced to bipolar zero state. After 3,072 cycles of system clock, a “Low” to “High” at ML (pin12) will initiate programming.

**Table-8 Register Reset States**

| Register Name | State               |
|---------------|---------------------|
| <b>Reg0</b>   | 0000 0001 1111 1111 |
| <b>Reg1</b>   | 0000 0011 1111 1111 |
| <b>Reg2</b>   | 0000 0101 0010 0000 |
| <b>Reg3</b>   | 0000 0110 0010 0000 |
| <b>Reg4</b>   | 0000 1001 1111 1111 |
| <b>Reg5</b>   | 0000 1011 1111 1111 |
| <b>Reg6</b>   | 0000 1101 1111 1111 |
| <b>Reg7</b>   | 0000 1111 1111 1111 |
| <b>Reg8</b>   | 0001 0001 1111 1111 |
| <b>Reg9</b>   | 0001 0010 0000 0000 |

## Audio Input Format

The register bits, FM1 and FM0 of **Reg3** together determine the audio input data format as shown in the following table:

**Table-9 Audio Interface Format Control**

| FM1 | FM0 | Audio Input Format Selected |
|-----|-----|-----------------------------|
| 0   | 0   | Right justified             |
| 0   | 1   | Left justified              |
| 1   | 0   | I <sup>2</sup> S            |
| 1   | 1   | Reserved                    |

## Audio Input Word Length

The register bits, IW1 and IW0 of **Reg3** together determine the audio input data word length as shown in the following table:

**Table-10 Audio Input Word Length Control**

| IW1 | IW0 | Audio Input Word Length Selected |
|-----|-----|----------------------------------|
| 0   | 0   | 16 bit                           |
| 0   | 1   | 20 bit                           |
| 1   | 0   | 24 bit                           |
| 1   | 1   | 32 bit                           |

## Digital Volume Control

**Reg0** [L1A7: L1A0] and **Reg1** [R1A7: R1A0] control the left and right channel attenuation for DAC1.

**Reg4** [L2A7: L2A0] and **Reg5** [R2A7: R2A0] control the left and right channel attenuation for DAC2.

**Reg6** [L3A7: L3A0] and **Reg7** [R3A7: R3A0] control the left and right channel attenuation for DAC3.

**Reg8** [SA7: SA0] controls the attenuation for all channels. The attenuation level for DAC is equal to  $20 \cdot \log(\text{data}/256)$  dB. The attenuation level varies logarithmically with the register bit value.

**Table-11 Attenuation Level Control**

| Control Data | DAC Attenuation |
|--------------|-----------------|
| Ffh          | 0 dB            |
| Feh          | -0.068 dB       |
| -----        | -----           |
| 01h          | -48.16 dB       |
| 00h          | Mute            |

In addition setting the ATC bit of **Reg2** can control the outputs of left and right channel of DAC to be attenuated independently or simultaneously. Following Table-11 shows their setting.

**Table-12 Left/Right Attenuation Control**

| Register<br>Bit Name | Logic Value                    | 0 | 1   |
|----------------------|--------------------------------|---|---|
|                      | ATC<br>DAC Attenuation Control |   | Left Channel Controlled by AL[7:0]<br>Right Channel Controlled by AR[7:0] |

### Soft Mute Function

Soft mute function is implemented for all DAC channels in both hardware mode and software mode. It takes  $256/f_s$  seconds for DAC to soft mute its output; therefore the time needed to soft mute the DAC depends on the sampling rate used. The Digital Attenuation bits of **Reg0**, **Reg1**, and **Reg4 ~ Reg7** can be used to mute each DAC output independently.

**Table-13 Soft Mute Function Control**

| MUT | Soft Mute Function |
|-----|--------------------|
| 0   | OFF                |
| 1   | ON                 |

### Infinite Zero Detect Function

The zero detect feature is used to avoid noise caused by DC level input. The **Reg2** bit 2 (OPE) and **Reg2** bit 4 (IZD) controls the infinite zero detect function. When OPE = "1", the output of DAC is forced to bipolar zero, which is equivalent to output MUTE, regardless of any data inputs. When OPE = "0", the zero detect function is controlled by IZD. When OPE = "0", IZD = "1", the zero detect feature is enabled. At this time if the digital audio input data are continuously zero for 65,536 BCK cycles, the output will be forced to bipolar zero. If the input data are not zero, the DAC will convert the non-zero data. On the other hand the zero detect function can be disabled by setting OPE = "0", IZD = "0", and an external mute circuit can be implemented at user's choice.

### De-emphasis Function and De-emphasis Frequency Response Selection

The register bit DEM of **Reg2** decides if the de-emphasis function is enabled. **Table-14** shows the control of DEM bit:

**Table-14 De-emphasis Function Control**

| DEM | De-emphasis Function |
|-----|----------------------|
| 0   | OFF                  |
| 1   | ON                   |

The setting of register bit SF1 and SF0 of **Reg9** determines the sampling frequency for De-emphasis.

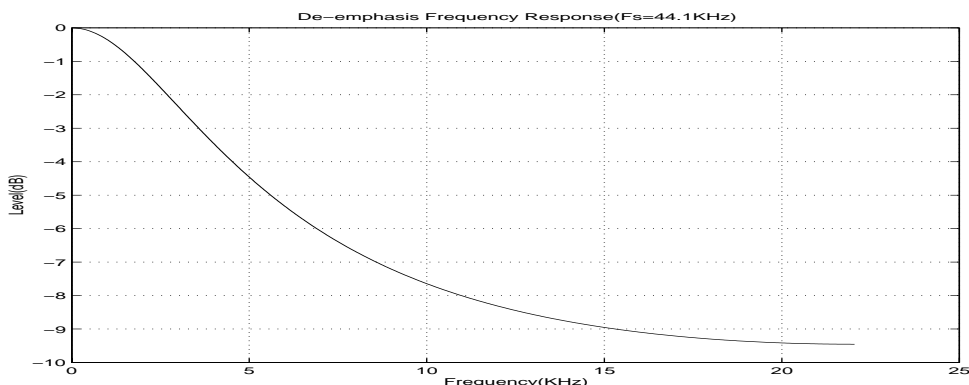
**Table-15** shows the bit setting combinations of SF1 and SF0 and their corresponding De-emphasis



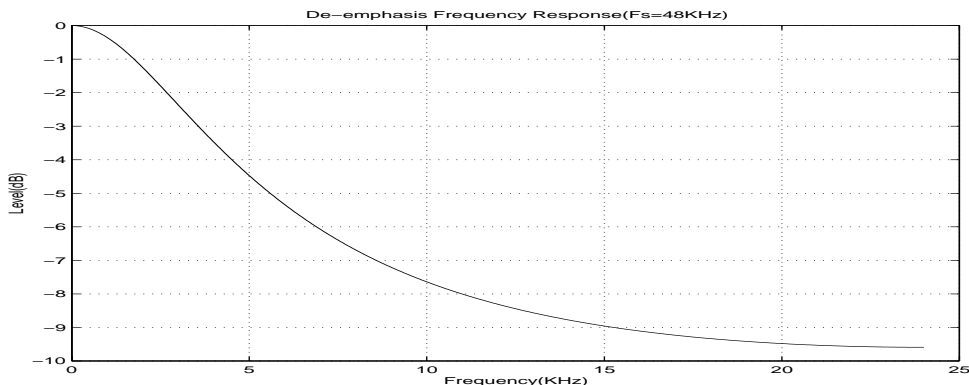
sampling frequencies. The resulted frequency response is also provided in the graphs below. To enable the de-emphasis function, the DEM is set to "1" and followed by the proper setting of the SF1 and SF0.

**Table-15 De-emphasis Sampling Frequency Control**

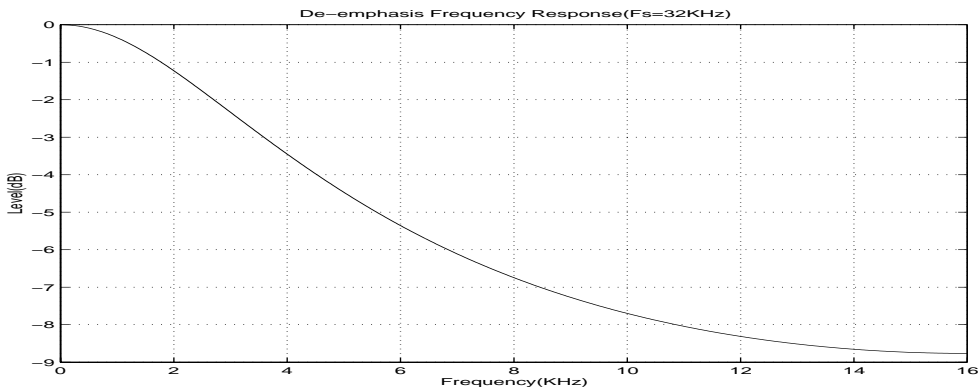
| SF1 | SF0 | De-emphasis Sampling Frequency |
|-----|-----|--------------------------------|
| 0   | 0   | OFF                            |
| 0   | 1   | 32 KHz                         |
| 1   | 0   | 48 KHz                         |
| 1   | 1   | 44.1KHZ                        |



De-emphasis at 44.1KHz Sampling Frequency



De-emphasis at 48KHz Sampling Frequency



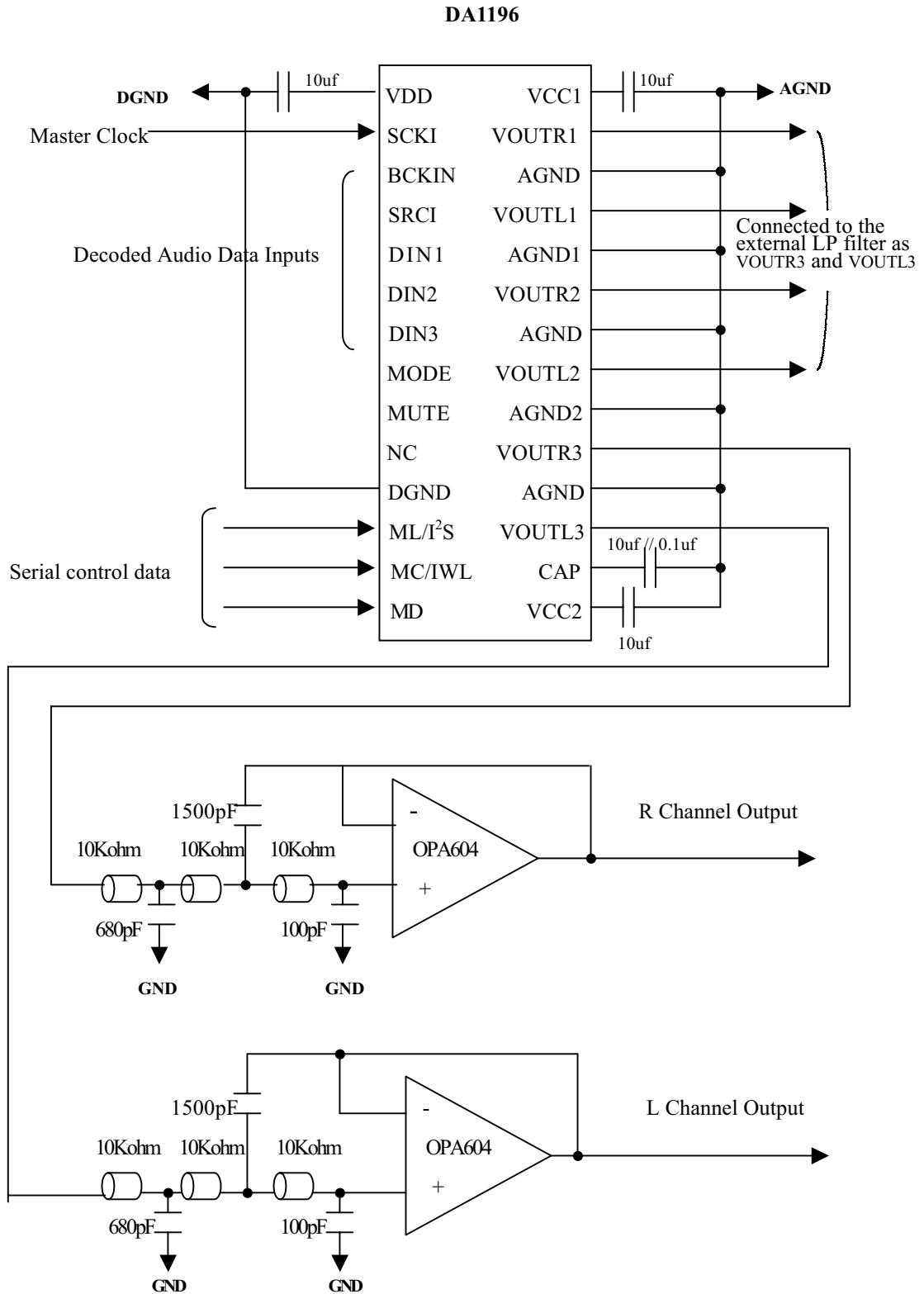
De-emphasis at 32KHz Sampling Frequency

**Modulator Over-sampling Control**

When the sampling rate SRCIN is below 16KHz, it is recommended to increase the over-sampling rate of modulator to 128X by setting the register bit MC1 of **Reg9** = "0" and register bit MC0 of **Reg9** = "1" to improve the dynamic performance of the DA converter.

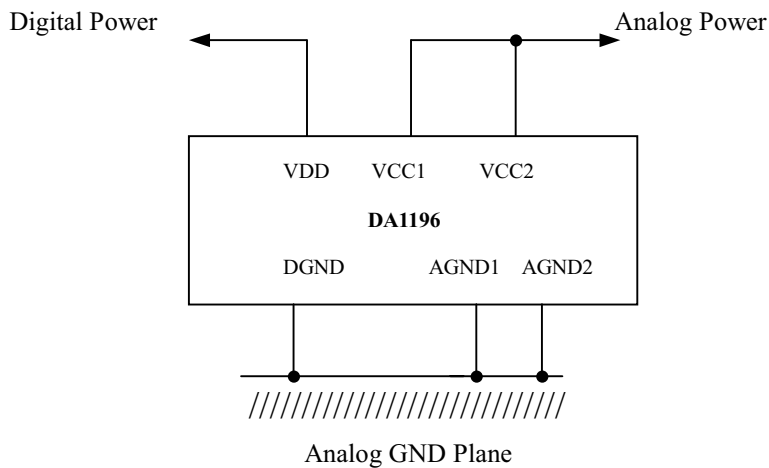
# Application Considerations

## Application Circuit



VCC1, VCC2, VDD all connected to 5V/3.3V analog power supply.

DA1196 has separate pins for two analog power supplies and digital power supply. It is recommended to connect the power pins together to the analog power supply and ground pins to the analog ground plane at locations near by the physical pins.



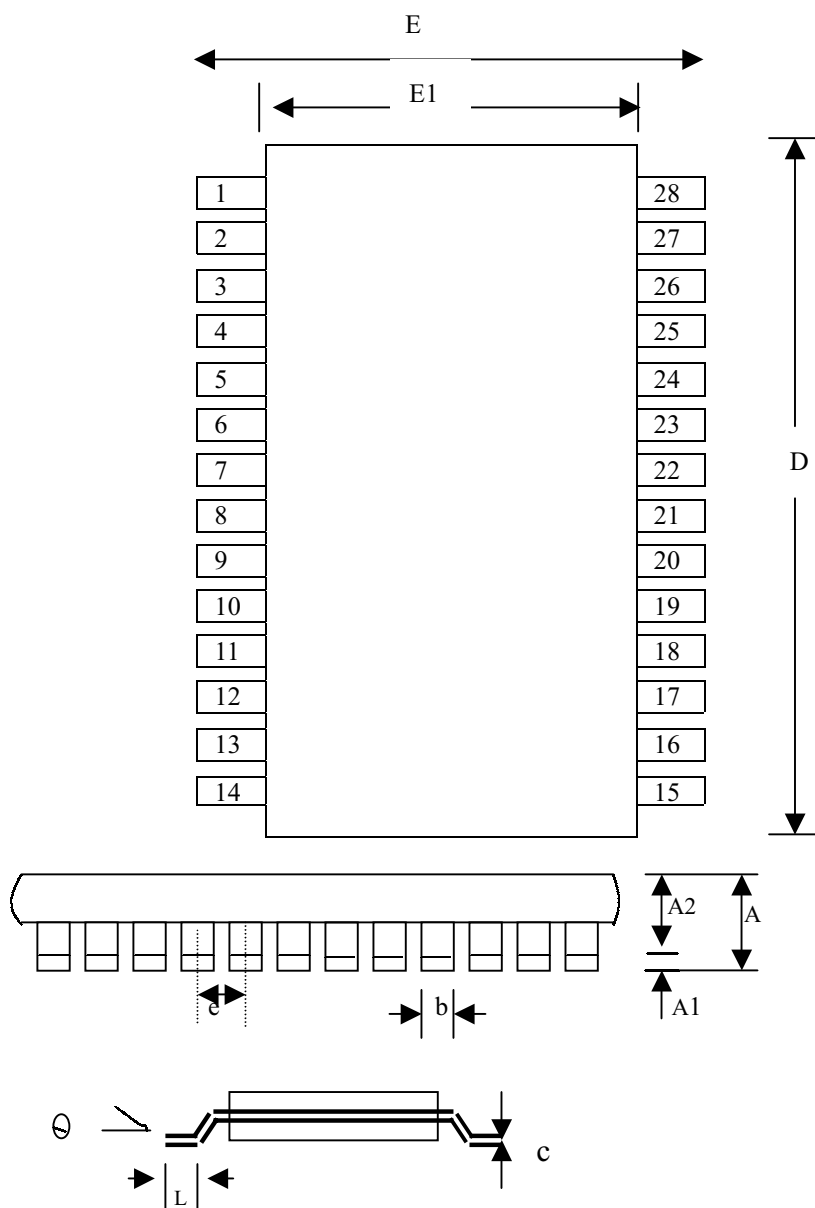
## Output Filtering

The internal low pass filter has 3dB bandwidth at 100kHz. To limit out of band noise, an external 3<sup>rd</sup> order filter as shown in the application circuit diagram is recommended, especially when the chip is to drive a wide band amplifier.

# Package Drawing No. 128-SS

|        |             |                     |
|--------|-------------|---------------------|
| Model  | Package     | Package Drawing No. |
| DA1196 | 28 pin SSOP | 128-SS              |

Package outline drawing is shown as below:



| Symbols  | Dimensions in millimeters |       |       | Dimensions in inches |        |        |
|----------|---------------------------|-------|-------|----------------------|--------|--------|
|          | Min                       | Nom   | Max   | Min                  | Nom    | Max    |
| A        | ----                      | ----  | 2.00  | ----                 | ----   | 0.079  |
| A1       | 0.05                      | ----  | ----  | 0.002                | ----   | ----   |
| A2       | ----                      | 1.75  | ----  | ----                 | 0.069  | ----   |
| b        | 0.22                      | 0.30  | 0.38  | 0.0086               | 0.012  | 0.015  |
| c        | 0.13                      | 0.15  | 0.20  | 0.0051               | 0.006  | 0.0079 |
| D        | 10.08                     | 10.20 | 10.34 | 0.397                | 0.402  | 0.407  |
| E        | 7.40                      | 7.80  | 8.20  | 0.291                | 0.307  | 0.323  |
| E1       | 5.00                      | 5.30  | 5.60  | 0.197                | 0.209  | 0.220  |
| e        | ----                      | 0.65  | ----  | ----                 | 0.0256 | ----   |
| L        | 0.56                      | 0.75  | 0.97  | 0.022                | 0.030  | 0.037  |
| $\theta$ | ----                      | 4°    | 8°    | ----                 | 4°     | 8°     |