SONY

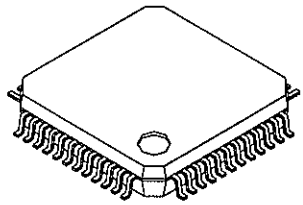
CXA1839Q

Y/Color Difference/RGB Controller for Color TV

Description

The CXA1839Q is a single chip bipolar IC which implements functions to carry out user control and various video parameter control for color TVs.

48 pin QFP (Plastic)



Features

- The built-in electronic volume and switches are controlled via the I²C bus, which allows various adjustments and user control.
- PICTURE, HUE, COLOR, BRIGHT and SHARPNESS adjustments are possible as user control.
- The IC allows adjustments of video parameters, such as detective axis setting, sharpness f0, PRE-OVER ratio, NR level, VM output level, DC transmission rate, CEC, dynamic picture and dynamic color.
- Built-in CEC (chrominance edge clear) circuit improves chroma transient.
- Built-in ABL, dynamic ABL and aging mode
- Two Y/color difference input blocks and two linear RGB input blocks
- High-speed I²C bus protocol.

Applications

TVs

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25℃, GND1 = 0V, GND2 = 0V)

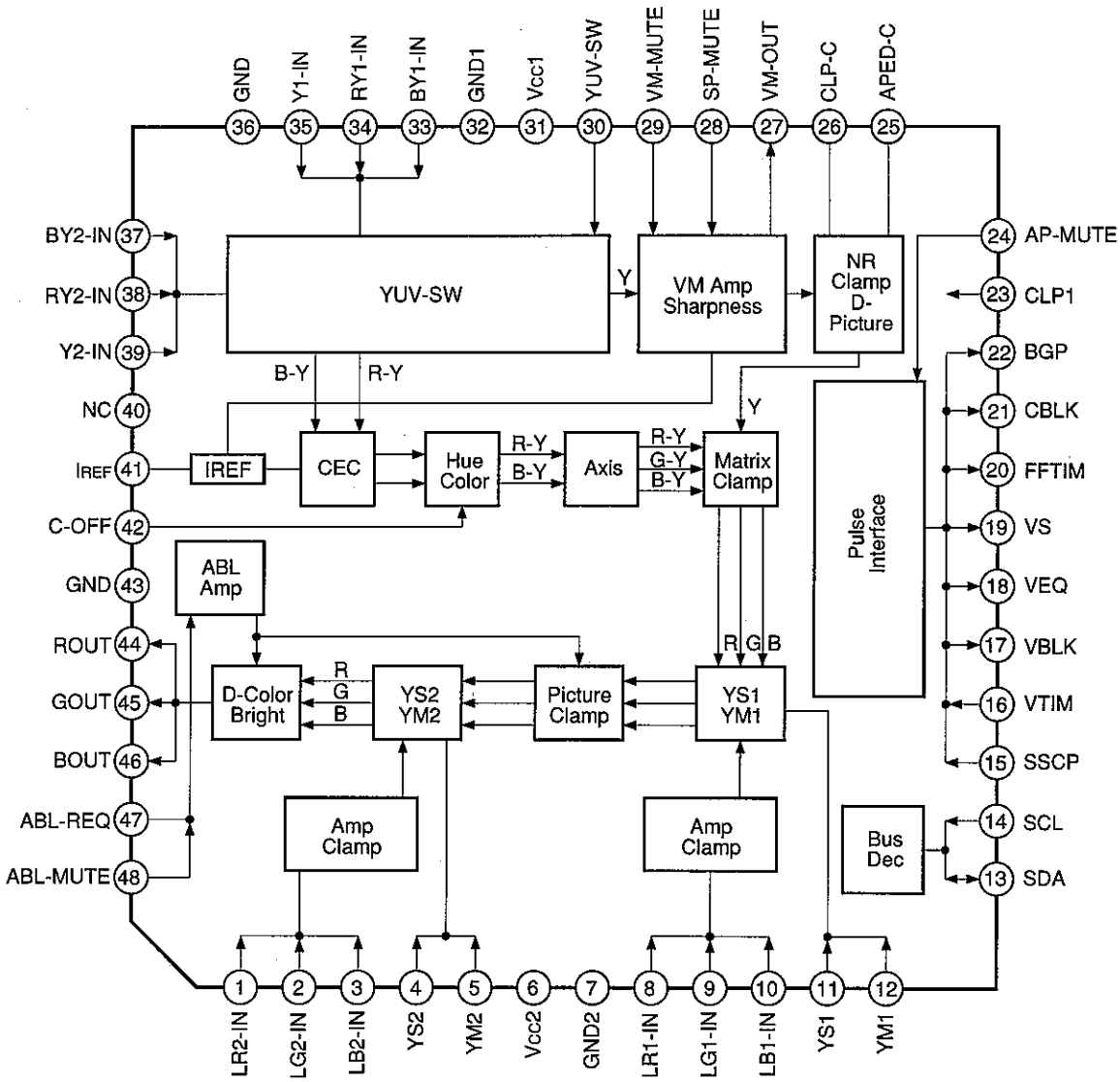
• Supply voltage	Vcc1, Vcc2	11	V
• Operating temperature		–20 to +75	℃
• Storage temperature		–65 to +150	℃
• Allowable power dissipation	P_D	750	mW
• Voltage at each pin			
	Pin 1 to Pin 5	–0.3 to Vcc +0.3	V
	Pin 8 to Pin 30	–0.3 to Vcc +0.3	V
	Pin 33 to Pin 35	–0.3 to Vcc +0.3	V
	Pin 37 to Pin 39	–0.3 to Vcc +0.3	V
	Pin 41 to Pin 47	–0.3 to Vcc +0.3	V

Operating Conditions

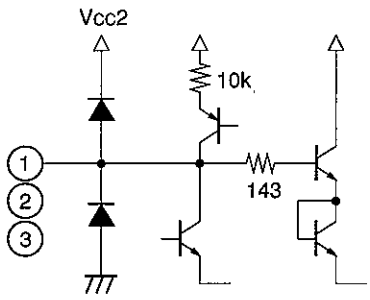
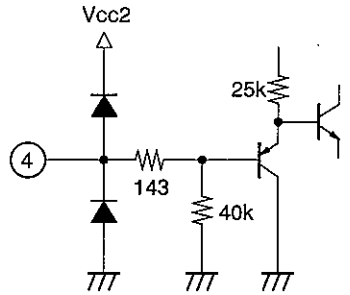
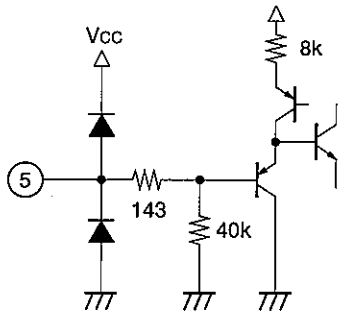
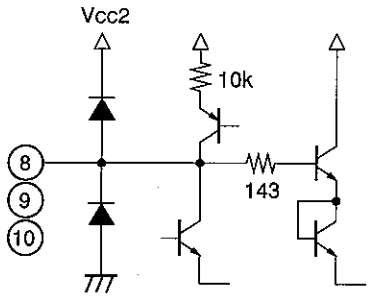
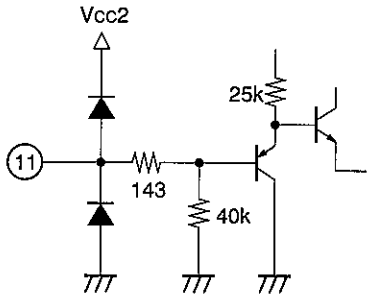
Supply voltage	Vcc1	9.0 ± 0.5	V
	Vcc2	9.0 ± 0.5	V

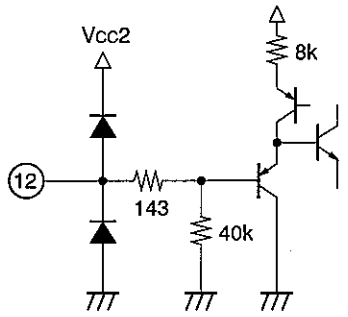
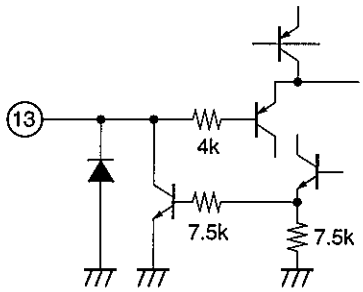
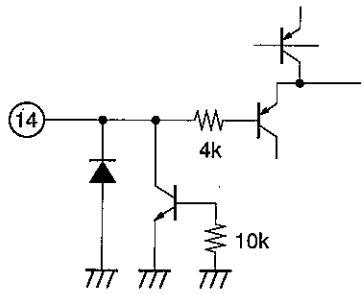
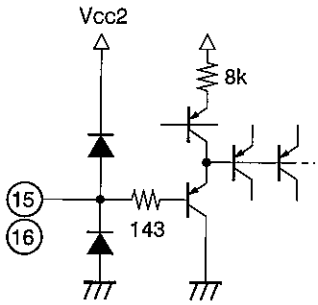
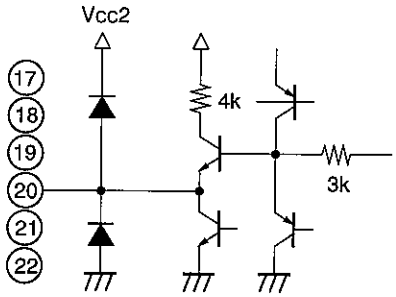
E95310B24

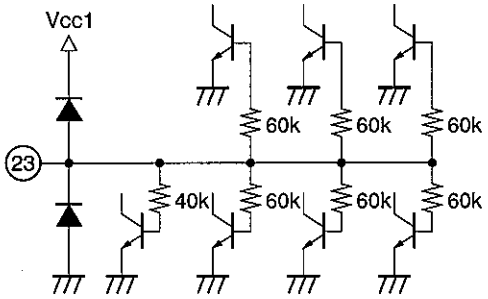
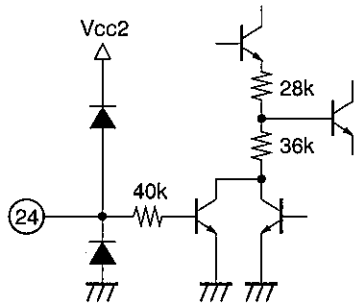
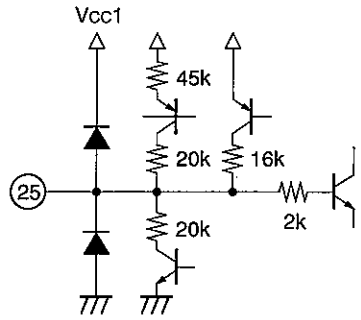
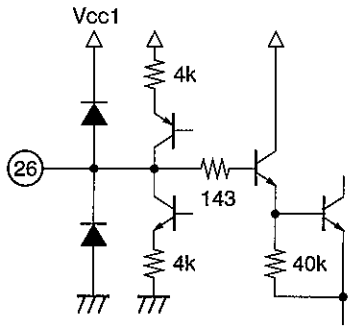
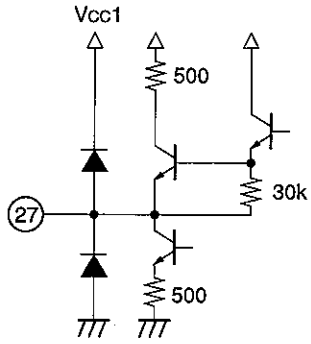
Block Diagram and Pin Configuration

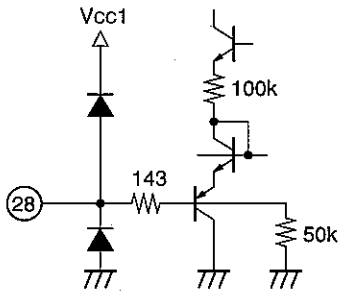
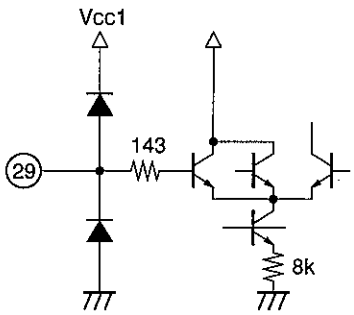
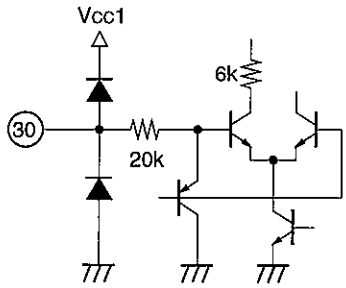
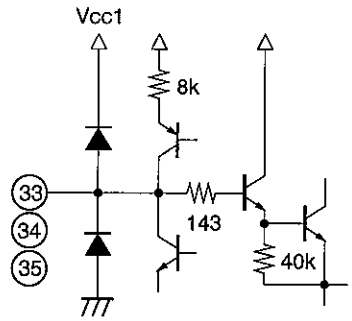
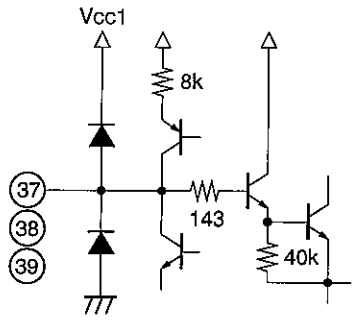


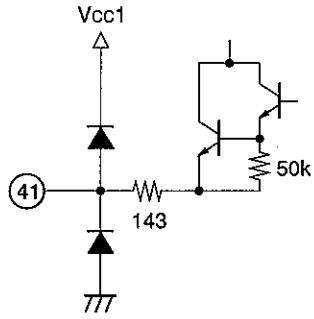
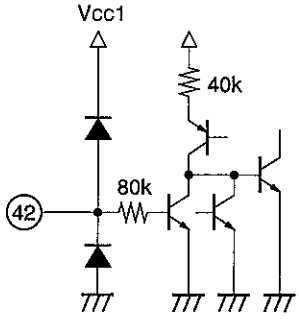
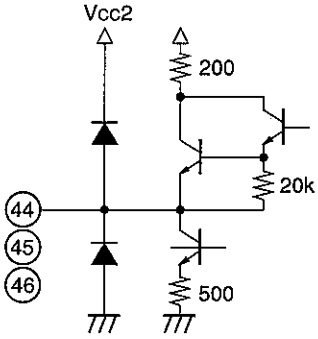
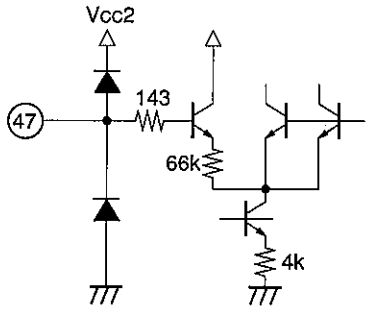
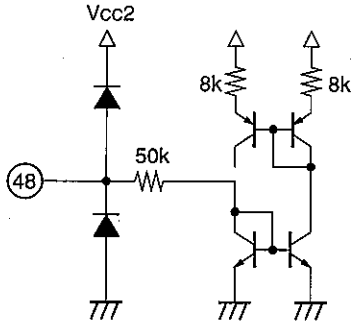
Pin Description

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
1 2 3	LR2-IN LG2-IN LB2-IN	6.2		Linear RGB2 inputs. Input a 0.7Vp-p signal (no sync) through capacitor. Picture control is not possible.
4	YS2	–		YS2 control. When YS2 is taken high, the linear RGB2 input signals are selected. V_{IL} max = 0.4V V_{IH} min = 1.0V V_{IH} max = 3.0V
5	YM2	–		YM2 control. When YM2 is taken high, YUVIN1, YUVIN2 and linear RGB1 input signals are attenuated by 10dB. V_{IL} max = 0.4V V_{IH} min = 1.0V V_{IH} max = 3.0V
6	Vcc2	9		
7	GND2	0		
8 9 10	LR1-IN LG1-IN LB1-IN	4.7		Linear RGB1 inputs. Input a 0.7Vp-p signal (no sync) through capacitor. Picture control is possible.
11	YS1	–		YS1 control. When YS1 is taken high, the linear RGB1input signals are selected. V_{IL} max = 0.4V V_{IH} min = 1.0V V_{IH} max = 3.0V

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
12	YM1	—		YM1 control. When YM1 is taken high, the YUVIN1 and YUVIN2 input signals are attenuated by 6dB. V_{IL} max = 0.4V V_{IH} min = 1.0V V_{IH} max = 3.0V
13	SDA	—		SDA I/O of the I²C bus protocol. At high impedance when the power is turned off. V_{IL} max = 1.5V V_{IH} min = 3.0V V_{OL} max = 0.6V
14	SCL	—		SCL input of the I²C bus protocol. V_{IL} max = 1.5V V_{IH} min = 3.0V
15 16	SSCP VTIM	—		Composite signal (SSCP: Super Sand Castle Pulse) input. Refer to SSCP Signal Level Drawing for the input level. V_{IH} max = 6.0V
17 18 19 20 21 22	VBLK VEQ VS FFTIM CBLK BGP	—		Various timing pulse outputs. V_{OH} = 3.3V V_{OL} = 0.3V

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
23	CLP1	—		Clamp pulse input for clamping the signal which passes throughY and YUV-SW blocks. BGP output of Pin 22 is applied normally. V_{IL} max = 0.4V V_{IH} min = 1.0V
24	AP-MUTE	—		When AP-MUTE is taken high, black detection is turned off, that is, dynamic picture is turned off. V_{IL} max = 0.4V V_{IL} min = 1.0V
25	APED-C	4.1		Pin for connecting the black detection capacitor. Connect a 10µF capacitor between this pin and GND.
26	CLP-C	4.7		Pin for connecting the Y block clamping capacitor. Connect a 0.47µF capacitor between this pin and GND.
27	VM-OUT	6.4		VM output. A waveform obtained by differentiating signals input to the Y1-IN and Y2-IN pins is output. Maximum 2.0Vp-p (when INPULSE is input)

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
28	SP-MUTE	—		When SP-MUTE is taken high, SHARPNESS is turned off. V_{IL} max = 1.0V V_{IH} min = 2.5V V_{IH} max = 5.0V
29	VM-MUTE	—		When VM-MUTE is taken high, the VM output is turned off. V_{IL} max = 1.0V V_{IH} min = 2.5V V_{IH} max = 5.0V
30	YUV-SW	—		Switching between YUVIN1 and YUVIN2. When YUV-SW is taken low, the YUVIN1 signal is selected. When YUV-SW is taken high, the YUVIN2 signal is selected. V_{IL} max = 1.0V V_{IH} min = 2.0V
31	Vcc1	9		
32	GND1	0		
33 34 35	BY1-IN RY1-IN Y1-IN	4.5		Video block YUVIN1 input. Input the following signal to each pin through capacitor: Pin 33: Color difference (B-Y) signal (1.25Vp-p) Pin 34: Color difference (R-Y) signal (0.98Vp-p) Pin 35: Luminance (Y) signal (0.7Vp-p) (100% color bar)
36	GND	0		
37 38 39	BY2-IN RY2-IN Y2-IN	4.5		Video block YUVIN2 input. Input the following signal to each pin through capacitor: Pin 37: Color difference (B-Y) signal (0.26Vp-p) Pin 38: Color difference (R-Y) signal (0.49Vp-p) Pin 39: Luminance (Y) signal (0.35Vp-p) (100% color bar) Input level: YUVIN1 –6dB

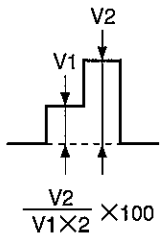
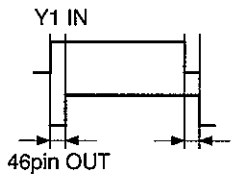
Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
40	NC	—		
41	IREF	2.7		Reference current setting. Connect a 27kΩ resistor between this pin and GND.
42	C-OFF	—		When C-OFF is taken high, COLOR is turned off. VIL max = 0.4V VIH min = 1.0V VIH max = 3.0V
43	GND	0		
44 45 46	ROUT GOUT BOUT	2.5		R, G, and B outputs. The output level is 1.0Vp-p at picture max when only 0.7Vp-p Y signal is input.
47	ABL-REQ	—		ABL control. When the CXA1840S is used as the CRT driver, connect this pin to the ABLFIL pin of the CXA1840S. ABL is disabled at 9V. ABL is maximized at 0V.
48	ABL-MUTE	—		ABL muting by analog control. Mute is applied in the range from 0.7V to 3.0V (maximum mute). Mute is disabled at 0V.

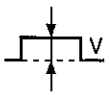
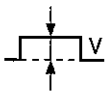
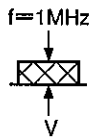
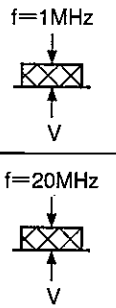
Electrical Characteristics

Setting Conditions (Ta = 25℃, Vcc1 = 9.0V, Vcc2 = 9.0V, GND1 = 0V, GND2 = 0V)

Before taking measurements, set the I²C bus registers as shown in I²C Bus Register Data Initial Setting Values.

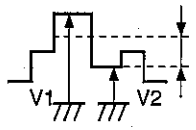
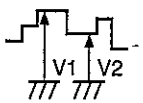
* Refer to the Electrical Characteristics Measurement Circuit for signal input pins and switch states specified in the measurement conditions column.
* For input signals, refer to Signals Used for Measurement.

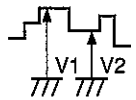
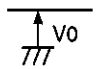
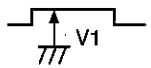
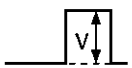
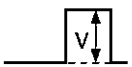
No.	Item	Symbol	Measurement conditions	Mesure-ment pins	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption 1	Icc1		31	Pin inflow current measurement.	20	32	40	mA
2	Current consumption 2	Icc2		6	Pin inflow current measurement.	20	31	40	mA
3	RGB linearity	LIN	Y1 IN/SIG4 PICTURE = 3F	44 45 46		95	99	105	%
4	Y delay time 1-1 NV mode	Tydi1-1	Y1 IN/SIG1 SYSTEM = 0 SHP-F0 = 0	46		310	410	510	ns
5	Y delay time 1-2 NV mode	Tydi1-2	Y1 IN/SIG1 SYSTEM = 0 SHP-F0 = 3	46		200	260	400	ns
6	Y delay time 2-1 FF mode	Tydi2-1	Y1 IN/SIG1 SYSTEM = 2 SHP-F0 = 0	46		170	220	300	ns
7	Y delay time 2-2 FF mode	Tydi2-2	Y1 IN/SIG1 SYSTEM = 2 SHP-F0 = 3	46		100	150	250	ns
8	Y delay time 3-1 HD mode	Tydi3-1	Y1 IN/SIG1 SYSTEM = 3 SHP-F0 = 0	46		50	80	160	ns
9	Y delay time 3-2 HD mode	Tydi3-2	Y1 IN/SIG1 SYSTEM = 3 SHP-F0 = 3	46		20	60	150	ns

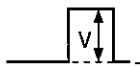
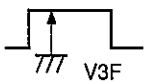
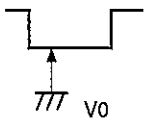
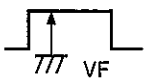
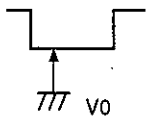
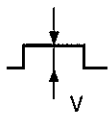
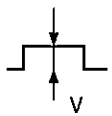
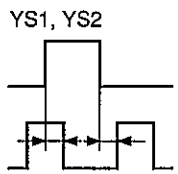
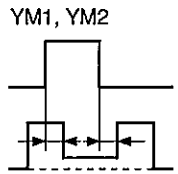
No.	Item	Symbol	Measurement conditions		Mesure-ment pins	Measurement contents		Min.	Typ.	Max.	Unit
10	SUB-CON 1 variable range	Gscon1-1	Y1 IN/SIG1 V30 = GND	SUBCON1 = F	46		$20\log \frac{V(SUBCON1 = F)}{V(SUBCON1 = 7)}$	1.1	1.6	2.2	dB
		Gscon1-2		SUBCON2 = 0			$20\log \frac{V(SUBCON1 = 0)}{V(SUBCON1 = 7)}$	–2.5	–2.0	–1.5	dB
11	SUB-CON 2 variable range	Gscon2-1	Y2 IN/SIG1 V30 = 2.5V	SUBCON2 = F	46		$20\log \frac{V(SUBCON2 = F)}{V(SUBCON2 = 7)}$	1.1	1.6	2.2	dB
		Gscon2-2		SUBCON2 = 0			$20\log \frac{V(SUBCON2 = 0)}{V(SUBCON2 = 7)}$	–2.5	–2.0	–1.5	dB
12	Y frequency response characteristic 1 NV mode	Gyf1	Y1 IN/SIG8, SIG14 0.7Vpp SHP-F0 = 3 SYSTEM = 0		44 45 46		$20\log \frac{V(f = 10MHz)}{V(f = 1MHz)}$	–3	—	—	dB
13	Y frequency response characteristic 2 FF mode	Gyf2	Y1 IN/SIG8, SIG16 0.7Vpp SHP-F0 = 3 SYSTEM = 2		44 45 46		$20\log \frac{V(f = 20MHz)}{V(f = 1MHz)}$	–3	—	—	dB

No.	Item	Symbol	Measurement conditions		Mesure-ment pins	Measurement contents		Min.	Typ.	Max.	Unit
14	Y frequency response characteristic 3 HD mode	Gyf3	Y1 IN/SIG8, SIG16 0.7Vpp SHP-F0 = 3 SYSTEM = 3		44 45 46	f=1MHz V f=20MHz V	$20\log \frac{V\,(f = 20MHz)}{V\,(f = 1MHz)}$	–3			dB
15	DC transmission ratio 1	Gdt1	Y1 IN/SIG1 Y1 IN/SIG5 Y1 IN/GND	DC-TRAN = 0	46	SIG1 V1 no signal V2 SIG5 V3	$\frac{V1 - V2}{V3} \times 100$	97	99	102	%
16	DC transmission ratio 2	Gdt2	Y1 IN/SIG1 Y1 IN/SIG5 Y1 IN/GND	DC-TRAN = 3	46	SIG1 V1 no signal V2 SIG5 V3	$\frac{V1 - V2}{V3} \times 100$	75	82	88	%
17	VM operation	Vvm1	Y1 IN/SIG10 0.7Vpp	VM-LEV = 0	27			0	—	30	mV
		Vvm2		VM-LEV = 3				1.6	2.1	2.6	V

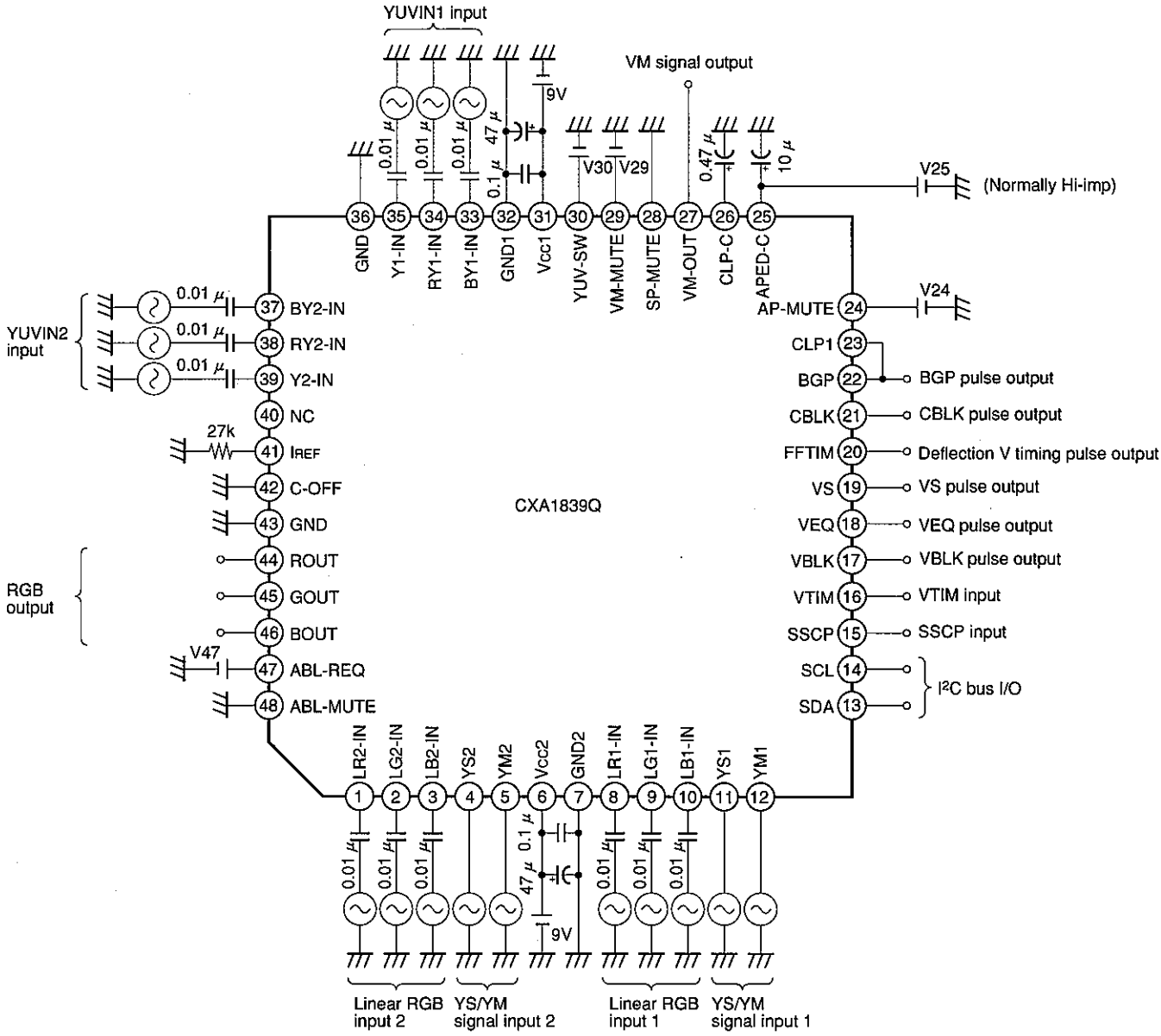
No.	Item	Symbol	Measurement conditions		Mesure-ment pins	Measurement contents		Min.	Typ.	Max.	Unit
18	NR operation	Gnr1	Y1 IN/SIG11 140mVpp SHP-F0 = 3	NR-LEV = 0	46	f=5MHz V	$20\log \frac{V\ (NRLEV = 3)}{V\ (NRLEV = 0)}$	–8.5	–5.5	–2.5	dB
				NR-LEV = 3							
19	COLOR variable range	Gcol1	BY1 IN/SIG17 0.5Vpp Y1 IN/SIG2	COLOR = 3F	46	V	$20\log \frac{V\ (COLOR = 3F)}{V\ (COLOR = 1F)}$	4.8	5.8	6.8	dB
		Gcol2		COLOR = 0			$20\log \frac{V\ (COLOR = 0)}{V\ (COLOR = 1F)}$	—	—	–40	dB
20	SUB-COL 1 variable range	Gscol1-1	BY1 IN/SIG17 0.5Vpp Y1 IN/SIG2 V30 = 0V SUB-COL1 = 0/7/F		46	V	$20\log \frac{V\ (SUBCOL1 = F)}{V\ (SUBCOL1 = 7)}$	1.1	1.6	2.1	dB
		Gscol1-2					$20\log \frac{V\ (SUBCOL1 = 0)}{V\ (SUBCOL1 = 7)}$	–2.3	–1.8	–1.3	dB
21	SUB-COL 2 variable range	Gscol2-1	BY2 IN/SIG17 0.25Vpp Y2 IN/SIG2 V30 = 2.5V SUB-COL2 = 0/7/F		46	V	$20\log \frac{V\ (SUBCOL2 = F)}{V\ (SUBCOL2 = 7)}$	1.1	1.6	2.1	dB
		Gscol2-2					$20\log \frac{V\ (SUBCOL2 = 0)}{V\ (SUBCOL2 = 7)}$	–2.3	–1.8	–1.3	dB

No.	Item	Symbol	Measurement conditions		Mesure-ment pins	Measurement contents		Min.	Typ.	Max.	Unit
22	HUE control characteristic	θ max	Y IN/SIG2 RY1 IN/SIG17 0.57Vpp BY1 IN/SIG17 1.015Vpp SUB HUE = 7	HUE = 3F	46		Pin 46 output VB = V1 – V2	28	34	40	deg.
		θ cent		HUE = 1F		$\theta = \tan^{-1} \frac{VB\ (RY1\ IN/SIG17)}{VB\ (BY1\ IN/SIG17)}$ The above is used as the center value.		–7	0	7	deg.
		θ min		HUE = 00		θ MAX = θ(3F) – θ(1F) θ MIN = θ(00) – θ(1F)		–40	–34	–28	deg.
23	SUB HUE control characteristic	θ MIN	Y IN/SIG2 RY1 IN/SIG17 0.57Vpp BY1 IN/SIG17 1.015Vpp HUE = 1F	SUB HUE = 0	46	Same as the measurement of HUE control characteristic except that SUB HUE is controlled instead of HUE.		–9.0	–7.0	–6.0	deg.
		θ MAX		SUB HUE = F				7.0	9.0	11.0	deg.
24	R-Y axis/R-Y component	Gry/r	Y1/SIG2 RY1/SIG17 0.57Vpp BY1/SIG17 1.015Vpp HUE = 1F	R-Y/R = 0	44 46	 Pin 44 output VR = V1 – V2 Pin 46 output VB = V1 – V2	$\frac{VR\ (RY1/SIG17)}{VB\ (BY1/SIG17)}$	0.76	0.87	0.97	–
				R-Y/R = F				0.42	0.48	0.55	
25	R-Y axis/B-Y component	Gry/b		B-Y/B = 0			$\frac{VR\ (BY1/SIG17)}{VB\ (BY1/SIG17)}$	–0.4	–0.35	–0.3	–
				B-Y/B = F				–0.03	0	0.03	

No.	Item	Symbol	Measurement conditions		Mesure-ment pins	Measurement contents		Min.	Typ.	Max.	Unit
26	G-Y axis/R-Y component	Ggy/r	Y1/SIG2 RY1/SIG17 0.57Vpp BY1/SIG17 1.015Vpp HUE = 1F	G-Y/R = 0	45 46	 Pin 45 output VG = V1 – V2 Pin 46 output VB = V1 – V2	$\frac{VG\ (RY1/SIG17)}{VB\ (BY1/SIG17)}$	–0.4	–0.36	–0.3	–
				G-Y/R = F				–0.22	–0.18	–0.15	
27	G-Y axis/B-Y component	Ggy/b		G-Y/B = 0			$\frac{VG\ (BY1/SIG17)}{VB\ (BY1/SIG17)}$	–0.31	–0.27	–0.2	–
				G-Y/B = F				–0.08	–0.04	–0.02	
28	AGING 1 operation	Vag1	No signal	AGING1 = 0	44 45 46		V1 – V0	350	430	500	mV
				AGING1 = 1							
29	RGB1-LEV variable range	Grgb1-1	LR1, LG1, LB1 IN/SIG5 PICTURE = MAX YS1 = 1V	RGB1-LEV = F	44 45 46	 Each of R, G and B outputs	$20\log \frac{V\ (RGB1\text{-}LEV = F)}{V\ (RGB1\text{-}LEV = 7)}$	1.5	2.5	3.5	dB
		Grgb1-2		RGB1-LEV = 0			$20\log \frac{V\ (RGB1\text{-}LEV = 0)}{V\ (RGB1\text{-}LEV = 7)}$	–4.5	–3.5	–2.5	dB
30	RGB2-LEV variable range	Grgb2-1	LR2, LG2, LB2 IN/SIG5 PICTURE = MAX YS2 = 1V	RGB2-LEV = F	44 45 46	 Each of R, G and B outputs	$20\log \frac{V\ (RGB2\text{-}LEV = F)}{V\ (RGB2\text{-}LEV = 7)}$	1.5	2.5	3.5	dB
		Grgb2-2		RGB2-LEV = 0			$20\log \frac{V\ (RGB2\text{-}LEV = 0)}{V\ (RGB2\text{-}LEV = 7)}$	–4.3	–3.5	–2.3	dB

No.	Item	Symbol	Measurement conditions		Mesure-ment pins	Measurement contents		Min.	Typ.	Max.	Unit
31	RGB picture variable range	Gpic1	LR1, LG1, LB1 IN/SIG5	PICTURE = 3F	44 45 46	 Each of R, G and B outputs	$20\log \frac{V(PICTURE = 3F)}{V(PICTURE = 1F)}$	4.0	5.0	6.0	dB
		Gpic2		PICTURE = 00			$20\log \frac{V(PICTURE = 0)}{V(PICTURE = 1F)}$	–13.5	–11.8	–10.0	dB
32	BRIGHT variable range	Δ Vbrt1	No. signal	BRIGHT = 3F	46		V3F – V(BRIGHT = 1F)	100	150	200	mV
		Δ Vbrt2		BRIGHT = 0			V0 – V(BRIGHT = 1F)	–200	–150	–100	mV
33	SUB-BRIGHT variable range	Δ Vsbrt1	No. signal	SUBBRIGHT = F	46		VF – V(SUB-BRIGHT = 7)	55	80	105	mV
		Δ Vsbrt2		SUBBRIGHT = 0			V0 – V(SUB-BRIGHT = 7)	–90	–70	–45	mV
34	YM1 operation	Gym1	Y1 IN/SIG1		46		$20\log \frac{V (YM1 ON)}{V (YM1 OFF)}$	–7	–6	–5	dB
35	YM2 operation	Gym2	Y1 IN/SIG1		46		$20\log \frac{V (YM2 ON)}{V (YM2 OFF)}$	–11.5	–9.5	–7.0	dB
36	YM1, YM2, YS1, YS2 operation delay	Tym1 Tym2 Tys1 Tys2	Y1 IN/SIG5 LR1, LG1, LB1 IN/No signal LR2, LG2, LB2 IN/No signal YS1, YS2, YM1, YM2 IN/SIG18		46			0	30	70	ns

Electrical Characteristics Measurement Circuit



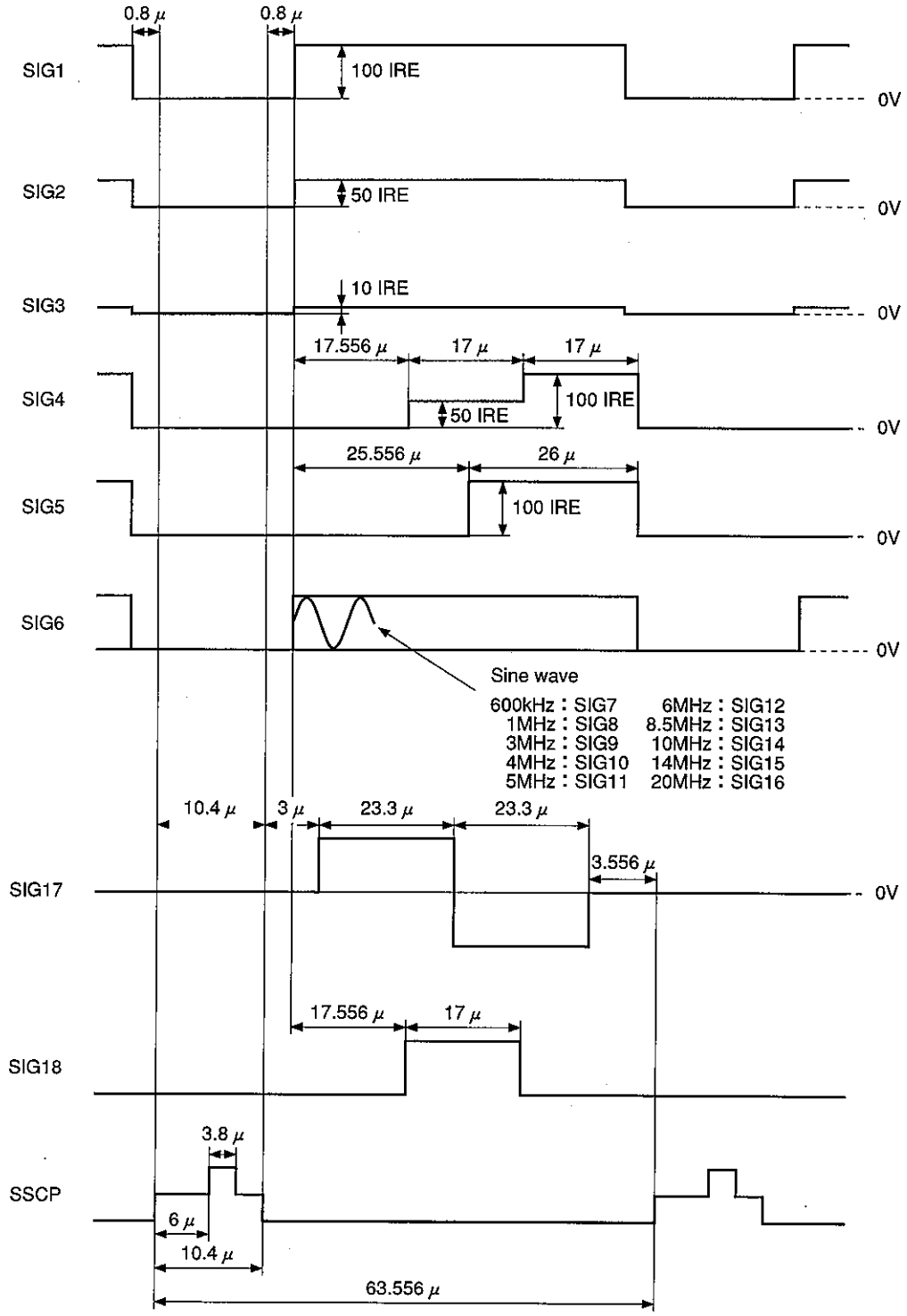
I²C Bus Register Data Initial Setting Values

Register name	Initial setting value	Register name	Initial setting value	Register name	Initial setting value	Register name	Initial setting value	Register name	Initial setting value
PICTURE	1F	R-Y/R	5	SUB-COL2	7	DC-TRAN	0	POL-SW	0
HUE	1F	R-Y/B	C	RGB1-LEVEL	7	DYNAMIC-PIC	0	SHP-LIM	0
COLOR	1F	G-Y/R	9	RGB2-LEVEL	7	CEC-LEVEL	0	D-ABL	0
BRIGHT	1F	G-Y/B	8	SUB-SHP	0	VM-LEVEL	0	YSYM-SW	0
SHARPNESS	1F	SUB-CON1	7	SHP-F0	0	ABL-MODE	0	AGING1	0
SUB-HUE	7	SUB-COL1	7	PRE-OVER	0	D-COL	0	AGING2	0
SUB-BRIGHT	7	SUB-CON2	7	NR-LEVEL	0	SYSTEM	0		

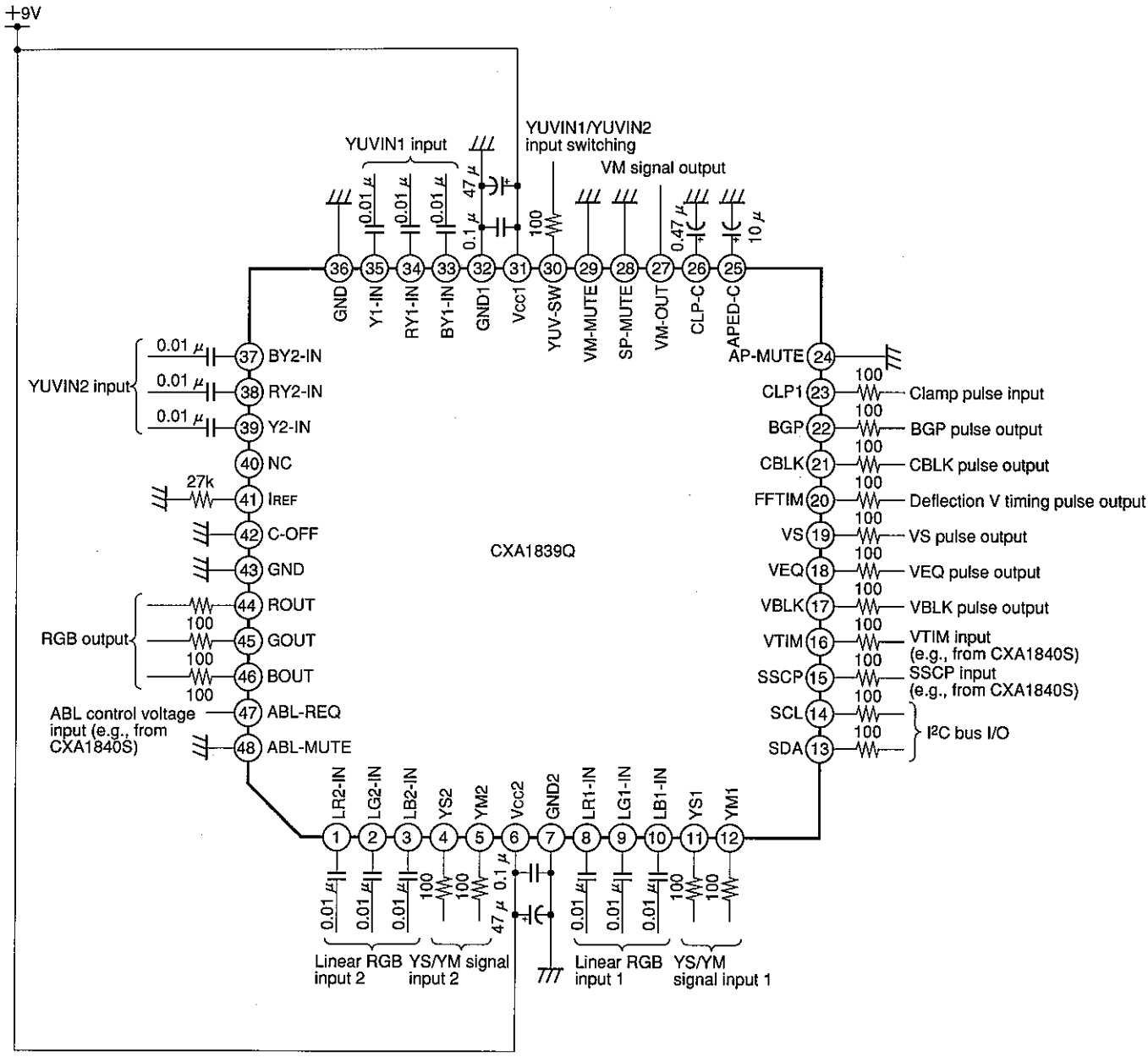
Signals Used for Measurement

Signal levels Input to YUVIN1, linear RGB1, linear RGB2: 100 IRE = 0.7V
Input to YUVIN2: 100 IRE = 0.35V

Refer to the measurement conditions column of Electrical Characteristics for the signal levels not specified in the figure below.



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1) YUV-SW operation

This IC has two Y/color difference input blocks (YUVIN1 and YUVIN2). Input signals of YUVIN1 and YUVIN2 are input to the YUV-SW circuit, which selects either block according to the voltage of Pin 30. The selected signal is then output to the Y signal processing block and the color difference signal processing block. The IC is provided with gain control amplifiers to perform subcontrast control and subcolor control.

The signal input level of YUVIN2 (Pins 37, 38 and 39) is 6dB lower than that of YUVIN1 (Pins 33, 34 and 35). However, as the YUV-SW circuit raises the signal input level of YUVIN2 by 6dB, both signals are processed on the same level inside the IC.

2) Y signal processing

The Y signal of the Y/color difference signal selected by the YUV-SW circuit is output to the matrix clamp circuit through the sharpness control (delay line aperture correction), coring noise reduction, clamp, DC transmission ratio correction, and dynamic picture circuits.

The sharpness control fo is set to the value matching the TV system (NV, FF, HD) specified via the I²C bus. It can also be adjusted freely via the I²C bus.

A signal obtained by differentiating the Y signal is output from Pin 27 as the VM signal. When YS1 and YS2 pin voltages are taken high, the VM output is muted automatically. The VM output can also be muted by taking the Pin 29 voltage high.

The delay time of each delay line of the sharpness circuit varies with TV systems (NV, FF, HD) specified via the I²C bus. In other words, the signal I/O delay time varies with TV systems (NV, FF, HD).

The dynamic picture circuit detects the maximum black level of the video signal and compares it with the reference voltage inside the IC. When the signal level is lower than the reference (inflection point), the signal is gain-controlled to come closer to the pedestal level (black-level Stretcher).

The inflection point of dynamic picture and the control amount of sharpness, noise reduction,and DC transmission ratio can be set via the I²C bus. Sharpness can be muted by taking the Pin 28 voltage high. The dynamic picture operation can be turned off by taking the Pin 24 voltage high.

This IC is able to output aging signals AGING1 (all-white output mode) and AGING2 (all-black output mode), which can be turned on/off via the I²C bus. When AGING1 or AGING2 is turned on, the color function is automatically turned off. Precedence is given to AGING2 over AGING1. The aging signal is not output when linear RGB1 or linear RGB2 is selected.

3) Color difference signal processing

The color difference signal of the Y/color difference signal selected by the YUV-SW circuit is output to the matrix clamp circuit through the CEC (chrominance edge clear: chroma transient improving circuit with delay line), HUE, COLOR and AXIS control circuits.

The CEC circuit creates a correction signal to sharpen the rising and falling edges of the color difference signal with delay line, then adds the correction signal to the original color difference signal to improve chroma transient.

The color difference signal going through the CEC circuit is fed to the base-band HUE circuit, then color-controlled by the gain control amplifier. When the COLOR register data of the I²C bus is set to 00H, the color function is turned off by the switch circuit.

The AXIS circuit adjusts the detective axis and creates G-Y component based upon R-Y and B-Y components. The detective axis is set by fixing the B-Y axis and setting R-Y and G-Y axis components.

The CEC, HUE, COLOR and AXIS functions can be controlled via the I²C bus. The COLOR control function can be turned off by taking the Pin 42 voltage high.

Color difference signals R-Y, G-Y and B-Y generated by the AXIS circuit are output to the matrix clamp circuit. The matrix clamp circuit then creates R, G and B signals based upon the color difference signal and the Y signal, and outputs them to the RGB signal processing circuit.

4) RGB signal processing

The R, G and B signals created from the Y/color difference signal are output to the outside of IC as the RGB signal via the YM1, picture, YM2, dynamic color and brightness circuits. When the voltage at Pin 12 is taken high, YM1 attenuates signals input to YUVIN1 and YUVIN2 by 6 dB. When the voltage at Pin 5 goes high, YM2 attenuates signals input to YUVIN1, YUVIN2 and linear RGB1 by 10dB. The dynamic color function changes the RGB output ratio and increases the color temperature only when 75% of the R signal level is lower than the G or B signal level.

This IC has two linear RGB input blocks. When the voltage at Pin 11 is taken high, linear RGB1 signals (Pins 8, 9 and 10) are selected and output as the RGB signal through the YM1, picture, YM2, dynamic color and brightness circuits. When the voltage at Pin 4 is taken high, linear RGB2 signals (Pins 1, 2 and 3) are selected and output as the RGB signal through the YM2, dynamic color, and brightness circuits. Therefore, YM1 and picture control are disabled when linear RGB2 signals are selected.

The YS1, YM1 inhibit mode is set when the YSYMSW register of the I^2C bus is set to 1. In this mode, linear RGB1 signals are not selected even when voltages at Pins 11 and 12 are taken high, and YM1 does not execute attenuation.

This IC implements the ABL function. Apply the ABL control voltage to the ABL control pin (Pin 47). When the CXA1840S is used as the CRT driver, connect Pin 47 to the ABLFIL pin of the CXA1840S. The ABL control voltage applied to Pin 27 is compared with the internal reference voltage to perform the picture control (picture ABL) and the brightness control (brightness ABL). The ratio between picture ABL and brightness ABL can be changed using the I^2C bus.

In addition to ABL, the dynamic ABL function is provided and can be turned on/off using the I^2C bus. The dynamic ABL function works independently of ABL. Turning on the dynamic ABL function sets the picture ABL exclusive mode. Brightness ABL is also executed when the maximum black level of video is higher than the reference value.

5) Pulse interface

The pulse interface block generates various timing pulses based upon SSCP (Super Sand Castle Pulse: 4-value sand castle pulse) input to Pin 15. Of various pulses, the burst gate pulse and the composite blanking pulse are also output to the inside of IC and used as clamp and blanking timing. Input YUV-SW circuit and Y block clamping pulses to Pin 23, but in normal operation use the burst gate pulse output from Pin 22.

Description of Registers

Register name	Number of bits:	Function
PICTURE	(6):	Picture control 00: min –16.8dB 3F: max 0dB
D-COL	(1):	Dynamic color ON/OFF 0: off 9300° 1: on 11500°
HUE	(6):	Hue control. For YUVIN1 and YUVIN2 inputs. 00: max –34° 1F: center 0° 3F: max +34°
SYSTEM	(2):	Signal frequency band switching. Select the frequency band of the TV system in use. 0: NORMAL 2: FF 1: inhibited 3: HD
COLOR	(6):	Color control 00: min Color OFF 1F: center 0dB 3F: max +5.8dB
POL-SW	(1):	Color difference signal polarity setting 0: positive polarity input 1: negative polarity input
SHP-LIM	(1):	Sharpness limiter ON/OFF 0: off 1: on
BRIGHT	(6):	Brightness control. For all inputs. 00: min –15 IRE 1F: center 0 IRE 3F: max +15 IRE
D-ABL	(1):	Dynamic ABL ON/OFF 0: off 1: on
YSYM-SW	(1):	YS1/YM1 inhibit ON/OFF 0: off 1: on
SHARPNESS	(6):	Sharpness control. For YUVIN1 and YUVIN2 inputs. 00: min -10dB 1F: center +2dB 3F: max +7dB
AGING1	(1):	White signal generation ON/OFF 0: off Only when aging process of production line is used. 1: on When YUVIN1/YUVIN2 is selected and no signal, a white signal equivalent to 60 IRE is generated.
AGING2	(1):	Black signal generation ON/OFF 0: off 1: on When only YUVIN1/YUVIN2 is selected, all black and precedence is given to AGING2 over AGING1.

SUB-HUE (4): Hue center adjustment
0: flesh color → red MAX −7°
7: center 0°
F: flesh color → green MAX +9°

SUB-BRIGHT (4): Subbright adjustment
0: min −7 IRE
7: center 0 IRE
F: max +8 IRE

R-Y/R (4): Detective axis (R-Y component of R-Y axis) setting
0: max 0.87 (B-Y = 1.0) Example: JPN 5
F: min 0.48 US 7
PAL D

R-Y/B (4): Detective axis (B-Y component of R-Y axis) setting
0: max −0.35 Example: JPN C
F: min 0 US 3
PAL F

G-Y/R (4): Detective axis (R-Y component of G-Y axis) setting
0: max −0.36 Example: JPN 9
F: min −0.18 US 8
PAL B

G-Y/B (4): Detective axis (B-Y component of G-Y axis) setting
0: max −0.27 Example: JPN 8
F: min −0.04 US C
PAL 7

SUB-CON1 (4): Subcontrast 1 level adjustment; Y level adjustment of YUVIN1
0: min −2dB
F: max +1.6dB

SUB-COL1 (4): Subcolor 1 level adjustment; Color difference level adjustment of YUVIN1
0: min −1.8dB
F: max +1.6dB

SUB-CON2 (4): Subcontrast 2 level adjustment; Y level adjustment of YUVIN2
0: min −2dB
F: max +1.6dB

SUB-COL2 (4): Subcolor 2 level adjustment; Color difference level adjustment of YUVIN2
0: min −1.8dB
F: max +1.6dB

RGB1-LEVEL (4): Linear RGB1 input level adjustment
0: min −6.0dB
F: max 0dB

RGB2-LEVEL (4): Linear RGB2 input level adjustment
0: min −6.0dB
F: max 0dB

SUB-SHP (2): Sharpness center adjustment
0: min 0dB
3: max +3.7dB (SHARPNESS center)

SHP-F0 (2): Sharpness F0 setting.
The following values are set according to the SYSTEM setting.

	NORMAL	FF	HD
0: min	2.9MHz	5.7MHz	8.6MHz
3: max	4.8MHz	9.5MHz	14.3MHz

PRE-OVER (2): Preshoot/overshoot ratio setting
0: preshoot vs. overshoot = 1:1
3: preshoot vs. overshoot = 2:1

NR-LEVEL (2): Y signal noise reduction level setting
0: off
3: max 10 IRE (coring level)

DC-TRAN (2): DC transmission ratio setting
0: max 100%
3: min 82%

DYNAMIC-PIC (2): Auto pedestal setting
0: off
3: max Pull-in level 8 IRE

CEC-LEVEL (2): Chroma transient improvement level setting (strong, medium, weak)
0: off
3: max

VM-LEVEL (2): VM output level adjustment
0: off 0Vpp
3: max 2.1Vpp (at the time of 100% color bar signal input)

ABL-MODE (2): ABL mode setting
0: picture ABL mode
3: Maximum brightness ABL in the picture ABL and brightness ABL combination mode

Definition of I²C Bus Register

Slave address 8AH: SLAVE RECEIVER

Register Table

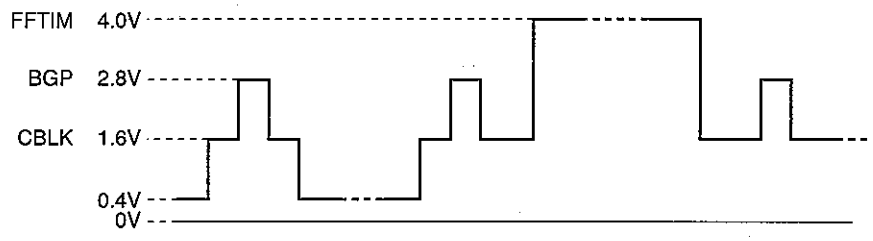
- * is undefined.
- The one-bit switch register is set to 0 when IC power supply is turned on.

[Control Register]

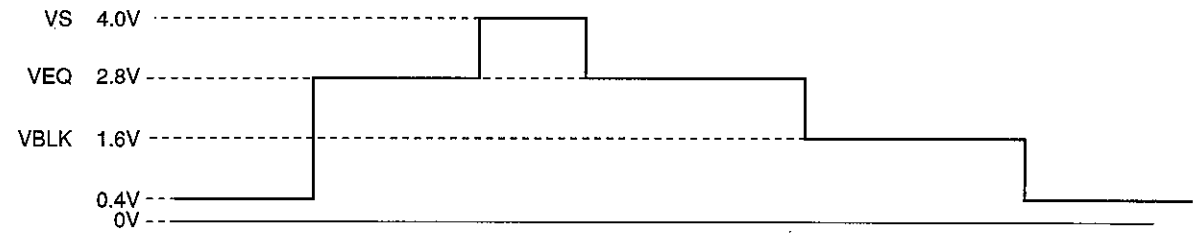
SUB ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0 0 0 0	PICTURE						0	D-COL
0 0 0 1	HUE						SYSTEM	
0 0 1 0	COLOR						POL-SW	SHP-LIM
0 0 1 1	BRIGHT						D-ABL	YSYM-SW
0 1 0 0	SHARPNESS						AGING1	AGING2
0 1 0 1	SUB-HUE				SUB-BRIGHT			
0 1 1 0	R-Y/R				R-Y/B			
0 1 1 1	G-Y/R				G-Y/B			
1 0 0 0	SUB-CON1				SUB-COL1			
1 0 0 1	SUB-CON2				SUB-COL2			
1 0 1 0	RGB1-LEVEL				RGB2-LEVEL			
1 0 1 1	SUB-SHP		SHP-F0		PRE-OVER		NR-LEVEL	
1 1 0 0	DC-TRAN		DYNAMIC-PIC		CEC-LEVEL		VM-LEVEL	
1 1 0 1	ABL-MODE		*	*	*	*	*	*

SSCP, VTIM Signal Input Level

SSCP



VTIM



Notes on Operation

When using this IC, be careful of the treatment of the following pins.

Pins 1, 2 and 3: Linear RGB2 input
Pins 8, 9 and 10: Linear RGB1 input

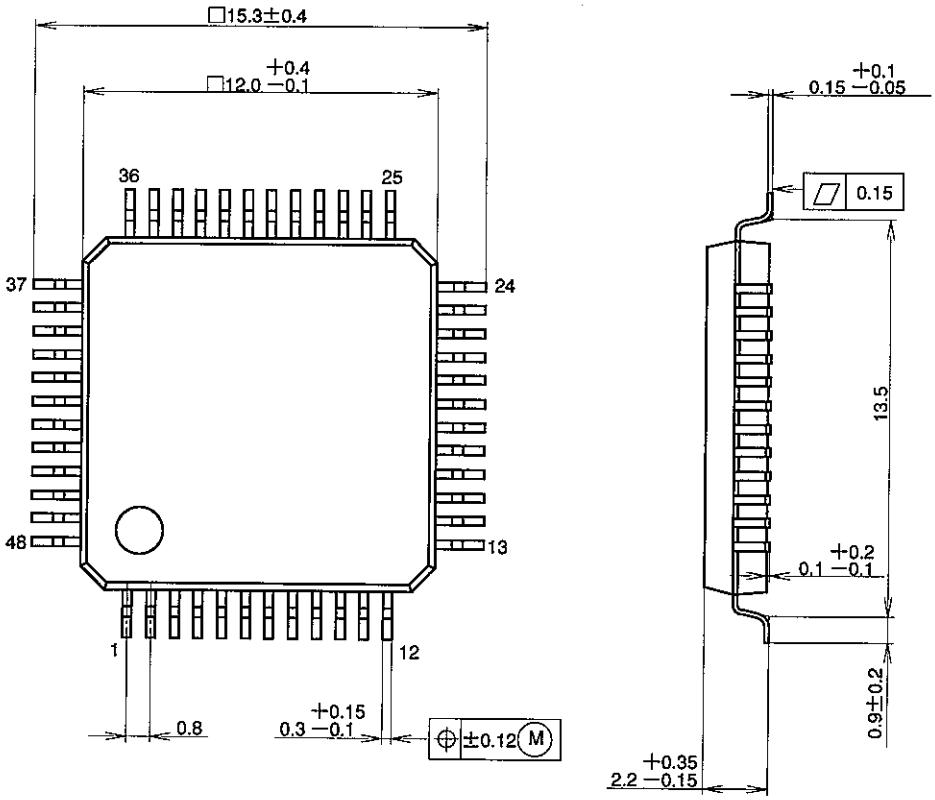
When the above pins are not in use, carry out either of the following:

1) Connect each pin to Vcc.
2) Connect each pin to GND via a capacitor.

When the above pins are connected directly to GND, a current of several ten mA flows to GND so that the IC does not operate normally.

Package Outline Unit : mm

48PIN QFP(PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).