

4MHz, BiMOS Operational Amplifier with MOSFET Input/CMOS Output

CA3260A and CA3260 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

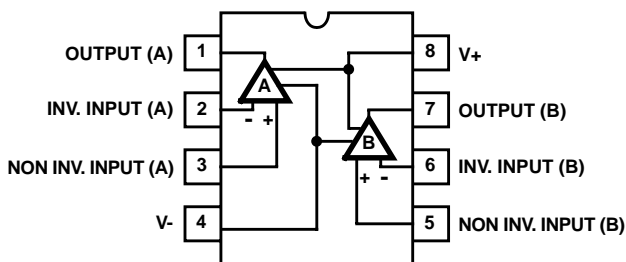
Gate protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3260 Series circuits operate at supply voltages ranging from 4V to 16V, or $\pm 2V$ to $\pm 8V$ when using split supplies. The CA3260A offers superior input characteristics over those of the CA3260.

Pinout

**CA3260, CA3260A (PDIP)
TOP VIEW**



Features

- MOSFET Input Stage provides
 - Very High $Z_i = 1.5T\Omega$ ($1.5 \times 10^{12}\Omega$) (Typ)
 - Very Low I_i 5pA (Typ) at 15V Operation
..... 2pA (Typ) at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (Or Both) Supply Rails

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Wien Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3260E	-55 to 125	8 Ld PDIP	E8.3
CA3260AE	-55 to 125	8 Ld PDIP	E8.3

CA3260, CA3260A

Absolute Maximum Ratings

DC Supply Voltage (V+ to V-)	16V
DC Input Voltage	(V+ +8V) to (V- -0.5V)
Differential Input Voltage	8V
Input Terminal Current	1mA
Output Short Circuit Duration (Note 1)	Indefinite

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	100	N/A
Maximum Junction Temperature (Plastic Package)	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C	

Operating Conditions

Temperature Range -55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- Short circuit may be applied to ground or to either supply.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^\circ\text{C}$, Typical Values Intended Only for Design Guidance

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA3260A	CA3260	
Input Resistance	R_I	$V_S = \pm 7.5\text{V}$	1.5	1.5	$\text{T}\Omega$
Input Capacitance	C_I	$f = 1\text{MHz}, V_S = \pm 7.5\text{V}$	4.3	4.3	pF
Unity Gain Crossover Frequency	f_T	$V_S = \pm 7.5\text{V}$	4	4	MHz
Slew Rate	SR	$V_S = \pm 7.5\text{V}$	10	10	$\text{V}/\mu\text{s}$
Transient Response	Rise Time	$C_L = 25\text{pF}, R_L = 2\text{k}\Omega, A_V = +1, V_S = \pm 7.5\text{V}$	0.09	0.09	μs
	Overshoot		10	10	%
Settling Time (to <0.1%, $V_{IN} = 4V_{P-P}$)	t_S	$C_L = 25\text{pF}, R_L = 2\text{k}\Omega, A_V = +1, V_S = \pm 7.5\text{V}$	1.8	1.8	μs
Input Offset Voltage	V_{IO}	$V_+ = 5\text{V}, V_- = 0\text{V}$	2	6	mV
Input Offset Current	I_{IO}	$V_+ = 5\text{V}, V_- = 0\text{V}$	0.1	0.1	pA
Input Current	I_I	$V_+ = 5\text{V}, V_- = 0\text{V}$	2	2	pA
Common Mode Rejection Ratio	CMRR	$V_+ = 5\text{V}, V_- = 0\text{V}$	70	60	dB
Large Signal Voltage Gain	A_{OL}	$V_O = 4V_{P-P}, R_L = 20\text{k}\Omega, V_+ = 5\text{V}, V_- = 0\text{V}$	100	100	kV/V
			100	100	dB
Common Mode Input Voltage Range	V_{ICR}	$V_+ = 5\text{V}, V_- = 0\text{V}$	0 to 2.5	0 to 2.5	V
Supply Current	I_+	$V_O = 5\text{V}, R_L = \infty, V_+ = 5\text{V}, V_- = 0\text{V}$	1	1	mA
		$V_O = 2.5\text{V}, R_L = \infty, V_+ = 5\text{V}, V_- = 0\text{V}$	1.2	1.2	mA
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V_+, V_+ = 5\text{V}, V_- = 0\text{V}$	200	200	$\mu\text{V}/\text{V}$

Electrical Specifications For Each Amplifier at $T_A = 25^\circ\text{C}$, $V_+ = 15\text{V}, V_- = 0\text{V}$, Unless Otherwise Specified

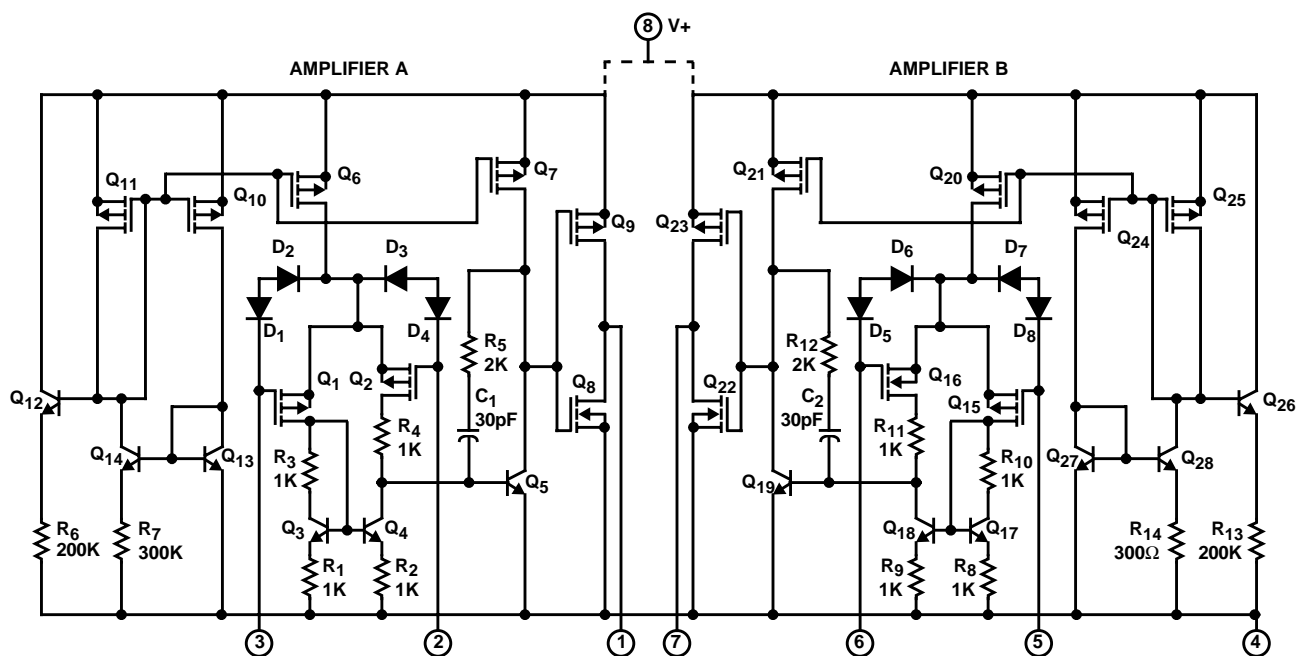
PARAMETER	SYMBOL	TEST CONDITIONS	CA3260A			CA3260			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$ V_{IO} $	$V_S = \pm 7.5\text{V}$	-	2	5	-	6	15	mV
Input Offset Current	$ I_{IO} $	$V_S = \pm 7.5\text{V}$	-	0.5	20	-	0.5	30	pA
Input Current	I_I	$V_S = \pm 7.5\text{V}$	-	5	30	-	5	50	pA
Large Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}, R_L = 10\text{k}\Omega$	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		80	95	-	70	90	-	dB

CA3260, CA3260A

Electrical Specifications For Each Amplifier at $T_A = 25^\circ\text{C}$, $V_+ = 15\text{V}$, $V_- = 0\text{V}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	CA3260A			CA3260			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Common Mode Input Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V	
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V_+$ $V_+ = 17.5\text{V}$	-	32	150	-	32	320	$\mu\text{V}/\text{V}$	
Maximum Output Voltage	V_{OM+}	$R_L = 10\text{k}\Omega$	11	13.3	-	11	13.3	-	V	
	V_{OM-}		-	0.002	0.01	-	0.002	0.01	V	
	V_{OM+}	$R_L = \infty$	14.99	15	-	14.99	15	-	V	
	V_{OM-}		-	0	0.01	-	0	0.01	V	
Maximum Output Current	I_{OM+} Source	$V_O = 7.5\text{V}$	12	22	45	12	22	45	mA	
	I_{OM-} Sink		12	20	45	12	20	45	mA	
Total Supply Current V_O (Amplifier A) = 7.5V V_O (Amplifier B) = 7.5V	I_+	$R_L = \infty$	-	9	15.5	-	9	15.5	mA	
			V_O (Amplifier A) = 0V V_O (Amplifier B) = 0V	-	1.2	3	-	1.2	3	mA
			V_O (Amplifier A) = 0V V_O (Amplifier B) = 7.5V	-	5	8.5	-	5	8.5	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	6	-	-	8	-	$\mu\text{V}/^\circ\text{C}$	
Crosstalk		$f = 1\text{kHz}$	-	120	-	-	120	-	dB	

Schematic Diagram



All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>