WM8720

24-bit, 96kHz Stereo DAC with Volume Control

DESCRIPTION

The WM8720 is a high performance stereo DAC designed for audio applications such as CD, DVD, home theatre systems, set top boxes and digital TV. The WM8720 supports data input word lengths from 16 to 24-bits and sampling rates up to 96kHz. The WM8720 consists of a serial interface port, digital interpolation filter, multi-bit sigma delta modulator and stereo DAC in a small 20-pin SSOP package. The WM8720 also includes a digitally controllable mute and attenuator function on each channel.

The WM8720 supports a variety of connection schemes for audio DAC control. The SPI-compatible serial control port provides access to a wide range of features including on-chip mute, attenuation and phase reversal. A hardware controllable interface is also available.

The programmable data input port supports a variety of glueless interfaces to popular DSPs, audio decoders and S/PDIF and AES/EBU receivers.

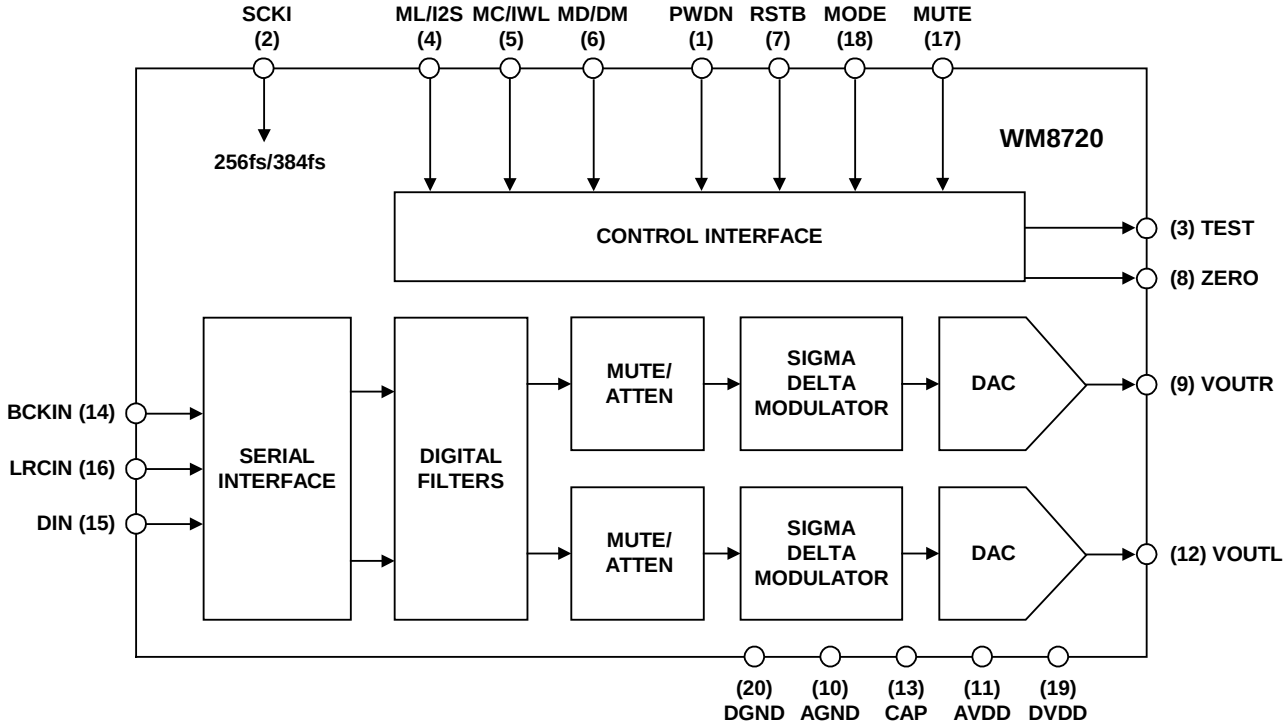
FEATURES

- Performance:
  - 102dB SNR ('A' weighted @48kHz),
  - THD: -95dB @ 0dB FS
- 5V or 3.3V supply operation
- Sampling frequency: 8kHz to 96kHz
- Input data word: 16 to 24-bit
- Hardware or SPI compatible serial port control modes:
  - Hardware mode: system clock, reset, mute, de-emphasis
  - Serial control mode: mute, de-emphasis, digital attenuation (256 steps), zero mute, phase reversal, power down

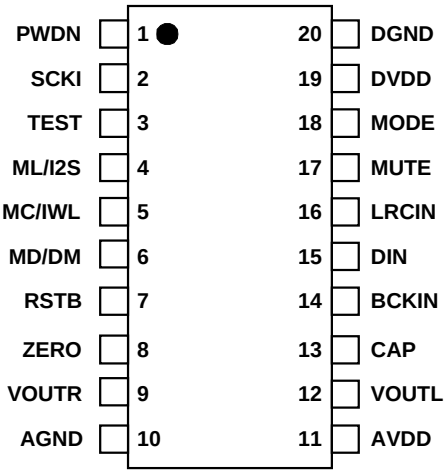
APPLICATIONS

- CD, DVD audio
- Home theatre systems
- Set top boxes
- Digital TV

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM8720EDS	-25 to +85°C	20-pin SSOP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	PWDN	Digital input	Powerdown control; low is ON, high is POWER OFF. Internal pull-down.
2	SCKI	Digital input	System clock input (256 or 384fs).
3	TEST	Digital output	Reserved.
4	ML/I2S	Digital input	Latch enable (software mode) or input format selection (hardware mode). Internal pull-up.
5	MC/IWL	Digital input	Serial control data clock input (software mode) or input word length selection (hardware mode). Internal pull-up.
6	MD/DM	Digital input	Serial control data input (software mode) or de-emphasis selection (hardware mode). Internal pull-up.
7	RSTB	Digital input	Reset input – active low. Internal pull-up.
8	ZERO	Digital output	Infinite zero detect – active low. Open drain type output with active pull-down.
9	VOUTR	Analogue output	Right channel DAC output.
10	AGND	Supply	Analogue ground supply.
11	AVDD	Supply	Analogue positive supply.
12	VOUTL	Analogue output	Left channel DAC output.
13	CAP	Analogue output	Analogue internal reference.
14	BCKIN	Digital input	Audio data bit clock input.
15	DIN	Digital input	Serial audio data input.
16	LRCIN	Digital input	Sample rate clock input.
17	MUTE	Digital IO	Mute control pin, input or automute output. Low is not mute, high is mute, Z is automute.
18	MODE	Digital input	Mode select pin. Low is software mode, high is hardware control. Internal pull-down.
19	DVDD	Supply	Digital positive supply.
20	DGND	Supply	Digital ground supply.

Note:

Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Supply voltage	-0.3V	+7V
Reference input		VDD + 0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C
Package body temperature (soldering, 10 seconds)		+240°C
Package body temperature (soldering, 2 minutes)		+183°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		-10%	3.3 to 5	+10%	V
Analogue supply range	AVDD		-10%	3.3 to 5	+10%	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Analogue supply current	AVDD = 5V			17		mA
Digital supply current	DVDD = 5V			6		mA
Analogue supply current	AVDD = 3.3V			16		mA
Digital supply current	DVDD = 3.3V			3		mA
Standby analogue current	AVDD = 5V			1.7		mA
Standby digital current	DVDD = 5V			30		µA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Circuit Specifications						
SNR (Note 1)		AVDD, DVDD = 5V	95	101		dB
		AVDD, DVDD = 3.3V		100		dB
THD		0dB FS		-96	-85	dB
Dynamic range		THD+N @ -60dB FS	95	101		dB
Passband		±0.25dB			0.4535	fs
Stopband		-3dB	0.491			fs
Pass band ripple				±0.25		dB
Out of band rejection				-40		dB
Channel Separation				98		dB
Gain mismatch channel-to-channel		0dB FS		±0.5	±5	%FSR
Digital Logic Levels						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW level	V_{OL}	I_{OL} = 2mA			AV_{SS} + 0.3V	
Output HIGH level	V_{OH}	I_{OH} = 2mA	AVDD - 0.3V			
Analogue Output Levels						
Output level		Into 10kohm, full scale 0dB, (5V supply)		1.1		V_{RMS}
		Into 10kohm, full scale 0dB, (3.3V supply)		0.72		V_{RMS}
Minimum resistance load		To midrail or AC coupled (5V supply)		1		kohms
		To midrail or AC coupled (3.3V supply)		1		kohms
Maximum capacitance load		5V or 3.3V		100		pF
Output DC level				AVDD/2		V
Reference Levels						
Potential divider resistance		AVDD to CAP and CAP to AGND		90		kohms
Voltage at CAP				AVDD/2		
POR						
POR threshold				2.0		V

TERMINOLOGY

1. Signal-to-noise ratio (dB) (SNR) is a measure of the difference in level between the full-scale output and the output with no signal applied.
2. Dynamic range (dB) (DNR) is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (eg THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) is a ratio of the r.m.s. values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) (also known as Cross-Talk) is a measure of the amount one channel is isolated from the other. Normally measured by sending a full-scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

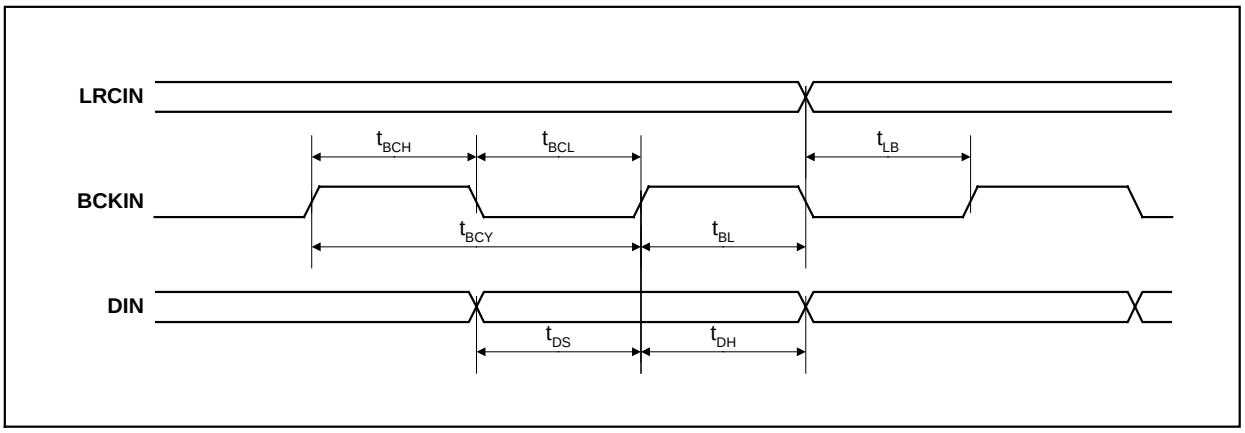


Figure 1 Audio Data Input Timing

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN pulse cycle time	t_{BCY}		100			ns
BCKIN pulse width high	t_{BCH}		40			ns
BCKIN pulse width low	t_{BCL}		40			ns
BCKIN rising edge to LRCIN edge	t_{BL}		20			ns
LRCIN rising edge to BCKIN rising edge	t_{LB}		20			ns
DIN setup time	t_{DS}		20			ns
DIN hold time	t_{DH}		20			ns

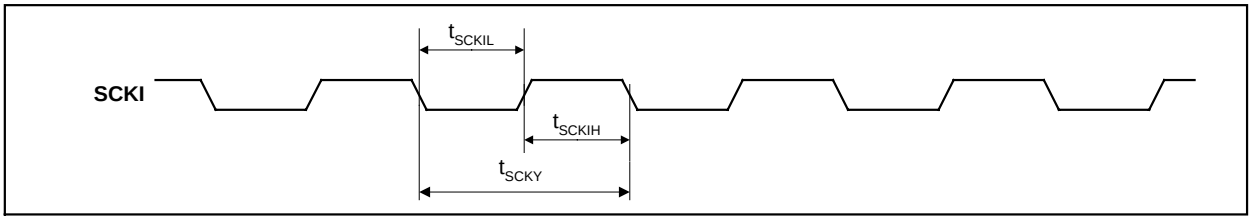


Figure 2 System Clock Timing Requirements

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
System clock pulse width high	t_{SCKIH}		10			ns
System clock pulse width low	t_{SCKIL}		10			ns
System clock cycle time	t_{SCKY}		27			ns

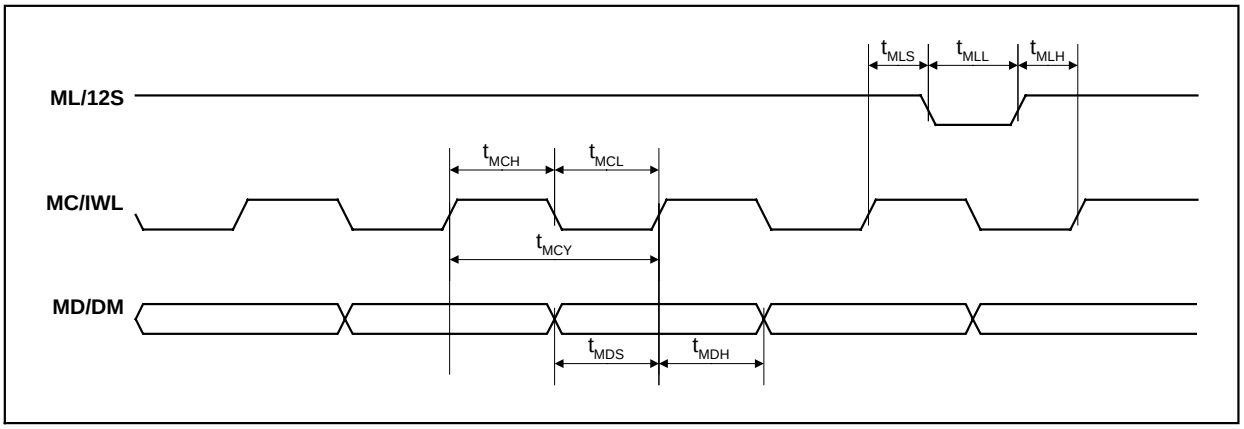


Figure 3 Program Register Input Timing

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
MC/IWL pulse cycle time	t_{MCY}		100			ns
MC/IWL pulse width low	t_{MCL}		40			ns
MD/DM pulse width high	t_{MCH}		40			ns
MD/DM set-up time	t_{MDS}		20			ns
MC/IWL hold time	t_{MDH}		20			ns
ML/I2S pulse width low	t_{MLL}		20			ns
ML/I2S set-up time	t_{MLS}		20			ns
ML/I2S hold time	t_{MLH}		20			ns

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured "A" weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

DEVICE DESCRIPTION

WM8720 is a complete stereo audio digital-to-analogue converter, including digital interpolation filter, multibit sigma delta with dither, switched capacitor multibit stereo DAC and output smoothing filters. Control of internal functionality of the device is by either hardware control (pin programmed) or software control (serial interface). The MODE pin selects between hardware and software control. In software control mode, an SPI type interface is used. This interface may be asynchronous to the audio data interface. Control data will be re-synchronized to the audio processing internally.

Operation using system clock of 256fs or 384fs is provided. Selection between clock rates is being automatically controlled in hardware mode, or serial controlled when in software mode. Sample rates (fs) from less than 8ks/s to 96ks/s are allowed, provided the appropriate system clock is input.

The data interface supports normal (Japanese right justified) and I^2S (Philips left justified, one bit delayed) interface formats, in both 'packed' and unpacked forms. When in hardware mode, the three serial interface pins become control pins to allow selection of input data format type (I^2S or normal), input word length (16, 18, 20, or 24-bit) and de-emphasis function.

SYSTEM CLOCK

The system clock for WM8720 must be either 256fs or 384fs, where fs is the audio sampling frequency (LRCIN) typically 32kHz, 44.1kHz, 48 or 96kHz. The system clock is used to operate the digital filters and the noise shaping circuits.

WM8720 has a system clock detection circuitry that automatically determines what the system clock frequency relative to the sampling rate is (to within ±8 system clocks). If greater than 8 clocks error, then the interface shuts down the DAC and mutes the output. The system clock should be synchronised with LRCIN, but WM8720 is tolerant of phase differences or jitter on this clock. Severe distortion in the phase difference between LRCIN and the system clock will be detected, and cause the device to automatically resynchronise. If the externally applied LRCIN slips in phase by more than half the internal LRCIN period, which is derived from master clock, then the interface resynchronises. Such a case would, for example, occur if repeated LRCIN clocks were received with only 252 systems clocks per period. In this case the interface would resynchronise every 64 LRCIN periods. During resynchronisation, the device will either repeat the previous sample, or drop the next sample, depending on the nature of the phase slip. This will ensure no discernible "click " at the analogue outputs during resynchronisation. Table 1 shows the typical system clock frequency inputs for the WM8720.

SAMPLING RATE (LRCIN)	SYSTEM CLOCK FREQUENCY (MHZ)	
	256fs	**384fs**
32kHz	8.192	12.288
44.1kHz	11.2896	16.9340
48kHz	12.288	18.432
96kHz	24.576	36.864

Table 1 System Clock Frequencies Versus Sampling Rate

AUDIO DATA INTERFACE

The Serial Data interface to WM8720 is fully compatible with both normal (MSB first, right-justified) or I^2S interfaces. Data may be 'packed' (number of serial bit clocks per LRCIN period is exactly 2 times the number of data bits, i.e. normally 32 in 16-bit mode) or unpacked (more than 32 bit clocks per LRCIN period).

The WM8720 will automatically detect 16-bit packed data being sent to the device in normal mode, and accept the data in this input format accordingly.

I^2S MODE	DESCRIPTION
0	Normal format (MSB-first, right justified)
1	I^2S format (Philips serial data protocol)

Table 2 Serial Interface Formats

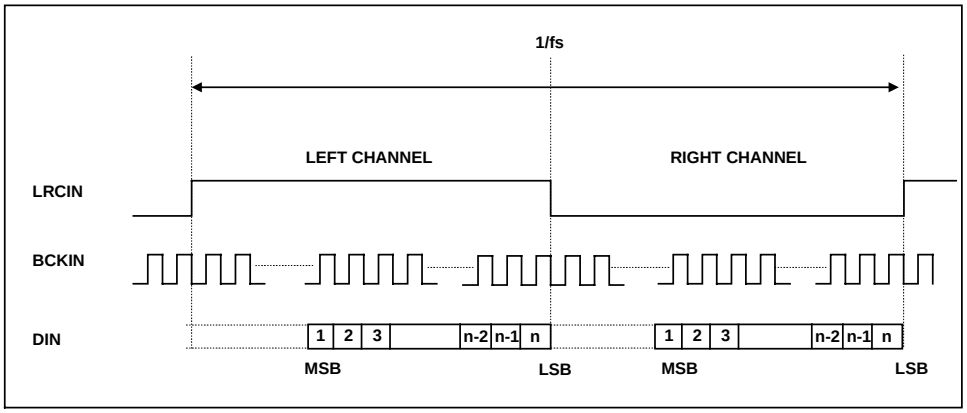


Figure 4 Normal Data Input Timing

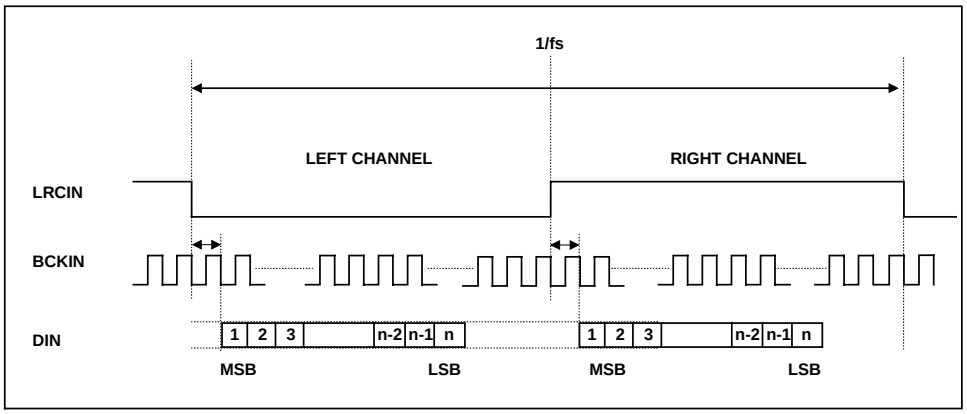


Figure 5 I^2S Data Input Timing

MODES OF OPERATION

Control of the various modes of operation is either by software control over the serial interface, or by hard-wired pin control. Selection of software or hardware mode is via MODE pin. The following functions may be controlled either via the serial control interface or by hard wiring of the appropriate pins.

FUNCTION		SOFTWARE CONTROL DEFAULT VALUE PIN 18: MODE = 0	HARDWARE CONTROL BEHAVIOUR PIN 18: MODE = 1
	OPTIONS		
Input audio data format	Normal format I^2S format	I^2S = 0 (default) I^2S = 1	Pin 4, 5: ML/ I^2S, MC/IWL = 00 or 01 or 10 Pin 4, 5: ML/I^2S, MC/IWL = 11
Input word length	16 18 20 24	IW[1:0] = 00 (default) IW[1:0] = 11 IW[1:0] = 01 IW[1:0] = 10	Pin 4, 5: ML/I^2S, MC/IWL = 00 Pin 4, 5: ML/I^2S, MC/IWL = 11 (I^2S only) Pin 4, 5: ML/I^2S, MC/IWL = 01 Pin 4, 5: ML/I^2S, MC/IWL = 10
De-emphasis selection	On Off	DE = 1 DE = 0 (default)	Pin 6: MD/DM = 1 Pin 6: MD/DM = 0
Mute	On Off	MU = 1 MU = 0 (default)	Pin 17: MUTE = 1 Pin 17: MUTE = 0
Power down control	WM8720 on WM8720 off	Available from Pin 1: PWDN	Pin 1: PWDN = 0 Pin 1: PWDN = 1
Input LRCIN polarity	Lch/Rch = High/low Lch/Rch = Low/high	LRP = 0 (default) LRP = 1	Not available in hardware mode, default value set
Volume control	Lch, Rch individually Lch, Rch common	ATC = 0; 0dB (default) ATC = 1	Not available in hardware mode, default 0dB
Infinite zero detect	On Off	IZD = 1 IZD = 0 (default)	Automute function controlled from MUTE pin Low = not mute Z = automute enable High = muted
Operation enable (OPE)	Enabled Disabled	OPE = 0 (default) OPE = 1	
DAC output control	See Table 11 for all options	Default is PL[3:0] = 1001, stereo mode	Not available in hardware mode

Table 3 Control Function Summary

HARDWARE CONTROL MODES

When the MODE pin is held high the following hardware modes of operation are available.

MUTE AND AUTOMUTE OPERATION

In both hardware and software modes pin 17 (MUTE) controls selection of mute directly, and can be used to enable and disable the automute function, or as an output of the automuted signal.

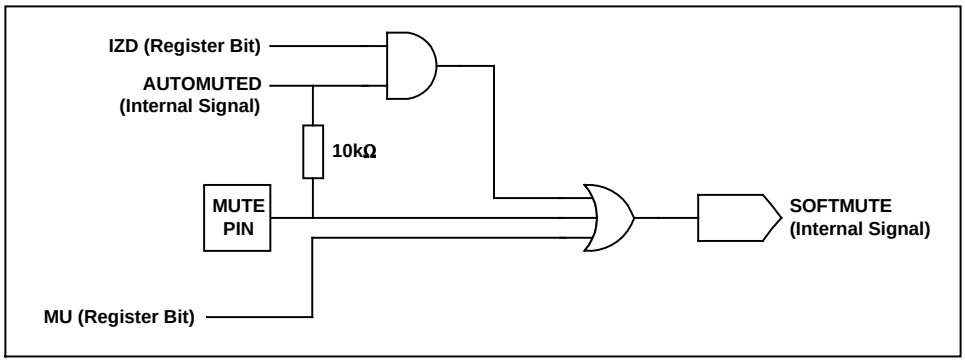


Figure 6 Mute Circuit Operation

The MUTE pin behaves as a bi-directional function, that is, as an input to select mute or NOT-mute, or as an output indication of automute operation. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter.

The automute function detects a series of zero value audio samples of 1024 samples long being applied to both left and right channels. After such an event, a latch is set whose output (automuted) is wire OR'ed through a 10kohm resistor to the MUTE pin. Thus if the MUTE pin is not being driven, the automute function will assert MUTE.

If MUTE is tied low, automute is overridden and will not mute. If MUTE is driven from a source follower, or diode, then both mute and automute functions are available. If MUTE is not driven, automute appears as a weak output (10k source impedance) so can be used to drive external mute circuits.

The automute signal is AND'ed with IZD, this qualified mute signal then being OR'ed into the SOFTMUTE control. Therefore, in software mode, automute operation may be controlled with IZD control bit.

I²S INPUT FORMAT SELECTION AND IWL INPUT FORMAT SELECTION

In hardware mode, pins 4 and 5 become input controls for selection of input data format type, and input data word length, see Table 4. I²S mode is designed to support any word length provided enough bit clocks are sent.

ML/I²S – PIN 4	MC/IWL – PIN 5	INPUT DATA MODE
0	0	16-bit normal
0	1	20-bit normal
1	0	24-bit normal
1	1	I²S mode

Table 4 Control of Input Data Format Type and Input Data Word Length

DM DE-EMPHASIS

In hardware mode, pin 6 becomes an input control for selection of de-emphasis filtering to be applied. See **Figure 8**.

DM	0	De-emphasis off
DM	1	De-emphasis on

Table 5 De-emphasis Control

PWDN POWERDOWN CONTROL

In both hardware and software modes, this pin selects powerdown of the entire device when taken high.

PWDN	0	Device powered up
PWDN	1	Device powered down

Table 6 Powerdown Control

SOFTWARE CONTROL INTERFACE

The WM8720 can be controlled using a 3-wire serial interface. MD/DM (pin 6) is used for the program data, MC/IWL (pin 5) is used to clock in the program data and ML/I2S (pin 4) is use to latch in the program data. The 3-wire interface protocol is shown in Figure 7.

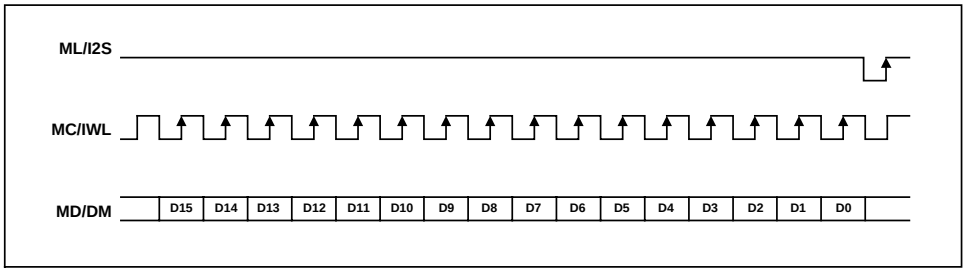


Figure 7 3-Wire Serial Interface

REGISTER MAP

WM8720 controls the special functions using 4 program registers, which are 16-bits long. These registers are all loaded through input pin MD/DM. After the 16 data bits are clocked in, ML/I2S/IWL is used to latch in the data to the appropriate register. Table 7 shows the complete mapping of the 4 registers.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
M0	--	-	-	-	-	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
M1	-	-	-	-	-	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
M2	-	-	-	-	-	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DE	MU
M3	-	-	-	-	-	A1	A0	IZD	SF1	SF0	-	-	-	ATC	LRP	I^2S

Table 7 Mapping of Program Registers

REGISTER NAME	BIT NAME	DEFAULT	DESCRIPTION
Register 0 (M0)	AL[7:0]	1111 1111	DAC attenuation data for left channel
A[1:0] = 00	LDL	0	Attenuation data load control for left channel
Register 1 (M1)	AR[7:0]	1111 1111	DAC attenuation data for right channel
A[1:0] = 01	LDR	0	Attenuation data load control for right channel
Register 2 (M2)	MU	0	Left and right DACs soft mute control
A[1:0] = 10	DE	0	De-emphasis control
	OPE	0	Left and right DACs operation control
	IW[1:0]	00	Input audio word resolution
	PL[3:0]	1001	DAC output control
Register 3 (M3)	I^2S	0	Audio data format select
A[1:0] = 11	LRP	0	Polarity of LRCIN (pin 7) select
	ATC	0	Attenuator control
	SF[1:0]	00	Sampling rate select
	IZD	0	Infinite zero detection circuit control and automute control

Table 8 Internal Register Mapping

DAC OUTPUT ATTENUATION

Register 0 (A[1:0] = 00) is used to control left channel attenuation. Bits 0-7 (AL[7:0]) are used to determine the attenuation level Table 9. The level of attenuation is given by:

Attenuation = [20.log10 (Attenuation_Data/256)] dB ..... Eqn. 1

AX[7:0]	ATTENUATION LEVEL
00(hex)	- ∞dB (mute)
01(hex)	-48.16dB
:	:
:	:
:	:
Fe(hex)	-0.07dB
FF(hex)	0dB

Table 9 Attenuation Control Levels

Bit 8 in register 0 (LDL) is used to control the loading of attenuation data in AL[7:0]. When LDL is set to 0, attenuation data will be loaded into AL[7:0], but it will not affect the attenuation level until LDL is set to 1. LDR in register 1 has the same function for right channel attenuation.

Register 1 (A[1:0] = 01) is used to control right channel attenuation in a similar manner.

Bit 2 in register 3 (A1[1:0] = 11) is used to control the attenuator (ATC). When ATC is high, the attenuation data loaded in program register 0 is used for both the left and the right channels. When ATC is low, the attenuation data for each register is applied separately to left and right channels.

LEFT AND RIGHT DACS SOFT MUTE CONTROL

Soft mute is controlled by setting bit MU, register 2:bit 0. A high level on MU (MU = 1) will cause the output to be muted, the effect of which is to ramp the signal down in the digital domain so that there is no discernible click. This can be seen in Figure 6 Mute Circuit Operation.

DE-EMPHASIS CONTROL

Bit 1 (DE) in register 2 is used to control digital de-emphasis. A low level on bit 1 (DE = 0) disables de-emphasis whilst a high level enables de-emphasis (DE = 1). De-emphasis applied to the filters shapes the frequency response of the digital filter according to the input sample frequency.

LEFT AND RIGHT DACS OPERATION CONTROL

Bit 2 (OPE) in register 2 is used for operation control. With OPE = 0 (default) the device functions normally. With OPE = 1 the device is disabled and the outputs are held at midrail. Current consumption of the digital section is minimized, but analogue sections remain active in order to preserve DC levels.

INPUT AUDIO WORD RESOLUTION

WM8720 allows maximum flexibility over the control of the audio data interface, allowing selection of format type, word length, and sample rates. Bits 3 and 4 of register 2 (IW[1:0]) are used to determine the input word resolution. WM8720 supports 16-bit, 18-bit, 20-bit and 24-bit formats as described in Table 10.

BIT 4 (IW1)	BIT 3 (IW0)	INPUT RESOLUTION
0	0	16-bit data word
0	1	20-bit data word
1	0	24-bit data word
1	1	18-bit data word

Table 10 Input Data Resolution

DAC OUTPUT CONTROL

Bits 5, 6, 7 and 8 (PL[3:0]) of register 2 are used to control the output format as shown in Table 11.

PL3	PL2	PL1	PL0	LEFT OUTPUT	RIGHT OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	Mute both channels
0	0	0	1	L	MUTE	
0	0	1	0	R	MUTE	
0	0	1	1	(L + R)/2	MUTE	
0	1	0	0	MUTE	L	
0	1	0	1	L	L	
0	1	1	0	R	L	Reverse channels
0	1	1	1	(L + R)/2	L	
1	0	0	0	MUTE	R	
1	0	0	1	L	R	Stereo mode
1	0	1	0	R	R	
1	0	1	1	(L + R)/2	R	
1	1	0	0	MUTE	(L + R)/2	
1	1	0	1	L	(L + R)/2	
1	1	1	0	R	(L + R)/2	
1	1	1	1	(L + R)/2	(L + R)/2	Mono mode

Table 11 Programmable DAC Output Format

SERIAL PROTOCOL

Bits 0 (I^2S) and 1 (LRP) of register 3 are used to control the input data format completely. A low on bit 0 (I^2S = 0) sets the format to Normal (MSB-first, right justified Japanese format), whilst a high (I^2S = 1) sets the format to I^2S (Philips serial data protocol).

POLARITY OF LRCIN SELECT

Bit 1 (LRP) of register 3 is used to control the polarity of LRCIN (sample rate clock). When bit 1 is low (LRP = 0), left channel data is assumed when LRCIN is in a high phase and right channel data is assumed when LRCIN is in a low phase. When bit 1 is high (LRP = 1), the polarity assumption is reversed.

INTERFACE CLOCKS AND SAMPLING RATES

Bits 6 (SF0) and 7 (SF1) of register 3 are used to control the sampling frequency, as shown in Table 12.

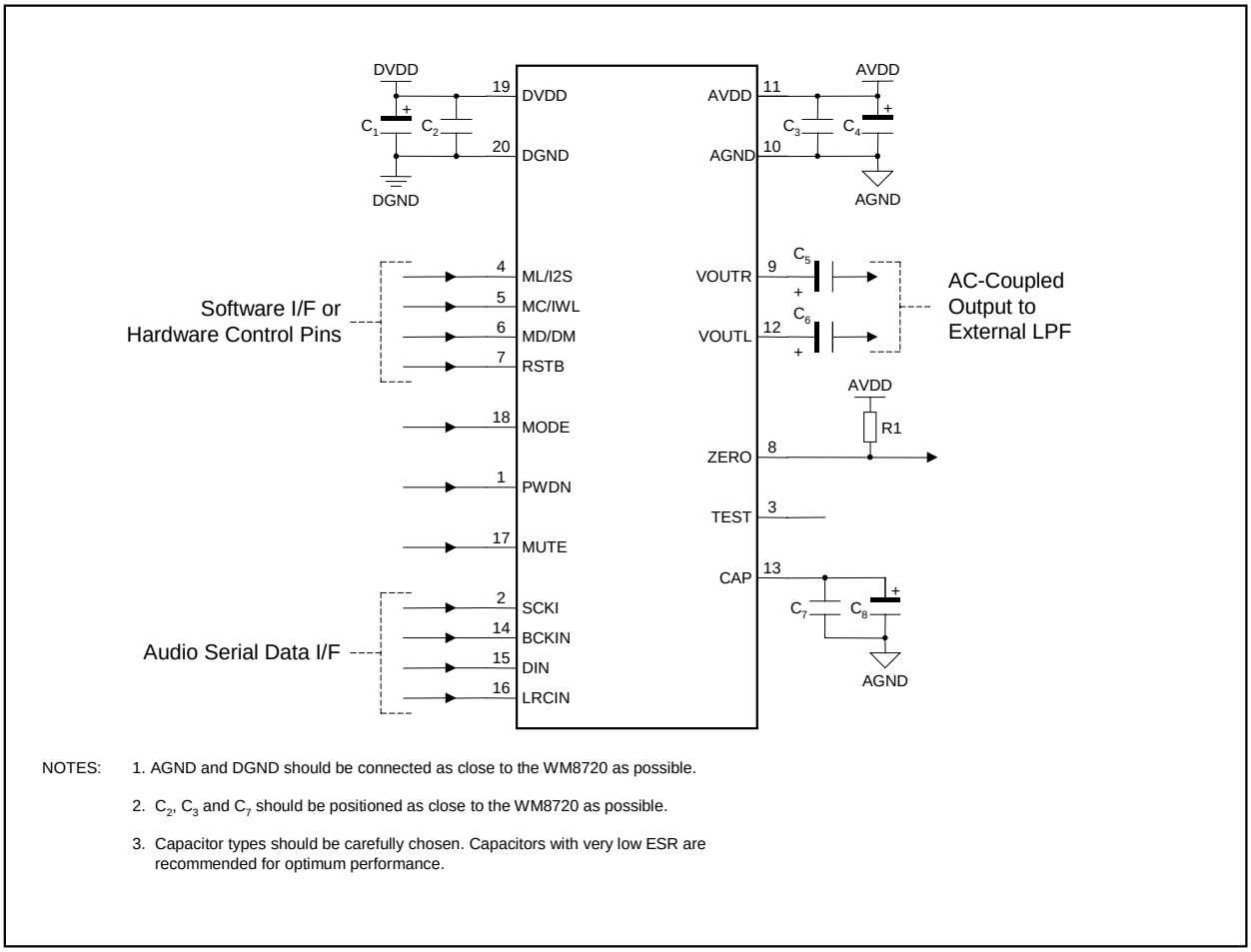
SF0	SF1	SAMPLING FREQUENCY	
0	0	44.1 kHz group	22.05 / 44.1 / 88.2 kHz
0	1	48 kHz group	24 / 48 / 96 kHz
1	0	32 kHz group	16 / 32 / 64 kHz
1	1	Reserved	Not defined

Table 12 Sampling Frequencies

INFINITE ZERO DETECTION

Bit 8 (IZD) in register 3 controls operation of the automute function. If IZD (Infinite Zero Detect) is high, 1024 consecutive zero audio samples will force the output to zero. See Figure 6. Note that the control of pin MUTE also affects automute operation. To turn off automute, pin MUTE must be held low as well as IZD being low (default).

RECOMMENDED EXTERNAL COMPONENTS



NOTES:
1. AGND and DGND should be connected as close to the WM8720 as possible.
2. C_2, C_3 and C_7 should be positioned as close to the WM8720 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.

Figure 8 External Components Diagram

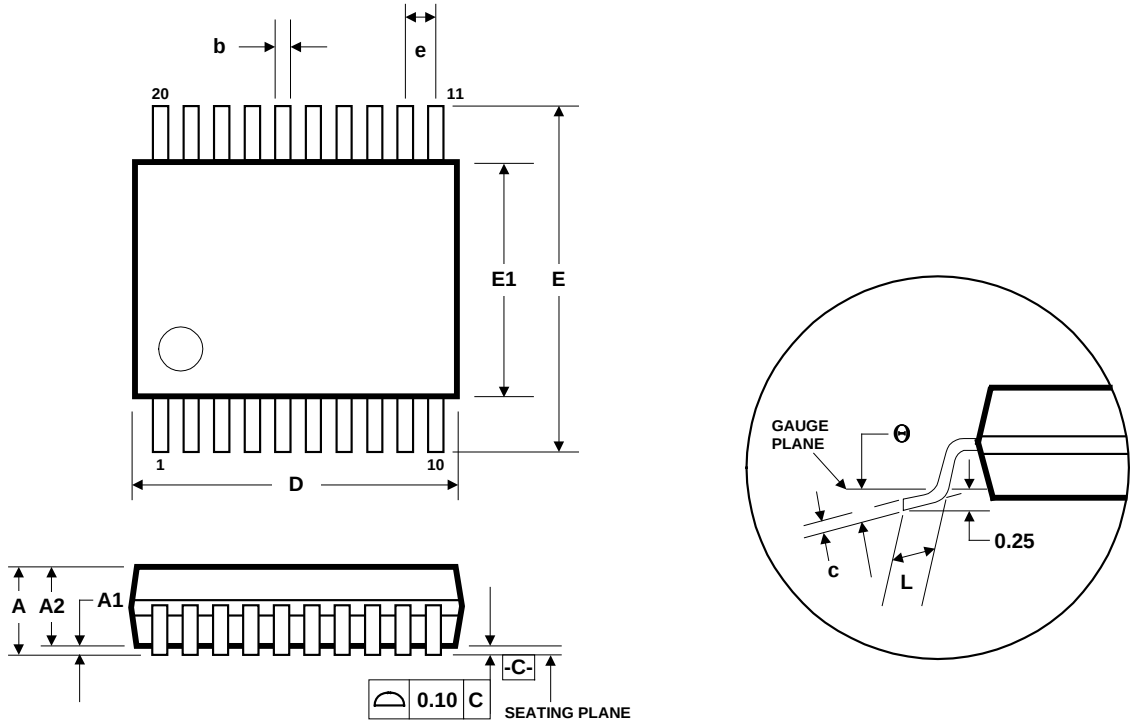
RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 and C4		10µF
C2 and C3		0.1µF
C5 and C6	10µF	Output AC coupling caps to remove midrail DC level from outputs.
C7	0.1µF	Reference de-coupling capacitors for CAP pin.
C8	10µF	
R1	10kΩ	Resistor to AVDD for open drain output operation.

Table 13 External Components Description

PACKAGE DIMENSIONS

DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm) **DM0015.A**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.65	1.75	1.85
b	0.22	-----	0.38
c	0.09	-----	0.25
D	6.90	7.20	7.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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