LINE OSCILLATOR COMBINATION

Technology: Bipolar

Features:

- o Line oscillator based on the threshold switching principle
- o Phase comparison between sync. pulse and oscillator (φ_1)
- o Internal gating pulse for phase detector φ_1 (additional noise suppression)
- o Phase comparison between fly-back pulse and oscillator (φ_2)
- o Extension of pull in range by coincidence detector φ_3 (coincidence between sync. and gating pulse)
- o Time constant switch for VTR operation
- o Sync. separator
- o Noise separator
- o Vertical sync. separator and output stage
- o Colour burst keying and line flyback blanking pulse generator
- o Phase shifter for output pulse
- o Output pulse duration switching
- o Output stage with separate voltage supply for direct thyristor triggering or driver transistor command
- o Low supply voltage protection

Case:

16 pin dual inline plastic

Absolute maximum ratings
Reference point pin 16

Supply voltages	Pin 1	V_{S1}	13.2	V
	Pin 2	V_{S2}	18.0	V
Input voltages	Pin 4	V_I	13.2	V
	Pin 9	$\pm V_I$	6.0	V
	Pin 10	$\pm V_I$	6.0	V
Output voltage	Pin 11	V_o	13.2	V
Input currents	Pin 4	I_I	1	mA
	Pin 6	$\pm I_I$	10	mA
Output currents	Pin 7	$-I_o$	10	mA
	Pin 11	I_o	2	mA
Thyristor operating	Pin 3	$-I_o=I_{S2}$	650	mA
Transistor operating	Pin 3	$-I_o=I_{S2}$	450	mA

T1.2/1747.0589 E

Power dissipation T_{amb} = 25 °C	P_{tot}	800	mW
Junction temperature	T_j	125	°C
Ambient temperature range	T_{amb}	-20 ... + 70	°C
Storage temprature range	T_{stg}	-25 ... + 125	°C

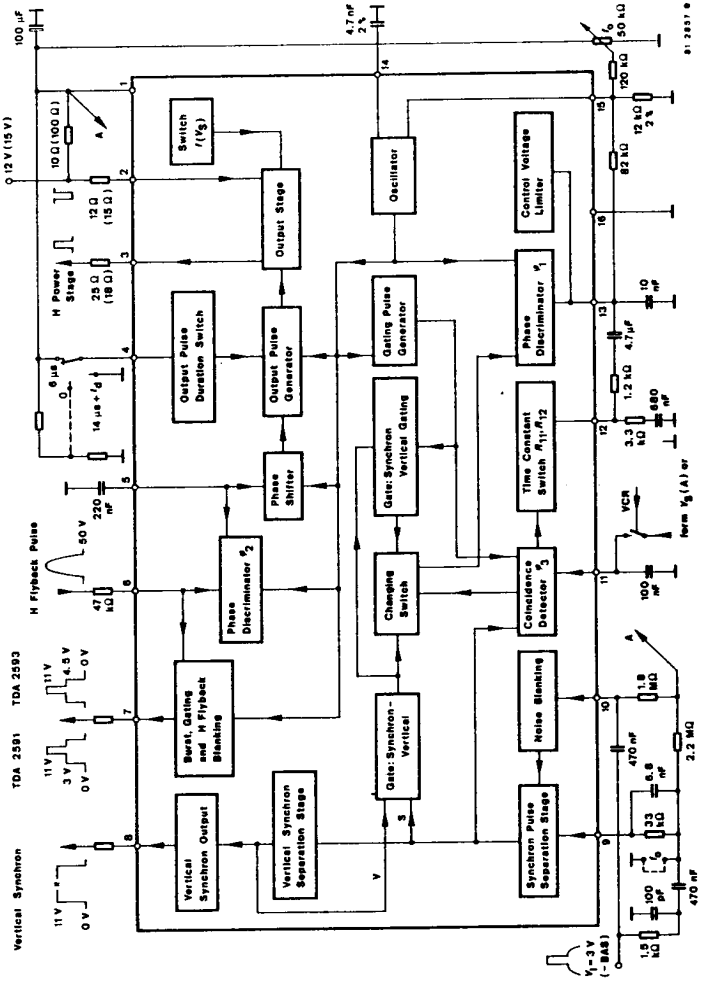


Fig. 1 Block diagram and application

Electrical characteristics

V_S = 12 V, reference point pin 16,
T_{amb} = 25 °C, unless otherwise specified

		Min.	Typ.	Max.	
Inputs					
Sync. pulse separator **Pin 9**					
Input switching voltage	V_i		0.8		V
Input switching current	I_i			5	µA
Input gating current	I_{IG}	5		100	µA
Input switch-off current	I_{OFF}	100	150		µA
Input blocking current V_i = -5 V	I_i			1	µA
Input signal (-BAS)	$-V_{IBAS}$	1	3	7	V_{pp}
Noise separator **Pin 10**					
Input switching voltage	V_i		1.4		V
Input switching current	I_i	100	150		µA
Input gating current	I_{IG}	5		100	µA
Input blocking current V_i = -5 V	I_{IOFF}			1	µA
Input signal (-BAS)	$-V_{IBAS}$	1	3	7	V_{pp}
Superimposed noise voltage	V_{in}			7	V_{pp}
Line flyback pulse input **Pin 6**					
Input switching voltage	V_{IT}		1.4		V
Input limiting voltage	V_I	-0.7		1.4	V
Input current	I_i	0.01	1		mA
VCR-Switching **Pin 11**					
Input voltage $-I_I \leqq 200$ µA	V_I	0		2.5	V
$I_I \leqq$ 2 mA	V_I	9		V_S	V

			Min.	Typ.	Max.	
Pulse duration switch	**Pin 4**					
Thyristor operating $I_I \leqq 200\ \mu A, t_{pTh} = 7\ \mu s$	Fig. 2	V_I	9.4		V_S	V
Transistor operating $-I_I \leqq 200\ \mu A, t_{pTh} = t_d + 14\ \mu s$ $V_3 = 0$, $t_p = 0$, $I_I = 0$	Fig. 2	V_I	0		3.5	V
		V_I 1)	5.4		6.6	V
Outputs						
Vertical pulse positive going Pin 8						
Output voltage		V_o	10	11		V_{pp}
Output resistance		R_o		2		kΩ
Delay between leading edge of input and output signal		t_{dON}		15		µs
Delay between trailing edge of input and output signal		t_{dOFF}		15		µs
Burst gating pulse	**Pin 7**					
Output voltage	Fig. 2	V_o	10	11		V_{pp}
Output resistance		R_o		70		Ω
Output current during trailing edge		I_o		2		mA
Burst gating pulse width $V_o = 7$ V	Fig. 2	t_{Burst}	3.7	4.0	4.3	µs
Phase relation between middle of sync. pulse at the input U_i and the leading edge of the burst gating pulse $V_o = 7$ V	Fig. 2	$t_{\varphi Burst}$	2.15	2.65	3.15	µs
Flyback blanking pulse	**Pin 7**					
Output voltage	**TDA 2591**	V_o	2.5		3.5	V_{pp}
	TDA 2593	V_o	4		5	V_{pp}

1) or input pin 4 "Open"

			Min.	Typ.	Max.	
Output resistance		R_o		70		Ω
Output current during trailing edge		I_o		2		mA
Line drive pulse	**Pin 3**					
Output voltage		V_o		10.5		V_{pp}
Output resistance for leading edge H		R_{oH}		2.5		Ω
Output resistance for trailing edge L		R_{oL}		20		Ω
Output pulse duration, Thyristor operating V_I = 9.4...4 V	Fig. 2	t_{pTh}	5.5	7.0	8.5	µs
Output pulse duration, Transistor operating V_I = 0...4 V, t_{fly} = 12 µs	Fig. 1	t_{pT}		14µs+t_d		
Supply voltage for switching off the output pulse V_o = 0		V_S		4		V
Overall phase relation						
Phase relation between middle of sync. pulse and the middle of fly-back pulse t_{fly} = 12 µs		Δt	1.9	2.6	3.3	µs

The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase detector m_2.

Additional adjustment is possible by current supplying into pin 5 according to:

$$\frac{I_0}{t_p} = 30\ \mu A/\mu s$$

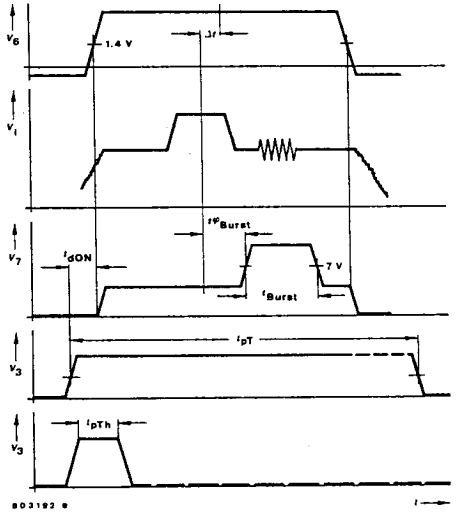
Oscillator	**Pin 14,15**					
Threshold voltage low level	Pin 14	V_{TU}		4.4		V
Threshold voltage high level	Pin 14	V_{TO}		7.6		V

			Min.	Typ.	Max.	
Recharge current		$+I_{CH}$		0.47		mA
Oscillator frequency (free running) C_{osc} = 4.7 nF; R_{osc} = 12 kΩ		f_{osc}		15.625		kHz
Spread of oscillator frequency		Δf_{osc} 2)			± 5	%
Frequency control sensitivity	Pin 15	$\frac{\Delta f_{osc}}{\Delta I_{15}}$ 2)		31		Hz/µA
Adjustment range of network		Δf_{osc}		±10		%
Influence of supply voltage on frequency		$\frac{\Delta f_{osc}/F_{osc}}{\Delta V_S/V_S}$ 2)			±0.05	%
Change of frequency when V_S drops to: V_S = 5 V		Δf_{osc} 2)			± 10	%
Temperatur coefficient of oscillator frequency		TKf_{osc} 2)			$\pm 10^{-4}$	1/K
Phase comparison φ_1	**Pin 13**					
Control voltage range		V_{oc}	3.8		8.2	V
Control current		$\pm I_{oc}$	1.9		2.3	mApp
Output blocking current V_{oc} = 4...8 V		I_{OFF}			1	µA
Output resistance V_{oc} = 4...8 V		R_o 3)			high ohmic	
$V_{oc} \leqq$ 3.8 V or $\geqq$ 8.2 V		R_o 4)			low ohmic	
Control sensitivity		$S\varphi$		2		kHz/µs
Catching and holding range $R_{13,15}$ = 82 kΩ		Δf		±780		Hz
Spread of catching and holding range		$\Delta(\Delta f)^2$		± 10		%

2) Excluding external component tolerances
3) Current source
4) Emitter follower

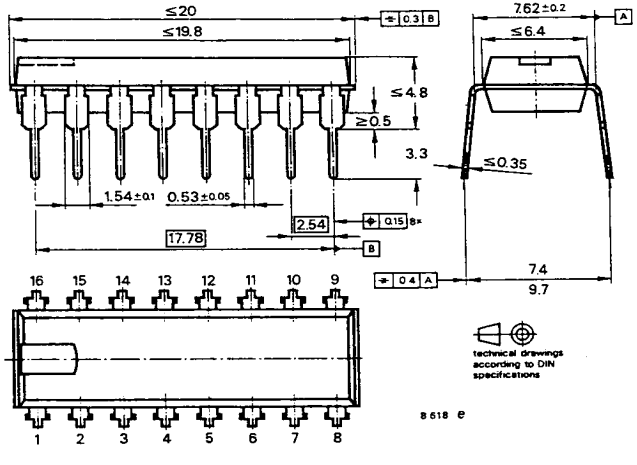
		Min.	Typ.	Max.	
Phase comparison φ_2 and phase shifter **Pin 5**					
Control voltage range	V_{oc}	5.4		7.6	V
Control current	$\pm I_{oc}$		1		mAp
Output blocking current V_{oc} = 5.4...7.6 V	I_{OFF}			5	µA
Output resistance V_{oc} = 5.4...7.6 V	R_o3)			high ohmic	
$V_{oc} \leqq 5.4$ or $\geqq 7.6$ V	R_o		8		kΩ
Permissible delay between leading edge of output pulse and leading edge of flyback pulse t_{fly} = 12 µs	t_d			15	µs
Static control error	$\frac{\Delta t}{\Delta t_{dON}}$			0.2	%
Coincidencedetector φ_3 **Pin 11**					
Output voltage	V_o	0.5		6.0	V
Output current without coincidence	I_o		0.1		mA
with coincidence	$-I_o$		0.5		mA
Time constant switch **Pin 12**					
Output voltage	V_o		6.0		V
Output current limited to:	$\pm I_o$			1	mA
Output resistance V_o = 2.5...7.0 V	R_o		100		Ω
$V_o = \leqq 1.5$ V, $\geqq 9.0$ V	R_o		60		kΩ
Pulse duration generator					
Pulse duration	t_p		7.5		µs

Fig. 2 Relationship of phases



t_{fly}	Flyback pulse
V_i	Video input signal
$t_{\varphi Burst}$	Burst and blanking pulse
t_{Burst}	
t_{pT}	Output pulse for transistor operating. $V_4 \leqq 3.55$ V
t_{pHt}	Output pulse for thyristor operating. $V_4 = 9.4 \ldots V_S$

Dimensions in mm



Case

JEDEC MO 001
DIP 16-leads