

## N - Channel 60- V (D-S) MOSFET

The 2N7002k is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

### General Features

$$\frac{1}{2} V_{DS} = 60V, I_D = 0.3A$$

$$R_{DS(ON)} < 3 \quad @ \quad V_{GS}=5V$$

$$R_{DS(ON)} < 2 \quad @ \quad V_{GS}=10V$$

ESD Rating ÖHBM 2300V

½ High power and current handing capability

½ Lead free product is acquired

½ Surface mount package

### Application

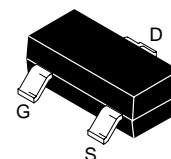
½Direct logic-level interface: TTL/CMOS

½Drivers: relays, solenoids, lamps, hammers,display, memories, transistors, etc.

½Battery operated systems

½Solid-state relays

## Package outline



**SOT-23**

N-Channel MOSFET

## Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
7002K	2N7002K	SOT-23	Ø180mm	8 mm	3000 units

## Absolute Maximum Ratings (T<sub>A</sub>=25 unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current (T <sub>J</sub> =150 )	I <sub>D</sub>	T <sub>A</sub> =25	0.3
		T <sub>A</sub> =100	0.19
Drain Current-Pulsed (Note 1)	I <sub>DM</sub>	0.8	A
Maximum Power Dissipation	P <sub>D</sub>	0.35	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 To 150	

## Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	R <sub>JA</sub>	350	/W
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## Electrical Characteristics (T<sub>A</sub>=25 unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250 A	60	68	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	A
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V	-	±100	±500	nA
		V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	±4	±10	uA
On Characteristics (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 A	1	1.7	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =5V, I <sub>D</sub> =0.4A	-	1.3	3	
		V <sub>GS</sub> =10V, I <sub>D</sub> =0.5A	-	1	2	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =0.2A	0.1	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	21	50	PF
Output Capacitance	C <sub>oss</sub>		-	11	25	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	4.2	5	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =0.2A V <sub>GS</sub> =10V, R <sub>GEN</sub> =10	-	10	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	50	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	17	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	10	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =0.3A, V <sub>GS</sub> =4.5V	-	1.7	3	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =0.2A	-	-	1.3	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	0.2	A

### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t<sub>r</sub> " 10 sec.
3. Pulse Test: Pulse Width " 300 s, Duty Cycle " 2%.
4. Guaranteed by design, not subject to production

Typical Electrical And Thermal Characteristics

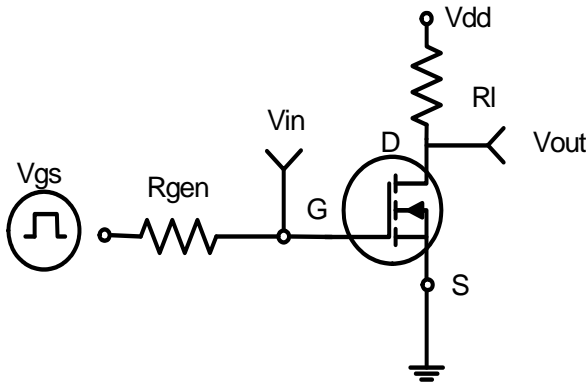


Figure 1: Switching Test Circuit

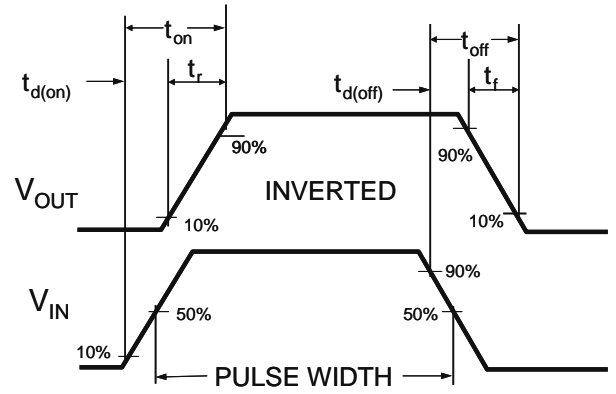


Figure 2: Switching Waveforms

I<sub>D</sub>- Drain Current (A)

V<sub>DS</sub> Drain-Source Voltage (V)  
Figure 3 Output Characteristics

I<sub>D</sub>- Drain Current (A)

V<sub>GS</sub> Gate-Source Voltage (V)  
Figure 4 Transfer Characteristics

R<sub>DS(on)</sub> On-Resistance (Ω)

I<sub>D</sub>- Drain Current (A)  
Figure 5 Drain-Source On-Resistance

R<sub>DS(on)</sub> On-Resistance (Ω)

V<sub>GS</sub> Gate-Source Voltage (V)  
Figure 6 R<sub>DS(on)</sub> vs V<sub>GS</sub>

Vgs Gate-Source Voltage (V)

Qg Gate Charge (nC)  
Figure 7 Gate Charge

I<sub>s</sub>- Reverse Drain Current (mA)

Vsd Source-Drain Voltage (V)  
Figure 8 Source-Drain Diode Forward

Normalized On-Resistance

T<sub>J</sub>-Junction Temperature( )  
Figure 9 Drain-Source On-Resistance

I<sub>D</sub>- Drain Current (A)

Vds Drain-Source Voltage (V)  
Figure 10 Safe Operation Area

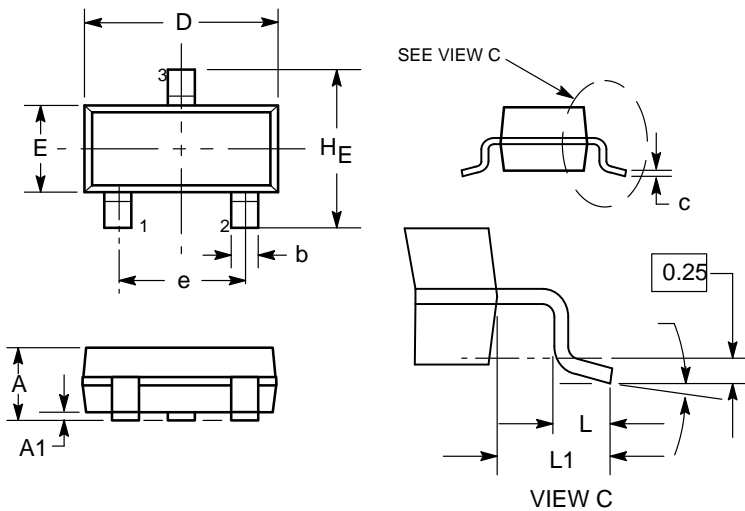
r(t), Normalized Effective  
Transient Thermal Impedance

Square Wave Pulse Duration(sec)  
Figure 11 Normalized Maximum Transient Thermal Impedance

Package Dimensions

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SOT-23



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. 318 i01 THRU i07 AND i09 OBSOLETE, NEW STANDARD 318 i08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104

- STYLE 6:  
 PIN 1. BASE  
 2. EMITTER  
 3. COLLECTOR

SOLDERING FOOTPRINT\*

