GenerAL Description

N - Channel 60- V (D-S) MOSFET

The 2N7002k is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

General Features

½ V_{DS} = 60V,I_D = 0.3A

$R_{DS(ON)}$ < 3 @ V_{GS}=5V

$R_{DS(ON)}$ < 2 @ V_{GS}=10V

ESD Rating ÖHBM 2300V

½ High power and current handing capability

½ Lead free product is acquired

½ Surface mount package

Application

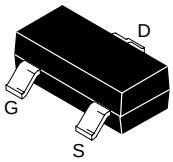
½Direct logic-level interface: TTL/CMOS

½Drivers: relays, solenoids, lamps, hammers,display, memories, transistors, etc.

½Battery operated systems

½Solid-state relays

Package outline



SOT–23

N-Channel MOSFET

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
7002K	2N7002K	SOT-23	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings (T $_A$=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J =150)	T_A =25	I_D	0.3	A
	T_A =100		0.19	
Drain Current-Pulsed (Note 1)		I_{DM}	0.8	A
Maximum Power Dissipation		P_D	0.35	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	R $_{JA}$	350	/W

Electrical Characteristics (T_A=25 unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250 A	60	68	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	A
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V	-	±100	±500	nA
		V_{GS}=±20V,V_{DS}=0V	-	±4	±10	uA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250 A	1	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=5V, I_D=0.4A	-	1.3	3	
		V_{GS}=10V, I_D=0.5A	-	1	2	
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=0.2A	0.1	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	21	50	PF
Output Capacitance	C_{oss}		-	11	25	PF
Reverse Transfer Capacitance	C_{rss}		-	4.2	5	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=0.2A V_{GS}=10V,R_{GEN}=10	-	10	-	nS
Turn-on Rise Time	t_r		-	50	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	17	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=0.3A, V_{GS}=4.5V	-	1.7	3	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=0.2A	-	-	1.3	V
Diode Forward Current (Note 2)	I_S		-	-	0.2	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ” 10 sec.
3. Pulse Test: Pulse Width ” 300 s, Duty Cycle ” 2%.
4. Guaranteed by design, not subject to production

Typical Electrical And Thermal Characteristics

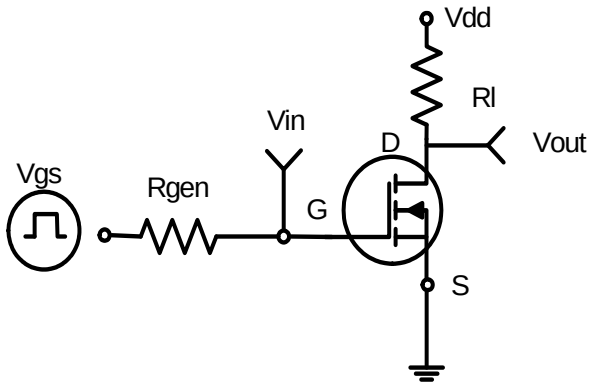


Figure 1:Switching Test Circuit

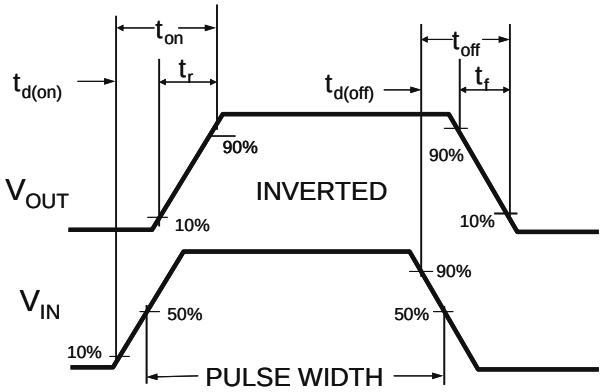


Figure 2:Switching Waveforms

I_D- Drain Current (A)

Vds Drain-Source Voltage (V)

Figure 3 Output Characteristics

I_D- Drain Current (A)

Vgs Gate-Source Voltage (V)

Figure 4 Transfer Characteristics

Rdson On-Resistance(i)

I_D- Drain Current (A)

Figure 5 Drain-Source On-Resistance

Rdson On-Resistance(i)

Vgs Gate-Source Voltage (V)

Figure 6 Rdson vs Vgs

Qg Gate Charge (nC)

Figure 7 Gate Charge

Vsd Source-Drain Voltage (V)

Figure 8 Source-DrainDiode Forward

T_J-Junction Temperature( )

Figure 9 Drain-Source On-Resistance

Vds Drain-Source Voltage (V)

Figure 10 Safe Operation Area

Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

Package Dimensions

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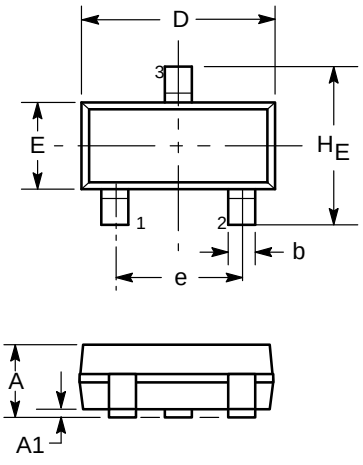

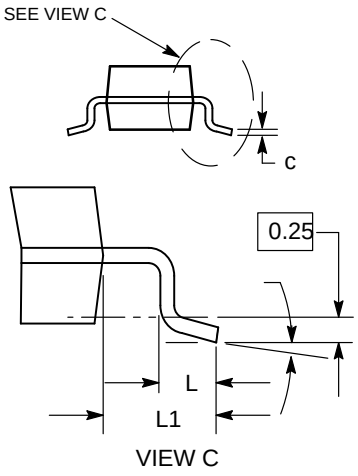

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318 ï01 THRU ï07 AND ï09 OBSOLETE, NEW STANDARD 318 ï08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*